AN3971
Application note

STEVAL-ISV005V2: solar battery charger for lead acid batteries based on the SPV1020 and SEA05

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Introduction

For photovoltaic standalone installations, both battery charging management and an efficient solar energy harvesting system are required.

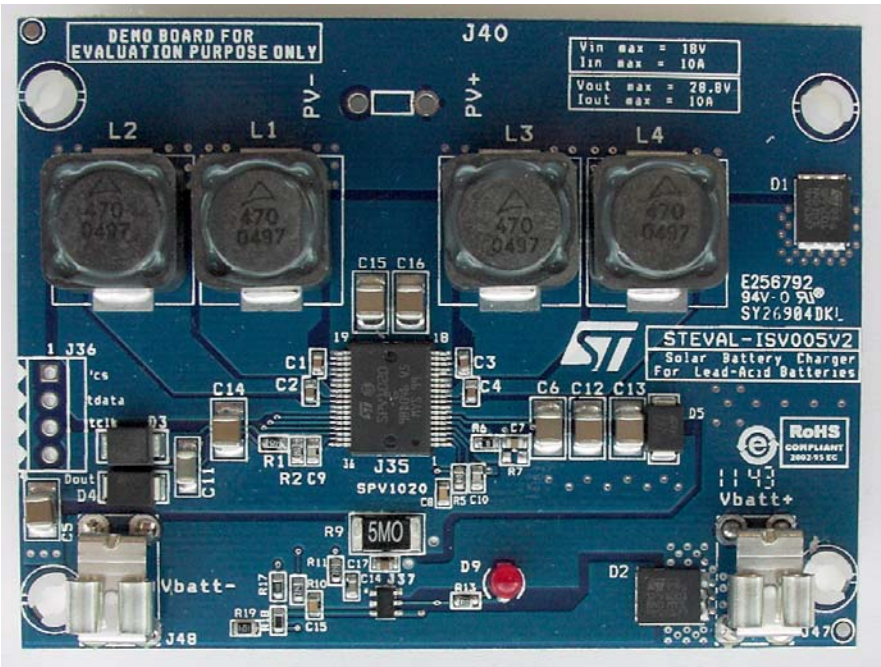
The lead acid battery charging control (which is a key feature, in terms of costs, in off-grid PV installations) must optimize both the charging time and the lifetime of the battery.

To optimize the energy extraction, the solar energy harvesting system needs a power conversion unit which performs an MPPT (max. power point tracking) algorithm.

The STEVAL-ISV005V2 is a demonstration board for users designing an MPPT-based lead acid battery charger using the SPV1020, which is a high efficiency, monolithic, step-up converter, with interleaved topology (IL4) and implementing MPPT.

In addition to the SPV1020, and to prevent battery overvoltage and overcurrent, the STEVAL-ISV005V2 system architecture proposes a solution with the SEA05 (CC-CV: constant current-constant voltage) IC.

Figure 1. STEVAL-ISV005V2 demonstration board



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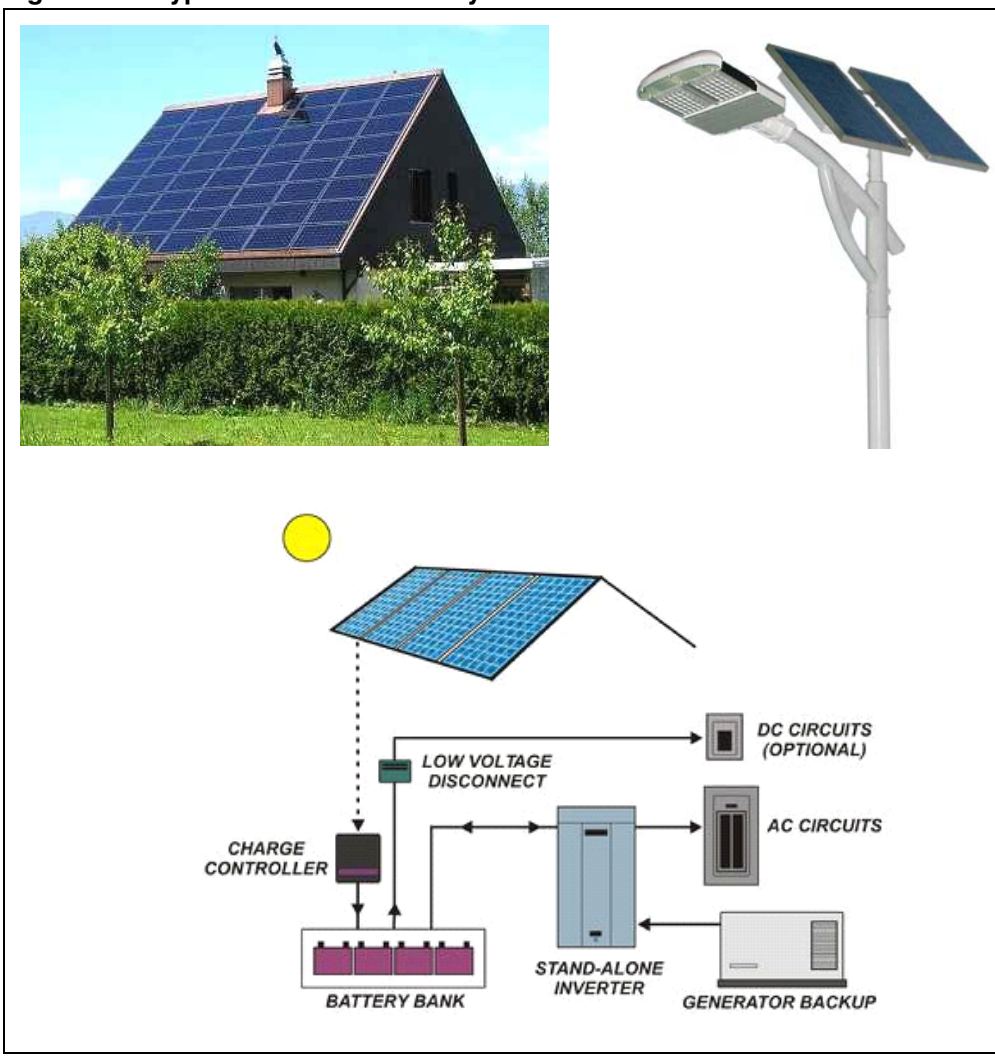
1 Application overview

The standalone photovoltaic (PV) system is a solution normally used in remote or isolated locations where the electric supply from the power-grid is unavailable or not available at a reasonable cost, such as mountain retreats or remote cabins, isolated irrigation pumps, emergency telephones, isolated navigational buoys, traffic signs, boats, camper vans, etc.

They are most suitable for users with a limited power need.

It is estimated that about 60% of all PV modules are used in these standalone applications, where the rechargeable batteries are normally used to store the energy surplus and supply the load in case of low renewable energy production.

Figure 2. Typical stand-alone PV systems



The primary function of a charge controller in a standalone PV system is to maintain the battery at the highest possible state of charge, and to protect it from overcharge by the array and from over-discharge by the loads.

Although some PV systems can be effectively designed without the use of charge control, any system that has unpredictable loads, user intervention, optimized or undersized battery storage (to minimize initial cost), typically requires a battery charge controller.

The algorithm or control strategy of a battery charge controller determines the effectiveness of battery charging and PV array utilization, and ultimately the ability of the system to meet the load demands.

Important functions of battery charge controllers and system controls are:

- To prevent battery overcharge: to limit the energy supplied to the battery by the PV array when the battery becomes fully charged
- To prevent battery over-discharge: to disconnect the battery from electrical loads when the battery reaches a low state of charge
- To provide load control functions: to automatically connect and disconnect an electrical load at a specified time, for example, operating a lighting load from sunset to sunrise.

The most common battery type used is the valve regulated lead acid (VRLA) battery, because of its low cost, maintenance-free operation and high efficiency characteristics.

Although the battery installation cost is relatively low compared to that of PV systems, the lifetime cost of the battery is greatly increased because of the limited service time.

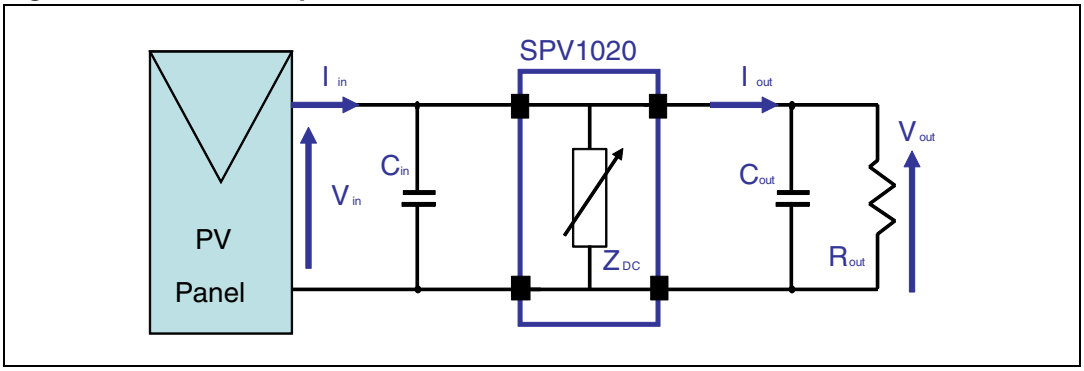
The lifetime parameter is reduced if there is low PV energy availability for prolonged periods or improper charging control, both resulting in low battery state of charge (SOC) levels for long time periods.

An increase in the lifetime of the battery results in improved reliability of the system and a significant reduction in operating costs. The life of a lead acid battery can be extended by avoiding critical operating conditions such as overvoltage and overcurrent during the charge.

2 Optimizing the energy from the panel

To guarantee the maximum power extraction from a photovoltaic panel, a real-time execution of a MPPT algorithm is needed. In the SPV1020 implementation the algorithm allows the changing of the DC-DC converter duty cycle according to the panel irradiation. In other words, the power conversion system based on the SPV1020 matches the impedance of the load to the dynamic output impedance of the panel.

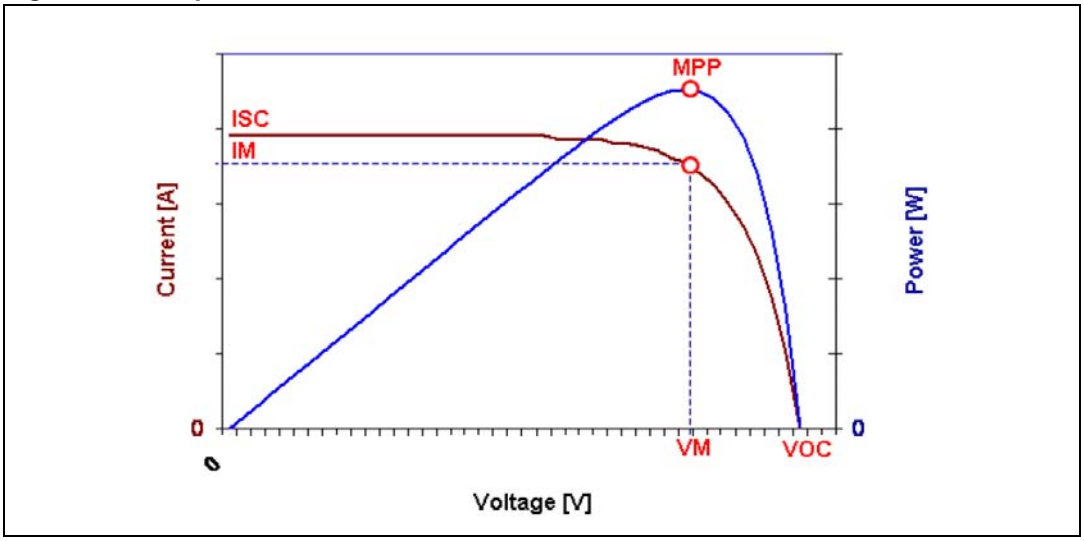
Figure 3. SPV1020 equivalent circuit



Each Z affects power transfer between the input source and output load and for each Z an input voltage (V_{in}) and current (I_{in}) can be measured. The purpose of the MPPT algorithm is to guarantee $Z = Z_M$, where Zm is the impedance of the source and Z is the impedance of the load which must match Zm to guarantee maximum power is extracted from the source. ($P_{in} = V_{in} * I_{in}$) is maximum ($P_{mpp} = V_{mpp} * I_{mpp}$).

In order to understand the tracking efficiency, it is best to graph the voltage-current curve, which shows all the available working points of the PV panel at a given solar irradiation. The voltage-power curve is derived from the voltage-current curve, plotting the product V*I for each voltage applied. *Figure 4* shows both the typical curves voltage-power and voltage-current of a photovoltaic panel.

Figure 4. I/V panel electrical curve



This algorithm approach is defined as perturb & observe because the system is excited (perturbed) with a certain DC, then power is monitored (observed) and then perturbed with a new duty cycle depending on the monitoring result.

The SPV1020 IC executes the MPPT algorithm with a fixed period (equal to 256 times the switching period), required for the application to stabilize its behavior (voltages and currents) with the new duty cycle.

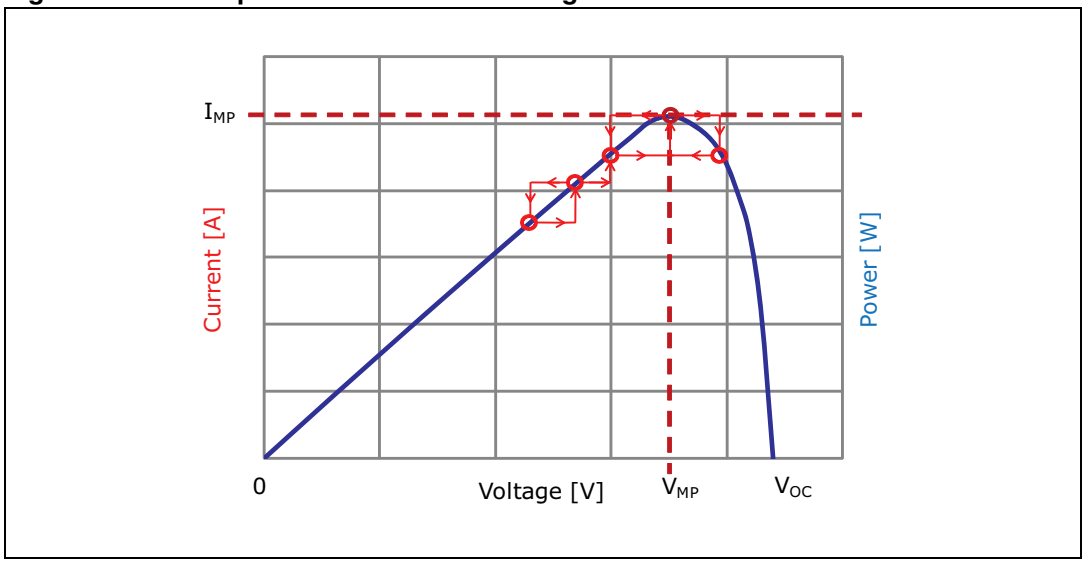
The duty cycle increase or decrease depends on the update done in the previous step and by the direction of the input power.

The MPPT algorithm compares the current input power (P_{tn}) with the input power computed in the previous step (Ptn-1).

If power is increasing then the update is done in the same direction as in the previous step. Otherwise the update is swapped in the opposite direction (from increasing to decreasing or vice-versa).

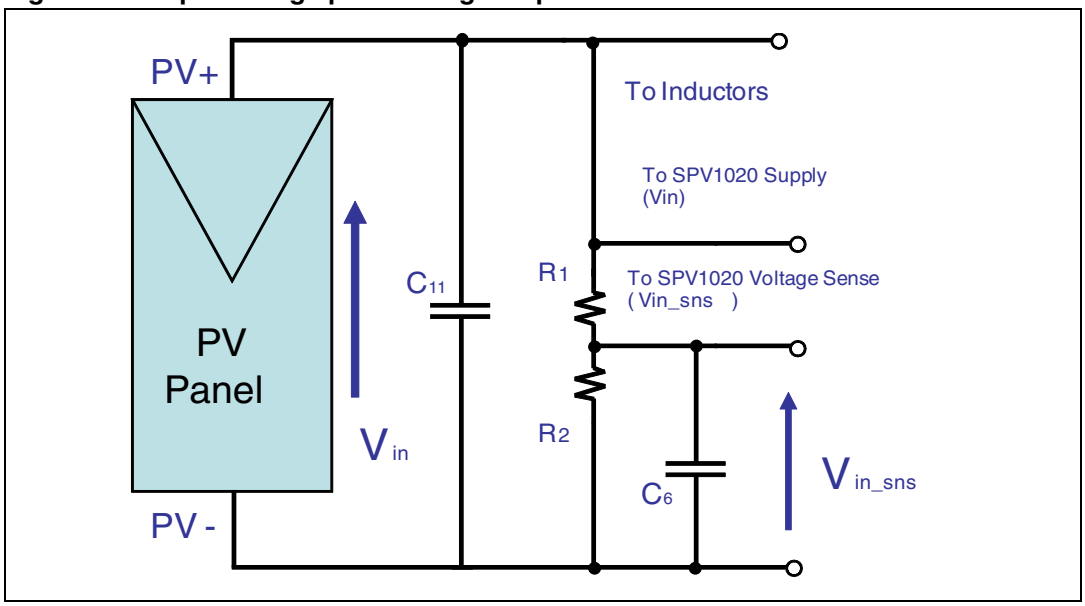
Figure 5 shows the sampling/working points (red circles) set by the SPV1020 and how they change (red arrows) during normal operating mode.

Figure 5. MPPT perturb & observe tracking



The input voltage is sampled by an external resistive partitioning, while the input current is sampled internally in order to reduce the external component. Here follows a simple schematic of the input voltage sensing circuitry (see the SPV1020 datasheet).

Figure 6. Input voltage partitioning sample circuit



Input voltage partitioning is important in order to adapt the correct panel to insert in the standalone PV system, also according to the battery current capability and the charging time necessary to reach the total battery SOC.

2.1 Regulations, protection, and features

The STEVAL-ISV005V2 implements the application settings to use the protection provided by the SPV1020 IC, which can be summarized as follows:

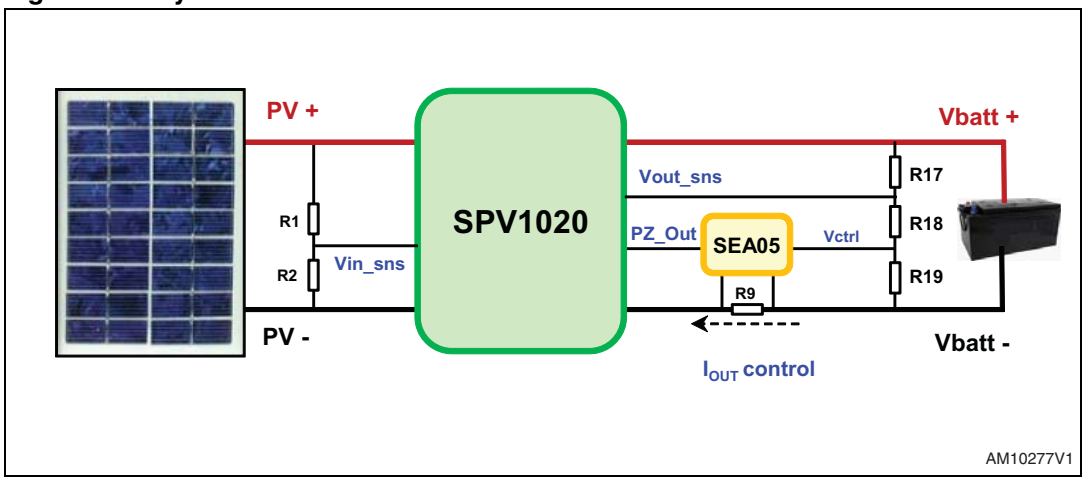
- Overtemperature protection
- Output overvoltage regulation
- Output overvoltage protection: input overcurrent protection
- Current balance
- Input MPPT settings.

For details regarding the above list of protection and functionalities, please refer to the SPV1020 datasheet and its basic application STEVAL-ISV009V1.

In addition to the above list, the STEVAL-ISV005V2 also implements an output overcurrent protection through the SEA05 IC (details in *Section 3.2* of this document).

Figure 7 offers a brief description of the architecture implemented.

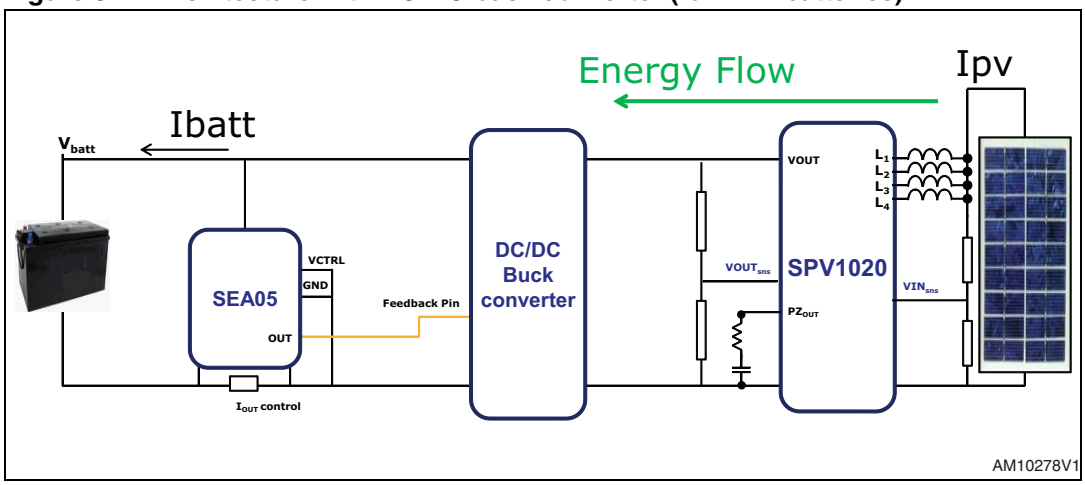
Figure 7. System architecture



The SPV1020 only implements an interleaved 4-boost converter, causing a voltage increase from input to output, so in order to charge a lead acid battery, it is mandatory to use a panel with Voc <= V_batt_min, just to keep a step-up voltage configuration.

If a 12 V battery charging is needed, it is necessary to add an additional buck stage to the system, in order to decrease the output voltage from STEVAL-ISV005V2 higher than Vbatt_min. A generic schematic may be that in the image below:

Figure 8. Architecture with DC-DC buck converter (for 12 V batteries)

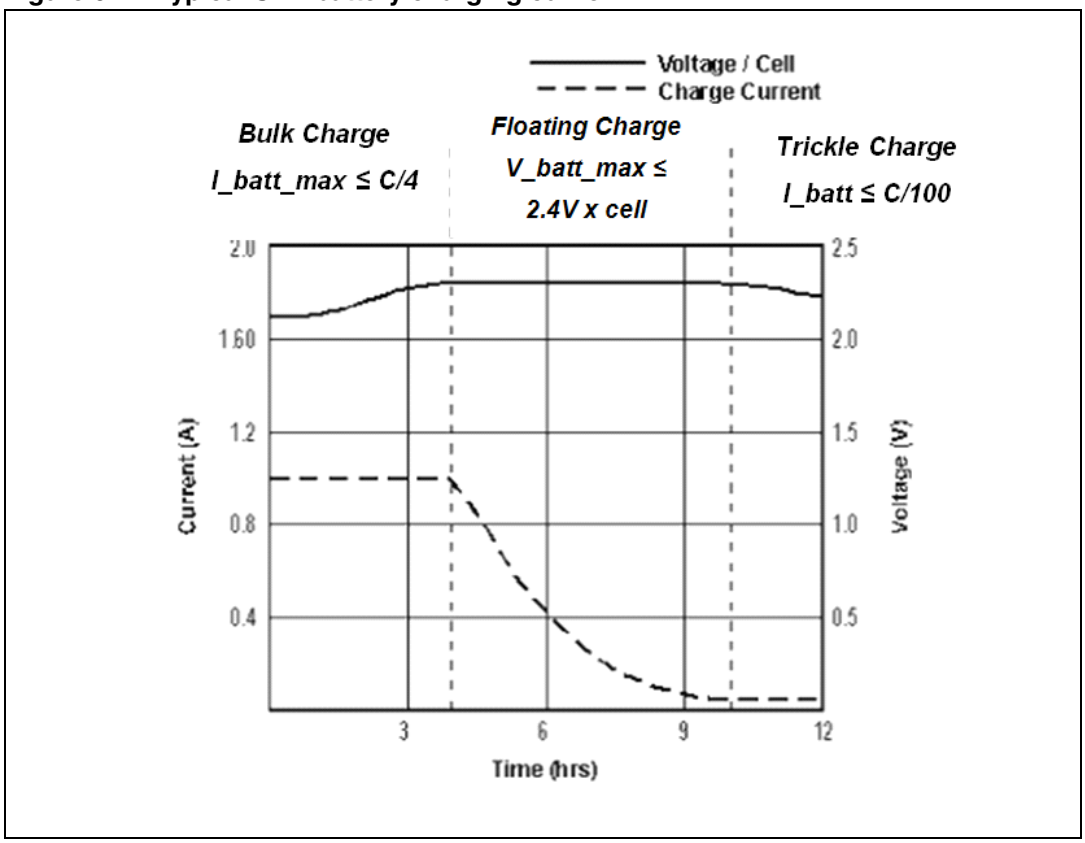


3 Charging a lead acid battery

A proper charging profile is important to guarantee a long battery lifetime.

The following figure shows the correct voltage/current charging profile (for a single cell only):

Figure 9. Typical SLA battery charging curve



Some of the charging constraints are given below and must be applied to all types of lead acid batteries.

1. Starting from a battery discharge, the maximum current must be lower than a value of C/4 (where C is the maximum battery capacity in Ampere hour [Ah]) →I_batt_max = 0.25 * C
2. In any charging step, the voltage applied must not be greater than the gassing voltage →V_batt_max = 2.4 V per cell
3. During the recharge and up to 100% of the previous discharge capacity, the current should be controlled to maintain a voltage lower than the gassing voltage →to reduce charge time, this voltage can be just below the gassing voltage.

So, to respect all the constraints mentioned above, the charging strategy used is a multi-voltage battery charging profile with:

- Constant current to perform a bulk charge, when the battery is charged using a current regulation to I_batt_max, up to 70% SOC, in about 4 hours, and the battery voltage slowly increases up to the nominal value (equal to 2 V per cell)
- Constant voltage to perform a floating charge, when the battery is charged using a voltage regulation to V_batt_max, up to the remaining 30% SOC, with a slow current decrease down to C/10 or C/100 values. This stage lasts 6 hours and is essential for the battery lifetime
- Constant current to perform a trickle charge, which compensates the self-discharge of the battery, even after it has been fully charged. Normally the charging current is less than C/100, and even if the battery is not completely saturated, the SLA can eventually lose its ability to accept a full charge and its performance is reduced.

3.1 Constant current – constant voltage control

In order to properly control the lead acid charging profile in terms of max. current during the bulk charge, and the max. voltage during the floating charge, the SEA05 IC has been used. The lead acid battery chemistry and physics behavior affect the charging strategy itself.

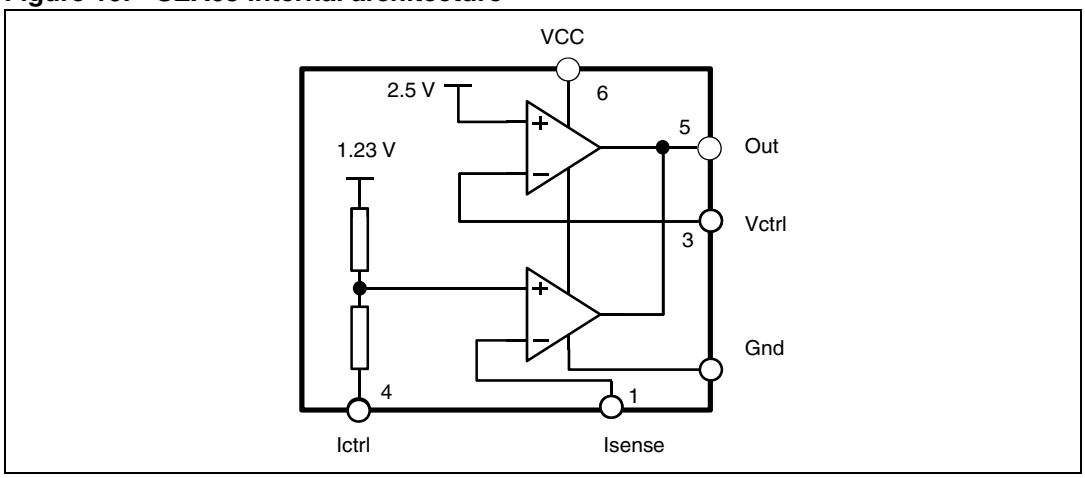
This occurs particularly during the last two steps of the lead acid charging profile:

- During the floating charge, the sink current decreases slowly because of the battery features keeping a constant voltage charge at the maximum value
- During the trickle charge (which is normally necessary just after the natural battery discharging), in order to keep the battery at a maximum SOC. In this case, no control acts, just to allow the energy flow directly from the panel towards the battery, without any constraints or voltage/current limitation.

3.2 SEA05 features

The SEA05 is a highly integrated solution for SMPS applications requiring a dual control loop to perform CV (constant voltage) and CC (constant current) regulation, implemented by two operational amplifiers, and a low-side current sensing circuit.

Figure 10. SEA05 internal architecture



The voltage reference, along with one op amp, is the core of the voltage control loop; the current sensing circuit and the other op amp make up the current control loop.

The external components needed to complete the two control loops are:

- A resistor divider that senses the output of the power supply and fixes the voltage regulation set-point at the specified value
- A sense resistor that feeds the current sensing circuit with a voltage proportional to the DC output current, setting the current regulation set-point (it must be adequately rated in terms of power dissipation)
- The frequency compensation components (R-C networks) for both loops.

Please refer to the SEA05 datasheet for further details.

3.3 Interaction between the SPV1020 and SEA05

The SPV1020 usually sets the duty cycle according to the MPPT algorithm except when even one of the protection or regulation thresholds is triggered.

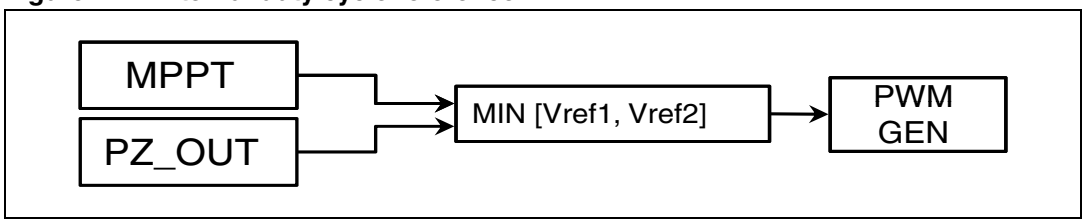
Regarding overvoltage regulation, if the voltage on the V_{out_sns} pin triggers 1 V, the output voltage feedback loop enters regulation, implying an upper limit to the duty cycle computed by the MPPT. The higher the voltage on the Vout_sns pin, the lower the upper limit on the duty cycle. The output voltage regulation acts in the range 1 V = V_{out_sns} < 1.04 V. If the 1.04 V threshold is triggered then the overvoltage protection forces the burst mode.

The stability of the regulation loop can be externally regulated by connecting a resistor and a capacitor (pole-zero compensation) between the PZ_OUT pin and SGND pin.

The PZ_OUT pin may have two different roles:

- To perform compensation loop to control the Vout_sns behavior
- To force an imposed duty cycle proportional to its voltage on the pin.

Figure 11. Internal duty cycle reference



The final duty cycle results from the minimum value between the one due to MPPT algorithm, and the second one imposed by the PZ_OUT external voltage.

The SEA05 provides two independent internal thresholds designed to separately control battery voltage and current control.

If one of the two thresholds is triggered, the common output is proportionally forced low, and the internal duty cycle imposed is proportional too.

Therefore, the output behavior of the SEA05 is perfectly compatible with the PZ_OUT pin of the SPV1020.

4 External component selection

The STEVAL-ISV005V2 is based on two ST key devices: the SPV1020 and SEA05.

In order to perform properly, both the SPV1020 and SEA05 require different application components whose selection depends on the electrical characteristics of the PV panel and of the battery.

The electrical characteristics of the PV panel limit the selection of the application components of the SPV1020. Please refer to the SPV1020 datasheet.

In order to properly define the application components for the SEA05, the user should simply define the following parameters:

- Output resistor partitioning (R7/R8) according to the SEA05 internal voltage control threshold, to control the maximum overvoltage battery protection
- Sensing resistor (Rsns: R9 and/or R10) in the PV-loop, to control the maximum overcurrent battery protection, according to the internal current threshold
- The PV panel must be selected in order to guarantee the SPV1020 functionality; and so, in order to respect the SPV1020 step-up conditions, the Voc of the PV panel must be lower than Vbat_min (voltage when the battery is deeply discharged).

The STEVAL-ISV005V2 application example has been developed for the following features:

SLA battery: V_{batt_nom} = 24 V & C = 4 Ah

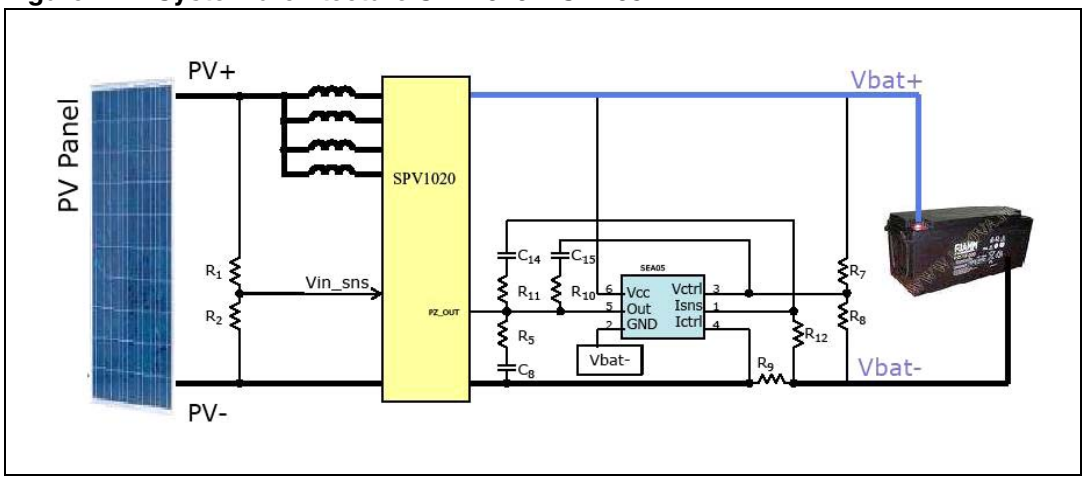
PV panel: V_{mp} = 18 V & V_{oc} = 20 V, I_{mp} = 1.6 A & I_{sc} = 2 A

So the SEA05 IC must limit at the following voltage and current:

V_{batt_max} = (24 * 1.2) V = 28.8 V

I_{batt_max} = (4/4) A = 1 A

Figure 12. System architecture SPV1020 + SEA05



4.1 Output current regulation

Output current regulation is implemented by the SEA05 current control loop.

The voltage threshold related to the current control is equal to 50 mV.

So to perform a current regulation, R_{sense} must be selected by the following equation:

$$R_{sense} \cdot I_{omax} = V_{csth}$$

For example, with I_{omax} = 1 A, V_{csth} = 50 mV, then R_{sense} = 50 mΩ

$$R_{sense} = \frac{V_{csth}}{I_{omax}}$$

Note that the R_{sense} resistor should be chosen taking into account the maximum power dissipation (Plim) through it during full load operation.

$$P_{lim} = V_{csth} \cdot I_{omax}$$

4.2 Battery voltage control

The voltage loop is controlled via a voltage divider R7, R8 directly inserted on the SPV1020 output voltage.

It is possible to choose their values using the following equations:

$$V_O = V_{csth} \cdot \frac{(R_1 + R_2)}{R_2}$$

and

$$R_1 = R_2 \cdot \frac{(V_O + V_{ctrl})}{V_{ctrl}}$$

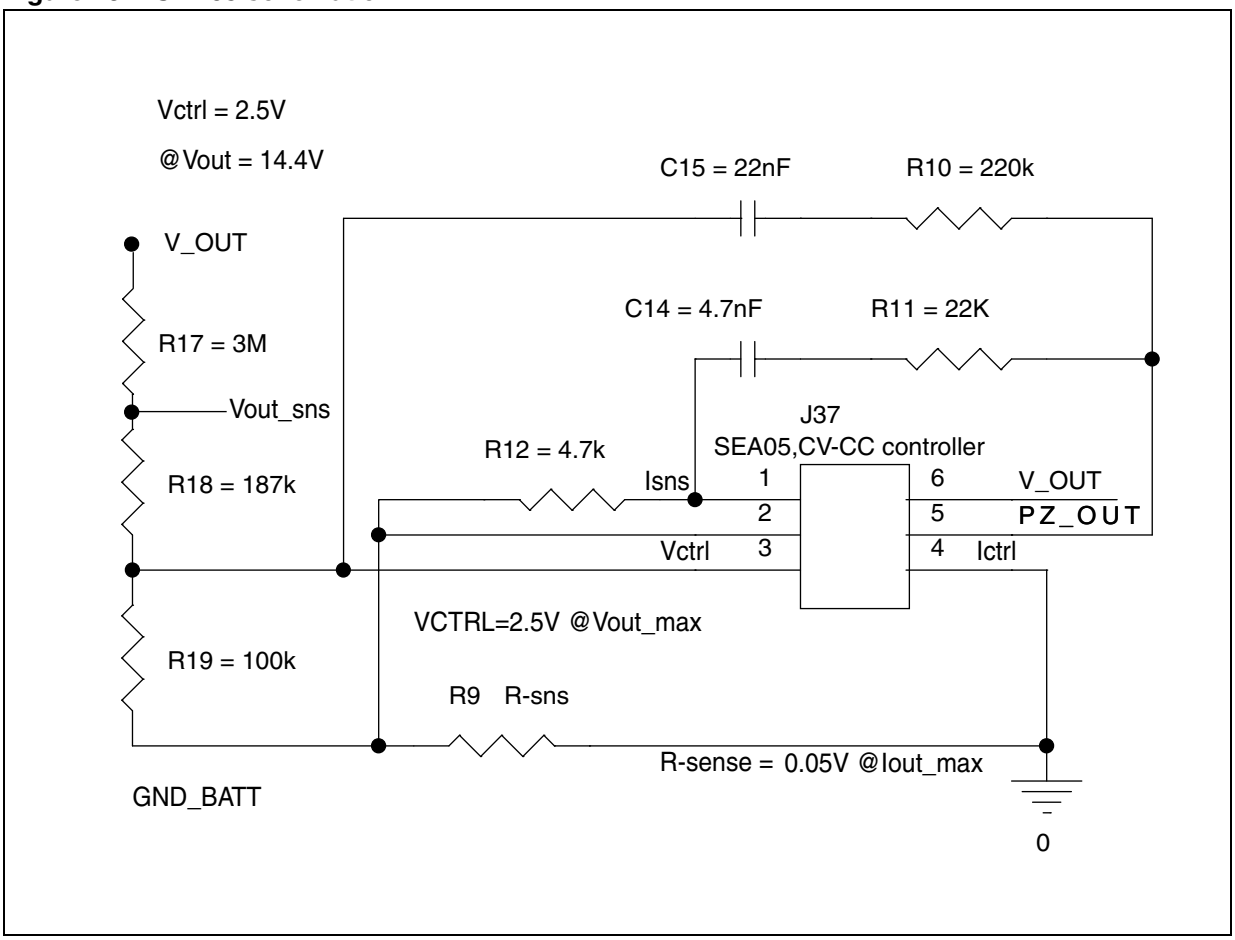
where V_O is the desired output voltage = V_batt_max.

In the case of V_batt_max = 28.8 V, with V_{ctrl} internally fixed by the SEA05 to 2.5 V, the values must be:

R7 = 2.7 MΩ ; R8 = 255 kΩ

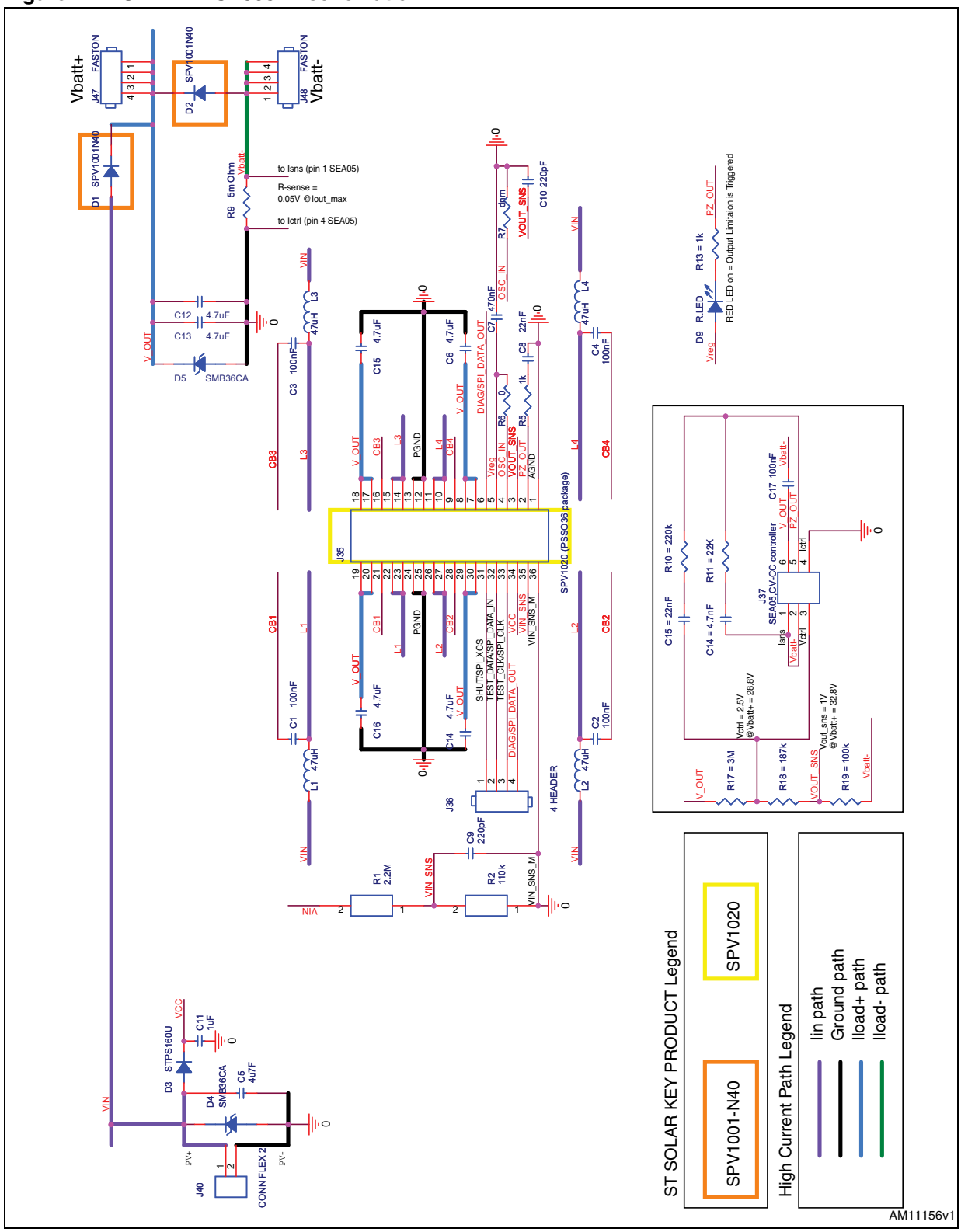
Here follows a schematic regarding SEA05 connections for the application example:

Figure 13. SEA05 schematic



5 STEVAL-ISV005V2 schematic

Figure 14. STEVAL-ISV005V2 schematic



6 Bill of materials

Table 1. Bill of materials

Item	Quantity	Reference	Part /value	Voltage current	Watt (mW)	Tecnology information	Package	Manufacturer	Manufacturer code	More Info
SPV1020 section										
1	1	J35					PSS036	ST	SPV1020	STM SUPPLY
2	4	C1, C2, C3,C4	100nF	16V 50V		X7R	0603	Murata	GRM188R71C104KA01D	Bootstrap capacitors
								TDK	C1608X7R1H104K X7R	
6	1	C7	470nF	25V		X7R	0603	Murata	GRM188R71E474KA12D	Internal reference voltage capacitor
								EPCOS	C1608X7R1C474K	
7	1	C8	22nF	25V		X7R	0603	Murata	GRM188R71C223KA01	Compensation capacitor
								EPCOS	C1608X7R1H223K	
8	2	C9, C10	220pF	50V		X7R	0603	Murata	GRM188R71E221KA01	Voltage sensing capacitor
								EPCOS	C1608C0G1H221J	
10	1	C11	1µF	50V		X7R	1206	Murata	GRM31MR71H105KA88	Input capacitor
								EPCOS	C3216X7R1H105K	
11	7	C5, C6, C12, C13, C14, C15, C16	4.7µF	50V		X7R	1210	Murata	GRM32ER71H475KA88L	Output capacitor
								EPCOS	C3225X7R1H475K	
18	2	D1, D2	Diode	15A, 60V			MLPD5x6	STM	SPV1001N40	Bypass diodes
20	1	D3	Diode	1A, 60V			SMB	STM	STPS160U	Noise filter on supply pin
21	2	D4, D5	Transil™	40V			SMB	STM	SMBJ36CA-TR	600W, 40V unidirectional protection Transil™

Table 1. Bill of materials (continued)

Item	Quantity	Reference	Part /value	Voltage current	Watt (mW)	Tecnology information	Package	Manufacturer	Manufacturer code	More Info
23	1	D9(1)	TH RED LED	1.8V, 2mA			TH	AVAGO TECH.	HLMP-1700	Output limitation led control
24	1	R1	2.2MΩ		125		0603	MULTICOMP	MCHP03W8F2204T5E	Input voltage pertitioning resistor
25	1	R2	110kΩ		125		0603	VISHAY DALE	CRCW0603110KFKEA	Input voltage pertitioning resistor
								MULTICOMP	MC0603SAF1103T5E	
26	1	R5	1kΩ		100		0603	YAGEO	RC0603FR-101KL	Compensation resistor
27	1	R13(1)	1.5kΩ		100		0603	YAGEO	RC0603FR-071K5L	LED polarization resistor
28	1	R6	0Ω		100		0603	YAGEO	RC0603FR-070RL	Pull up resistor(2)
29	0	R7 (optional)	Depending on desired Fsw			DNM	0603			Oscllator resistor (1)
29	4	L1, L2, L3, L4	47µH					EPCOS(3)	B82477G4473M	Phase x (x=1..4) inductors
								Coilcraft	MSS1278T-473ML	
								CYNTEC	PIMB136T-470MS-11	
								Murata	49470SC	
33	1	J36	4pin conn.			Pitch-2.54mm	TRH	Phoenix Contact	1723672	
34	2	J47, J48	Faston conn.				TH			
36	1	J40	2pin conn.			Pitch-6.35mm	TH	Phoenix Contact	1714955	
SEA05 section										
37	1	J37	SEA05				SOT23-6L	STM	SEA05TR	CV-CC controller

Table 1. Bill of materials (continued)

Item	Quantity	Reference	Part /value	Voltage current	Watt (mW)	Tecnology information	Package	Manufacturer	Manufacturer code	More Info
38	1	R9	5mΩ (4)	50ppm/°C	2010	Welwyn	ULR1S-R005FT2	Farnell: 1469782	Current sensing resistor	
39	1	R10	220kΩ		100		0603	YAGEO (PHYCOMP)	RC0603FR-07220KL	Voltage comp. loop resistor
40	1	R11	22kΩ		100		0603	YAGEO (PHYCOMP)	RC0603FR-0722KL	Current comp. loop resistor
41	1	R17	3MΩ		100		0603	VISHAY DRALORIC	CRCW06033M00FKEA	output voltage part. resistor(5)
42	1	R18	187kΩ		100		0603	VISHAY DRALORIC	CRCW0603187KFKEA	
43	1	R19	100kΩ		100		0603	VISHAY DRALORIC	CRCW0603100KFKEA	
44	1	C14	4.7nF	16V		X7R	0603	Murata	GRM188R71C472KA01B	Current comp. loop capacitor
								MULTICOMP	MCCA001139	
45	1	C15	22nF	16V		X7R	0603	Murata	GRM188R71C223KA01	Voltage comp. loop capacitor
								MULTICOMP	MCCA001143	
46	1	C17	100nF	16V 50V		X7R	0603	Murata	GRM188R71C104KA01D	Output filter
								TDK	C1608X7R1H104K X7R	

1. Do not mounted (DNM).
2. R6 must be removed if R7 is soldered.
3. Better performances can be obtained using part number B82477G4473M003 (DCR = 52mΩ)
4. Default value to sense 50 mV @10 A max.
5. Two threshold is suited: # 2.5 V for SEA05: R17=3MΩ, R18+R19=287kΩ => Vmax=28.8 V # 1V for SPV1020: R17+R18=3.187 , R19=100kΩ => Vmax= 35 V.

7 Layout guidelines

PCB layout is very important, especially for the SPV1020, in order to minimize noise, high frequency resonance problems, and electromagnetic interference.

Paths between each inductor and the relative pin must be designed with the same resistance. Different resistance between the four branches can be the root cause of unbalanced currents flowing between the four branches. Unbalanced currents can imply damage and a bad tracking of the MPPT.

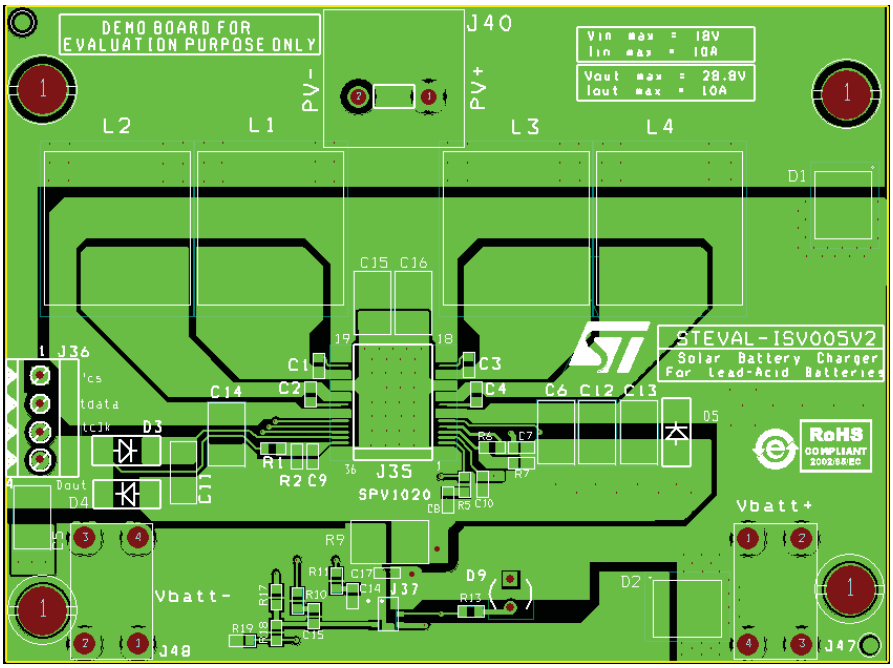
It is essential to keep the paths as small as possible where the high switching current circulates, to reduce peak voltages, radiation and resonance problems.

Large traces for high current paths and an extended ground plane under the metal slug of the package help reduce noise and heat dissipation, and furthermore, increase the efficiency. Depending on the maximum power of the application, two or more ground plane layers may be required, and in this case thermal vias must connect the ground plane layers. The number of layers, their thickness and number of thermal vias, affect the thermal resistance (R_{th}) of the SPV1020: for a proper design according to the power of the specific application it is suggested to refer to the TN0054 technical note.

The boost capacitors, output and input capacitors, must be placed as close as possible to the pins of the IC. Output capacitance must be shared in at least four capacitors, each one connected to the four V_{out} pins of the SPV1020 IC.

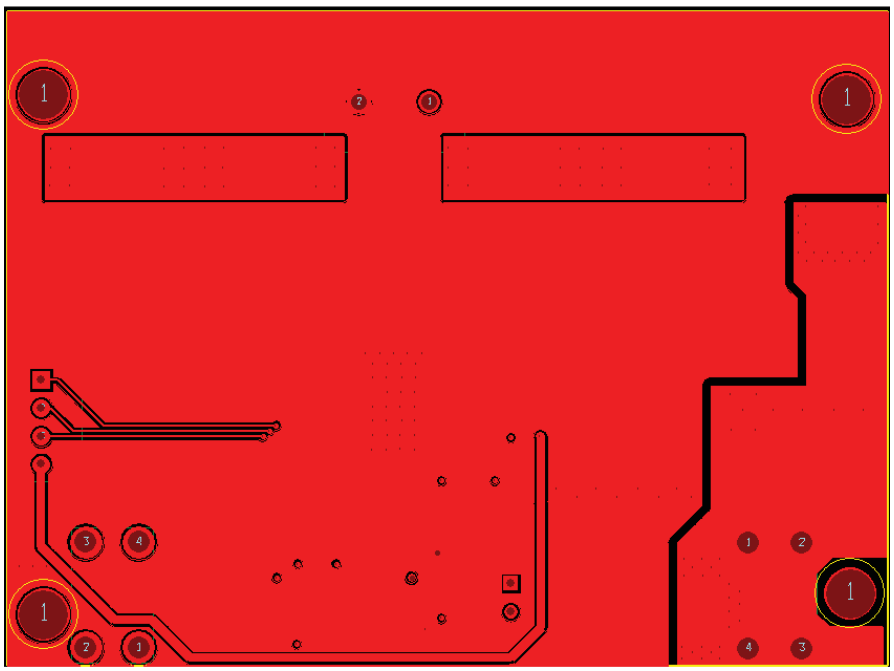
The external resistor dividers, if used, should be as close as possible to the V_{in_sns} and V_{out_sns} pins of the device, and as far as possible from the high current circulating paths, to avoid pick-up noise.

Figure 15. STEVAL-ISV005V2 (top view)



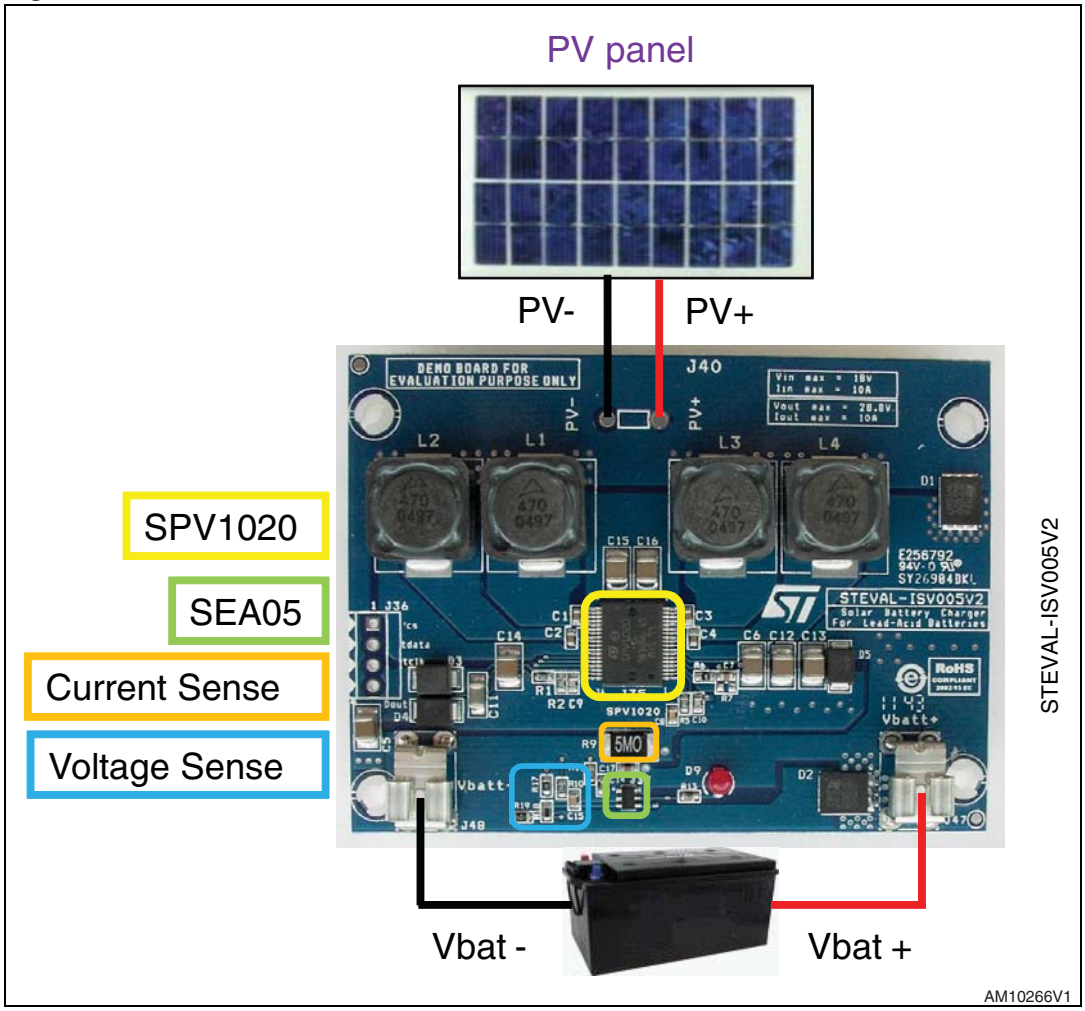
AM10267V1

Figure 16. STEVAL-ISV005V2 (bottom view)



8 Application connection example

Figure 17. STEVAL-ISV005V2 board connection



9 Experimental results

In order to test all the functionalities regarding the MPP tracking, and battery charging capability, the following parts are used:

- Two SLA batteries (12 V, 4 Ah), connected in series

Figure 18. SLA battery (12 V, 4 Ah)

- A solar array simulator (SAS), that allows total emulation of a PV panel electrical behavior

Figure 19. Solar array simulator (SAS)

- Four multimeters, to check the voltage and current values in the input and the output of the STEVAL-ISV005V2, to evaluate the MPP tracking efficiency, such as the power efficiency, and obviously to trace the battery charging curve.

Figure 20. SLA battery charging profile (24 V, 4 Ah)

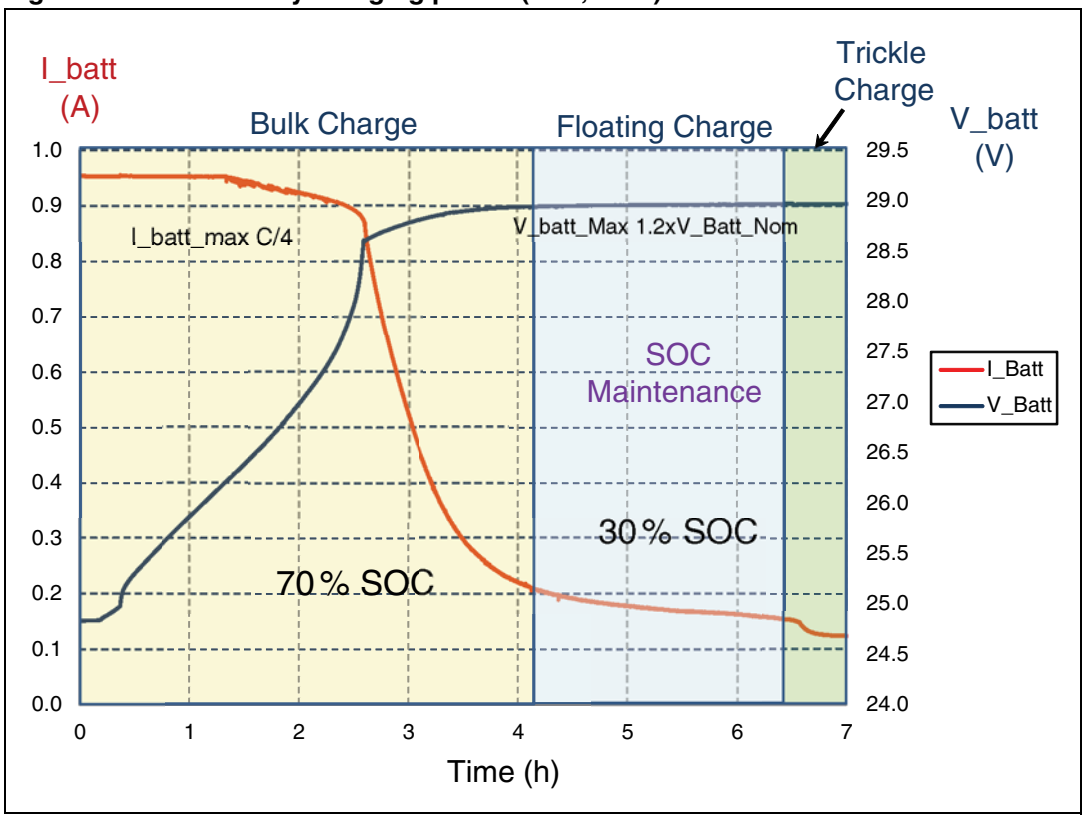


Figure 21. SLA battery charging profile (12 V, 12 Ah)

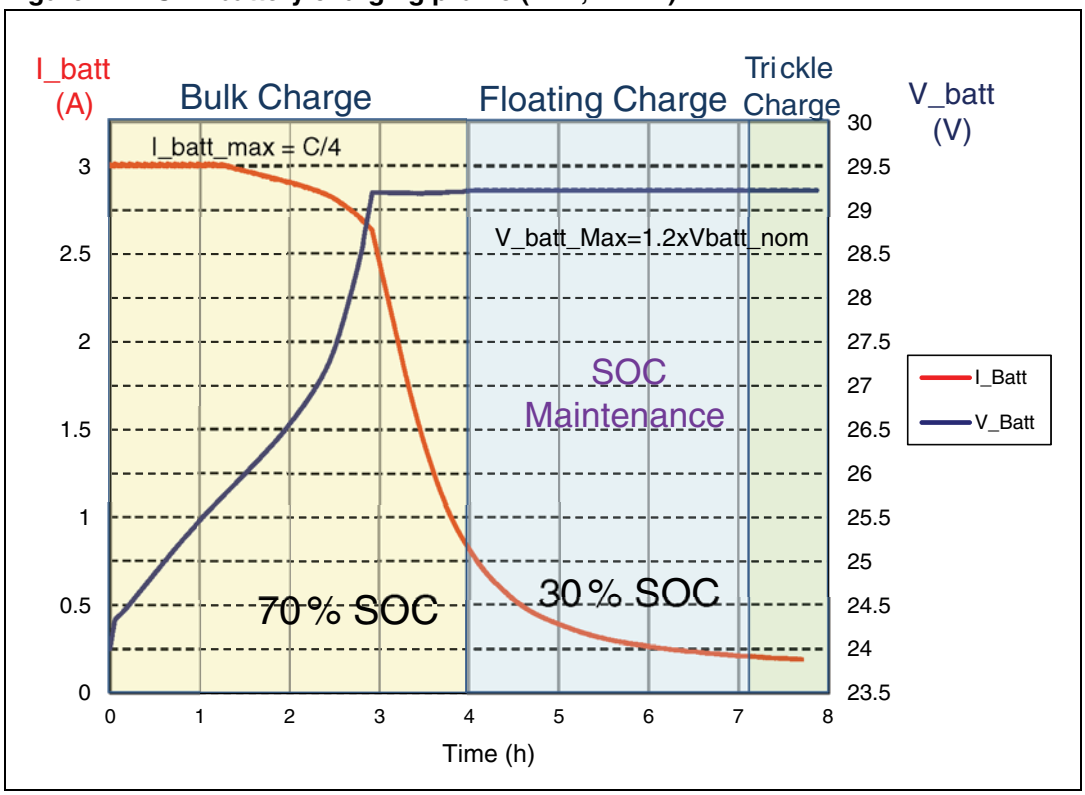
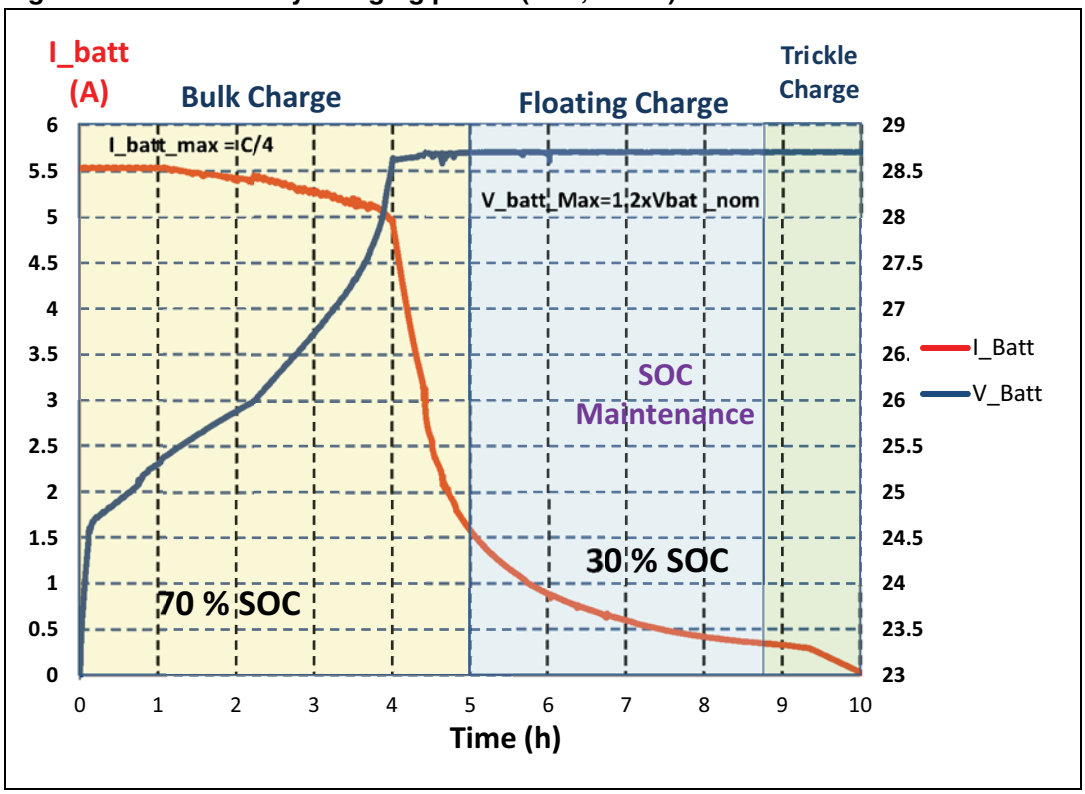


Figure 22. SLA battery charging profile (24 V, 24 Ah)



10 Conclusion

In a standalone PV system, an SPV1020 with MPPT and step-up IL4 embedded architecture, used in an application field together with the constant voltage - constant current SEA05, allows the proper charging of an SLA battery, without any damage or lifetime reduction.

The architecture, compared with a similar one implemented with a microcontroller, external discrete components and IL4 step-up, performs better in terms of power and MPPT efficiency.

Furthermore, the distributed approach, directly applied on the panel, allows the management of any power reduction due to shadow, clouds, etc.; all features which are unsuitable to centralized architecture.

The proposed solution is cost effective when compared with other systems, because of its MPPT algorithm, and IL4 architecture, which are fully integrated inside the SPV1020.

11 References

- SPV1020 datasheet
- SEA05 datasheet
- TN0054 technical note
- E. Koutroulis, K. Kalaitzakis, “A Novel Battery Charging Regulation System for Photovoltaic Applications” IEEE Proc.-Electr. Power Appl., 2004, vol. 151 n.2,.

12 Revision history

Table 2. Document revision history

Date	Revision	Changes
15-Feb-2012	1	Initial release.
11-May-2012	2	Minor text changes in *Section 2: Optimizing the energy from the panel*. Updated BOM list *Table 2* item 29.