

N-channel 30 V, 0.0048 Ω 21 A PowerFLAT™ 5x6
STripFET™ V Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STL66N3LLH5	30 V	<0.0058 Ω	21 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



Applications

- Switching applications
- Automotive

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

Figure 1. Internal schematic diagram

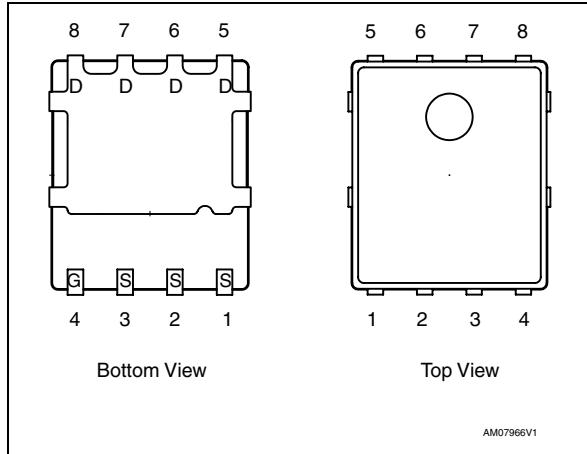


Table 1. Device summary

Order code	Marking	Package	Packaging
STL66N3LLH5	66N3LLH5	PowerFLAT™ 5x6	Tape and reel

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Table 8. Source drain diode

$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19 \text{ A}, V_{GS}=0$	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 19 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD}=25 \text{ V}, T_j=150 \text{ }^\circ\text{C}$	-	25 17.5 1.4	ns nC A	

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

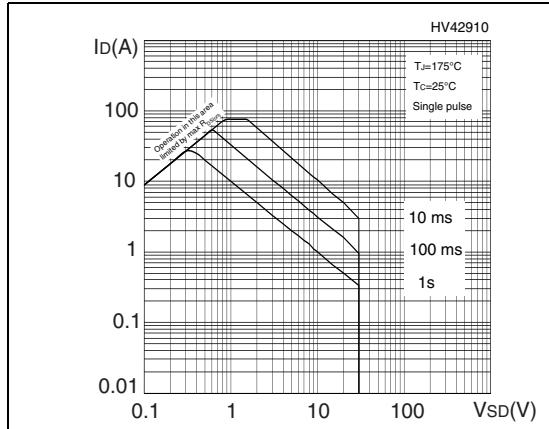


Figure 3. Thermal impedance

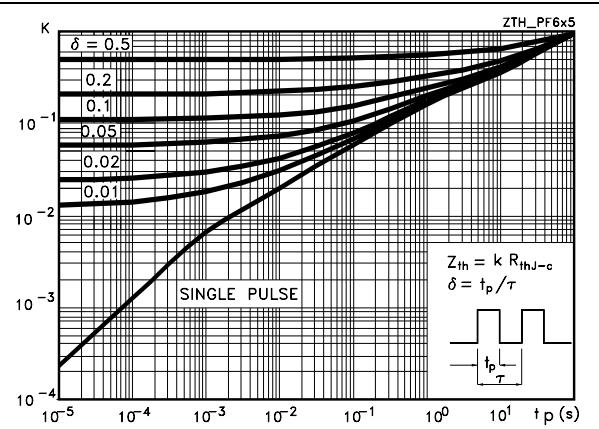


Figure 4. Output characteristics

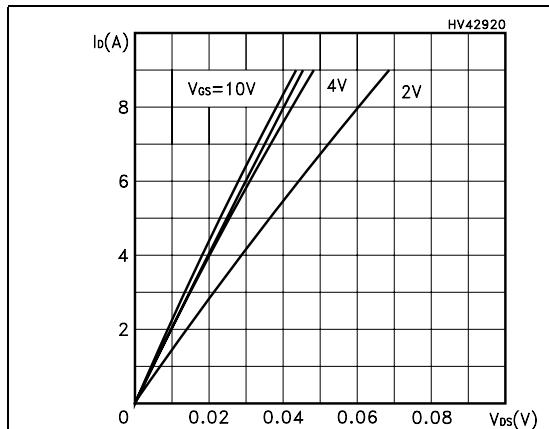


Figure 5. Transfer characteristics

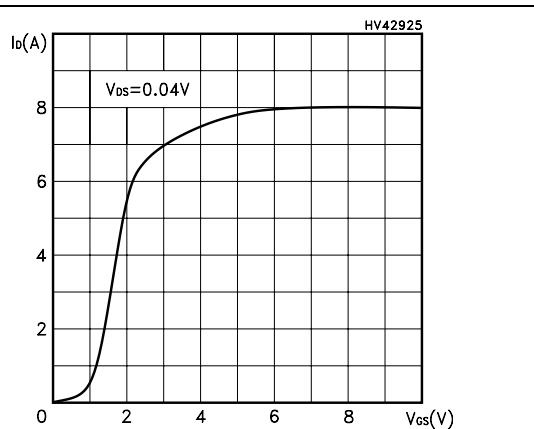


Figure 6. Normalized B_{VDSS} vs temperature

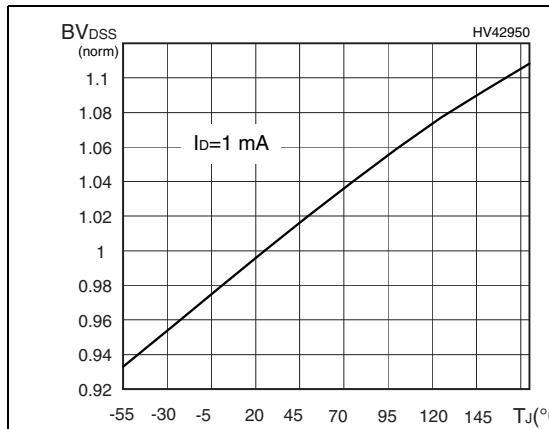


Figure 7. Static drain-source on resistance

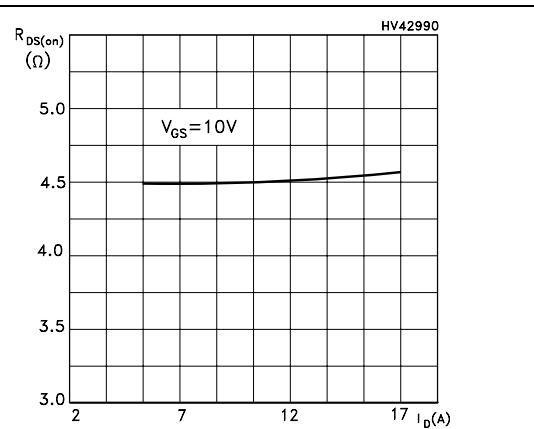
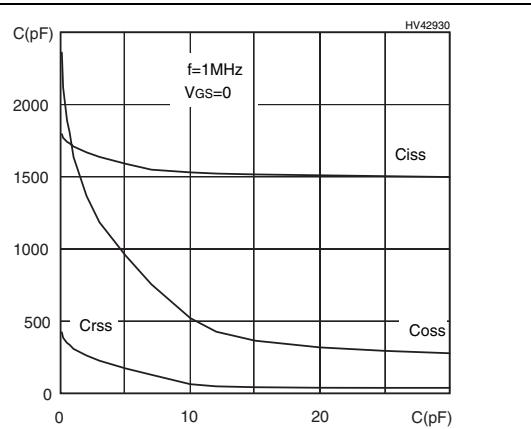
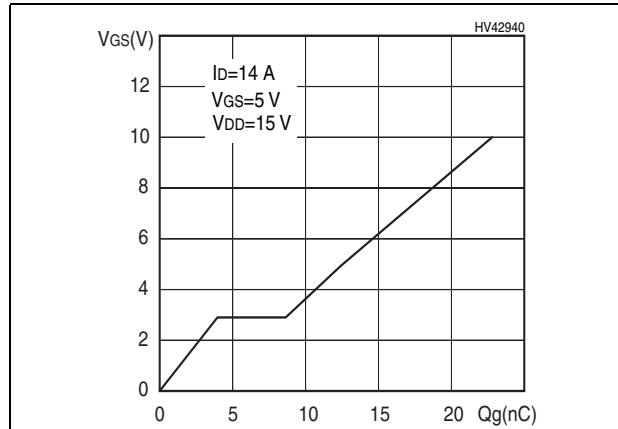
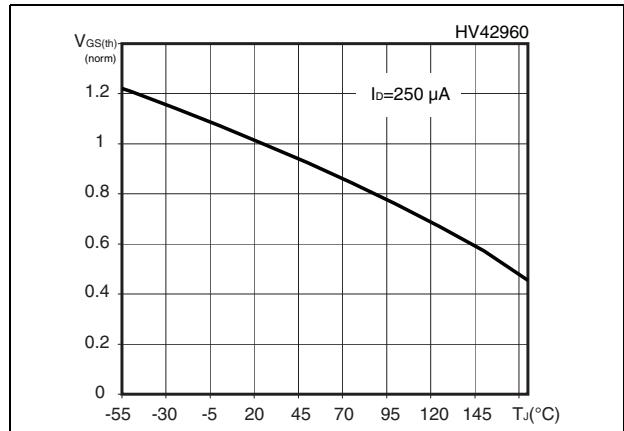
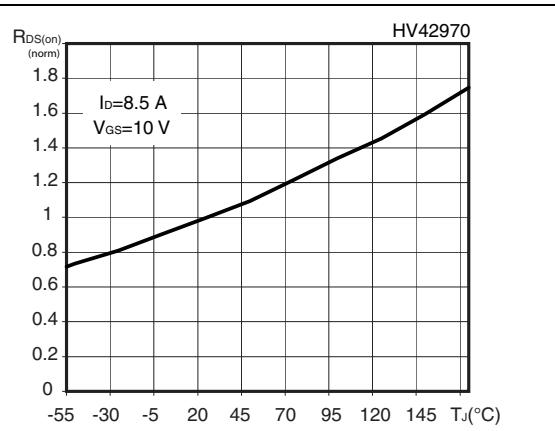
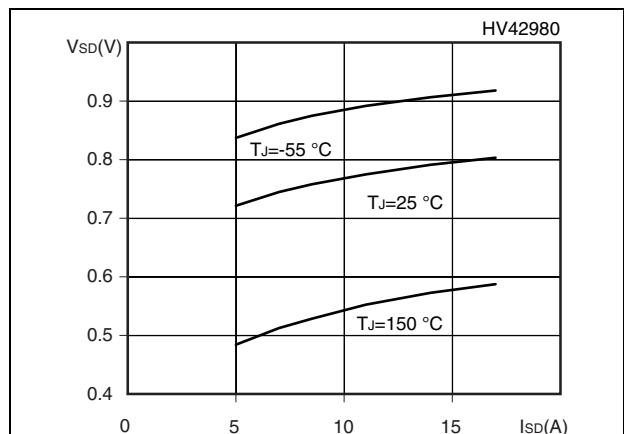


Figure 8. Gate charge vs gate-source voltage**Figure 10. Normalized gate threshold voltage vs temperature****Figure 11. Normalized on resistance vs temperature****Figure 12. Source-drain diode forward characteristics**

3 Test circuits

Figure 13. Switching times test circuit for resistive load

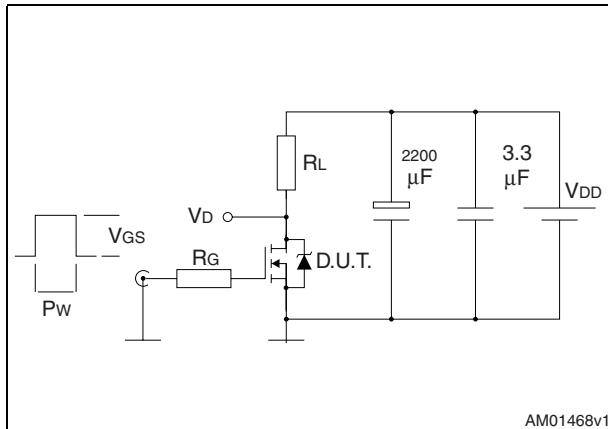


Figure 14. Gate charge test circuit

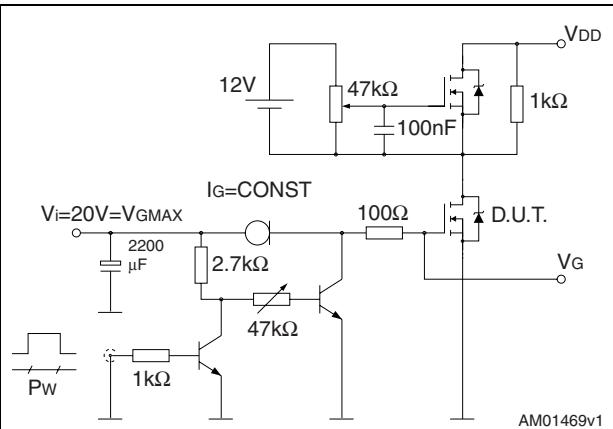


Figure 15. Test circuit for inductive load switching and diode recovery times

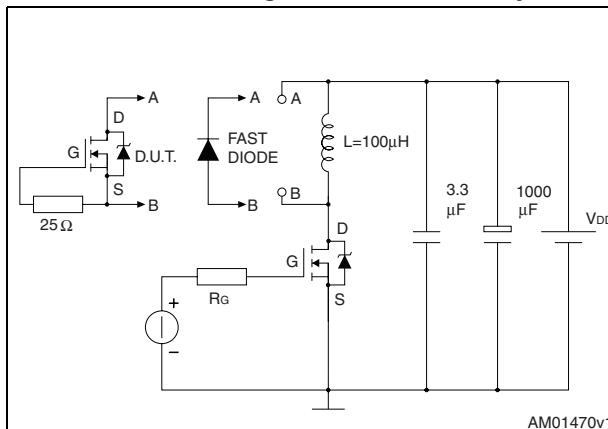


Figure 16. Unclamped inductive load test circuit

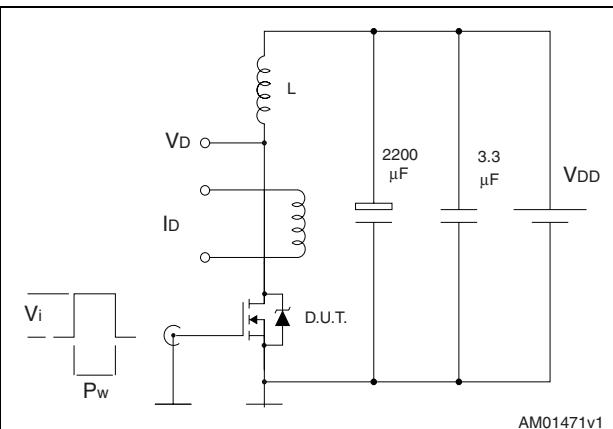


Figure 17. Unclamped inductive waveform

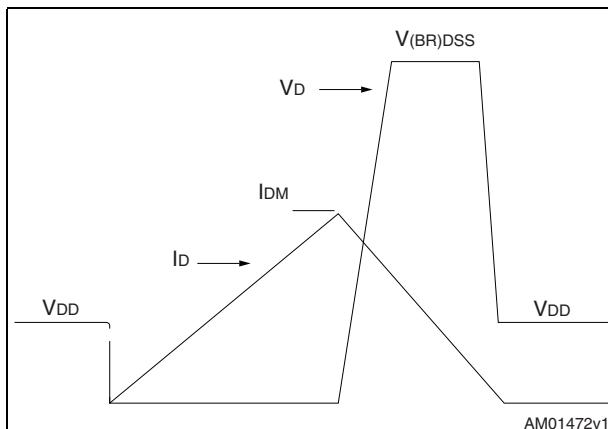
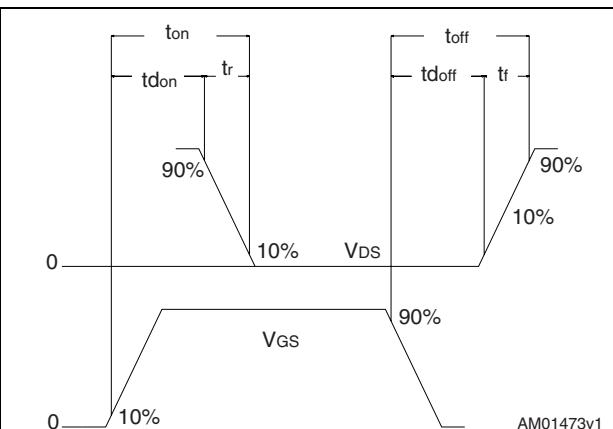


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

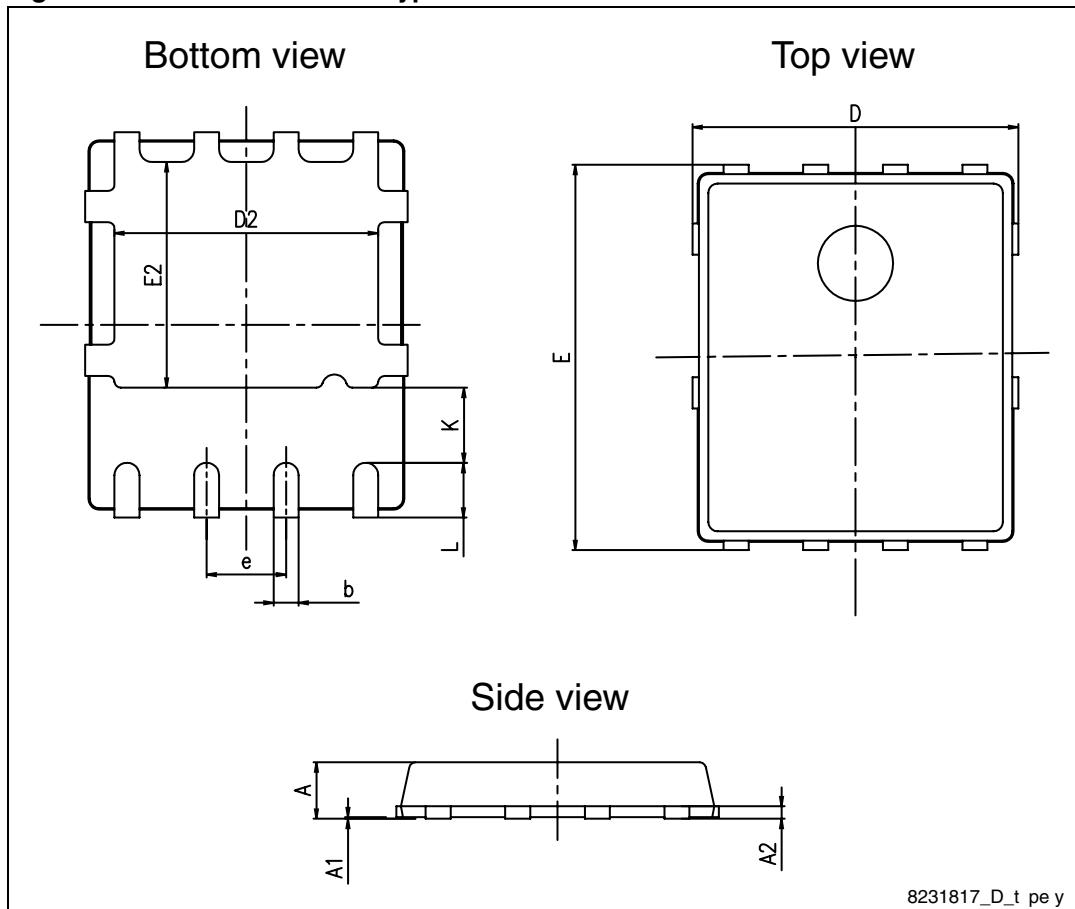
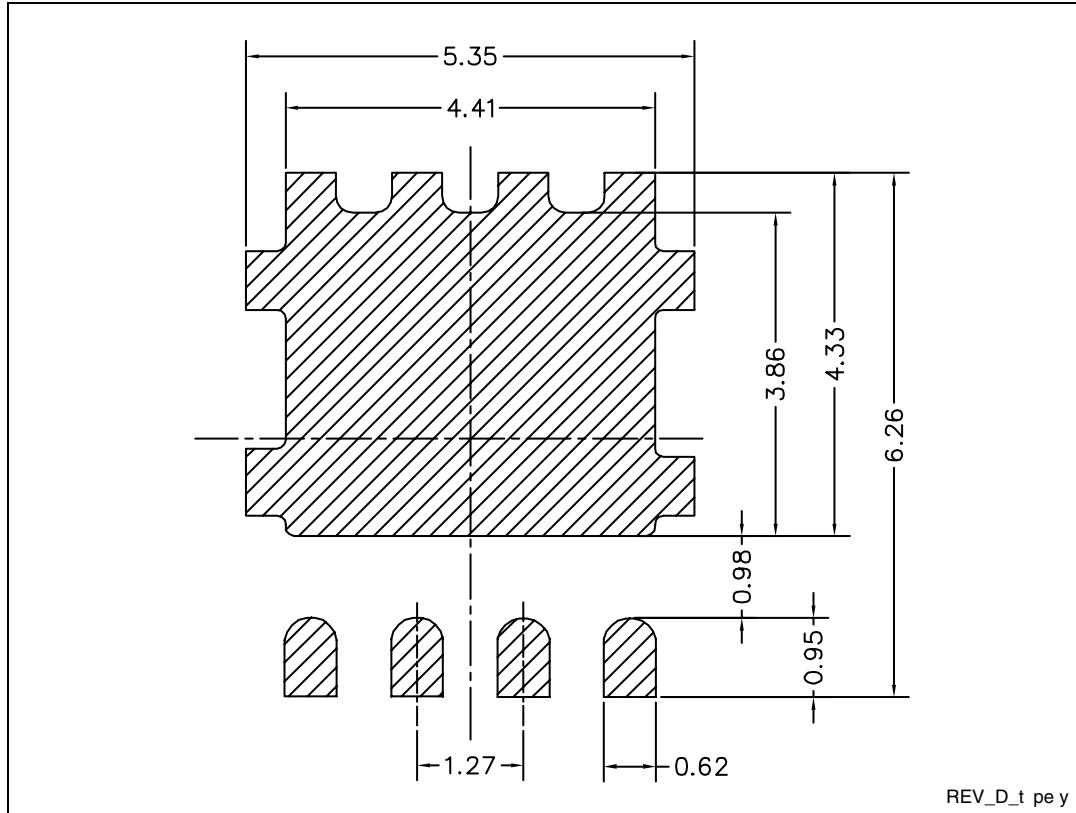


Figure 20. PowerFLAT™ 5x6 recommended footprint type S-C (dimensions in mm)

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-Oct-2011	1	First release.

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