

P-channel 30 V, 0.024 Ω typ., 12 A, STripFET™ VI DeepGATE™ Power MOSFET in a DPAK package

Datasheet - production data

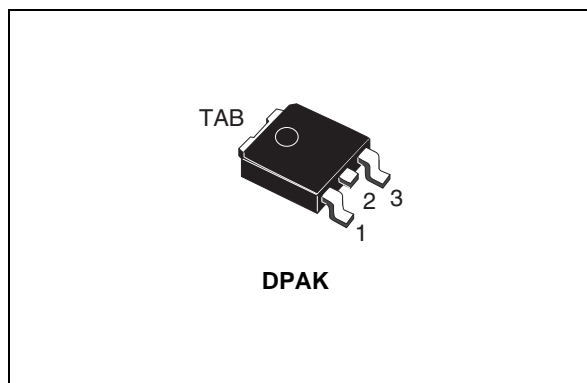
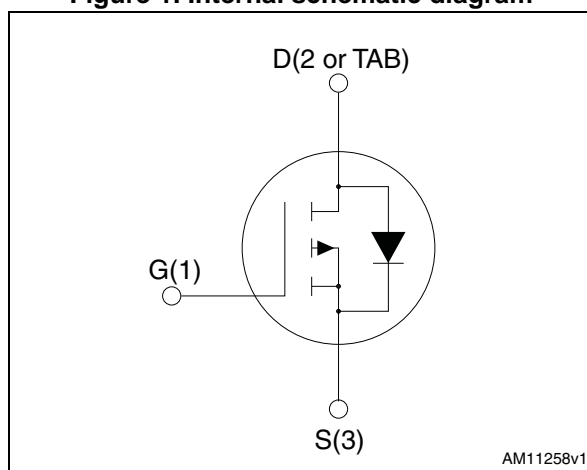


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max	I _D	P _{TOT}
STD26P3LLH6	30 V	0.030 Ω ⁽¹⁾	12 A	40 W

1. @ V_{GS} = 10 V

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate input resistance

Applications

- Switching applications
- LCC converters, resonant converters

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages

Table 1. Device summary

Order code	Marking	Package	Packaging
STD26P3LLH6	26P3LLH6	DPAK	Tape and reel

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	12	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8.5	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	48	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	40	W
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature	175	$^\circ\text{C}$

1. Limited by wire bonding.

2. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.75	$^\circ\text{C/W}$

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 30\text{ V}$, ($V_{GS} = 0$)			1	μA
		$V_{DS} = 30\text{ V}$, $T_c = 125\text{ }^{\circ}\text{C}$			10	μA
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, ($V_{DS} = 0$)			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$		0.024	0.03	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 6\text{ A}$		0.038	0.045	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1450	-	pF
C_{oss}	Output capacitance		-	178	-	pF
C_{rss}	Reverse transfer capacitance		-	120	-	pF
Q_g	Total gate charge	$V_{DD} = 24\text{ V}$, $I_D = 12\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see Figure 14)	-	12	-	nC
Q_{gs}	Gate-source charge		-	4.4	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ gate bias Bias = 0 test signal level = 20 mV open drain	-	1.8	-	Ω

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 24\text{ V}$, $I_D = 1.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	15	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	21	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 16\text{ V}$ (see Figure 15)	-	15		ns
Q_{rr}	Reverse recovery charge		-	6.5		nC
I_{RRM}	Reverse recovery current		-	0.9		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

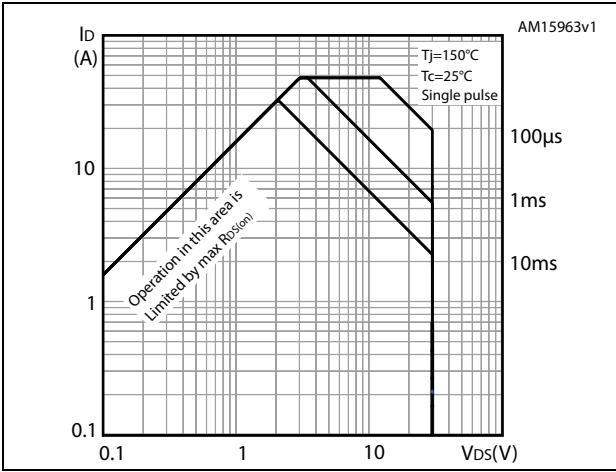


Figure 3. Thermal impedance

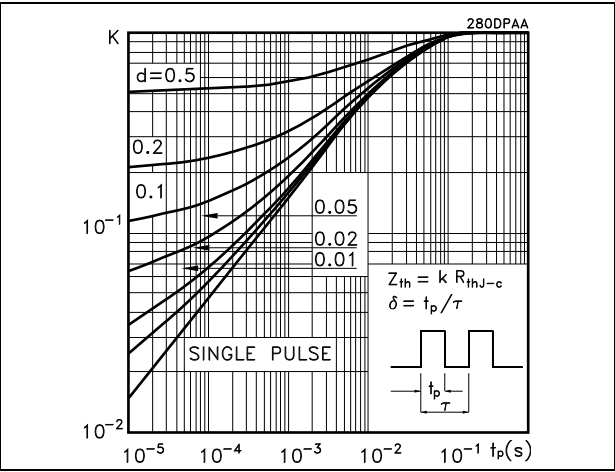


Figure 4. Output characteristics

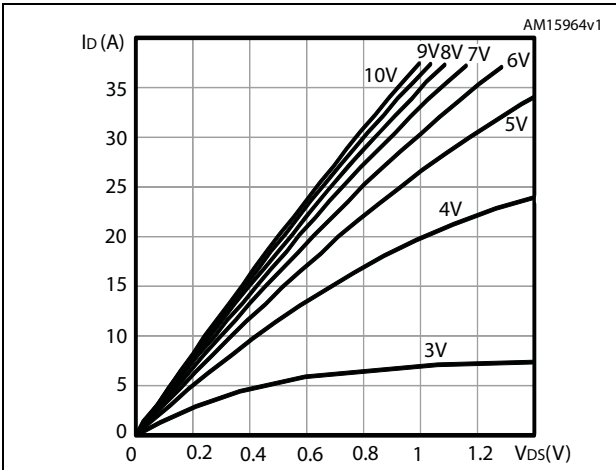


Figure 5. Transfer characteristics

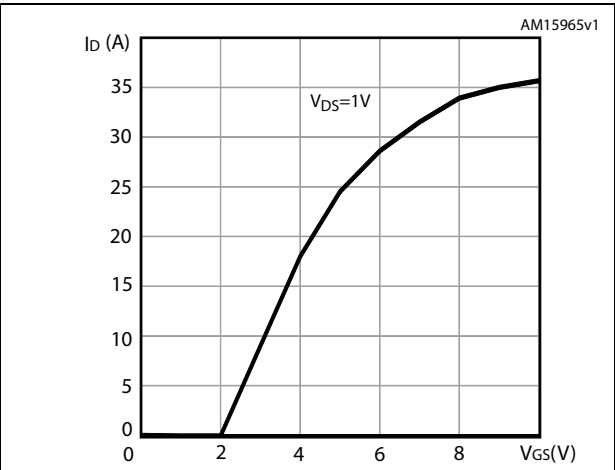


Figure 6. Gate charge vs gate-source voltage

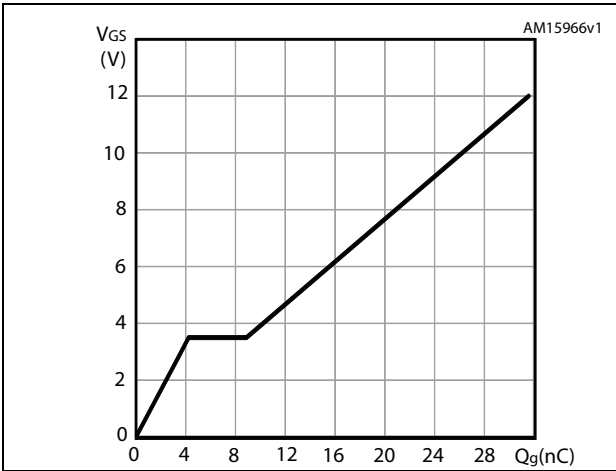


Figure 7. Static drain-source on-resistance

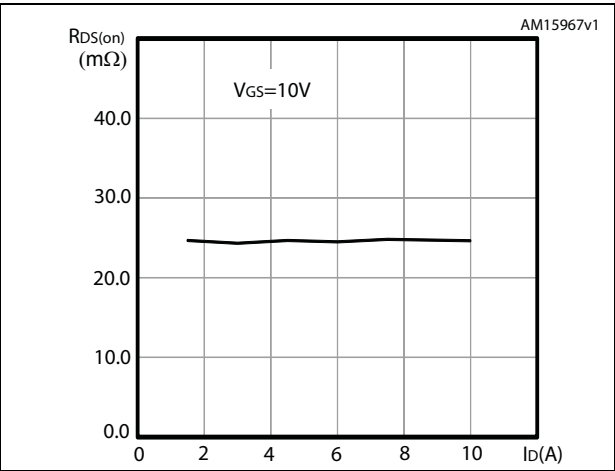


Figure 8. Capacitance variations

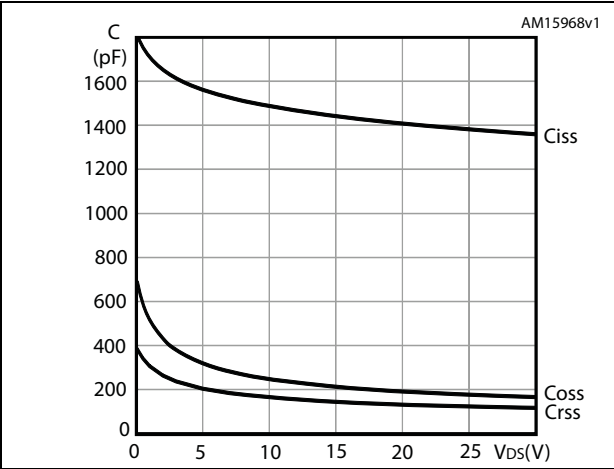


Figure 9. Normalized gate threshold voltage vs temperature

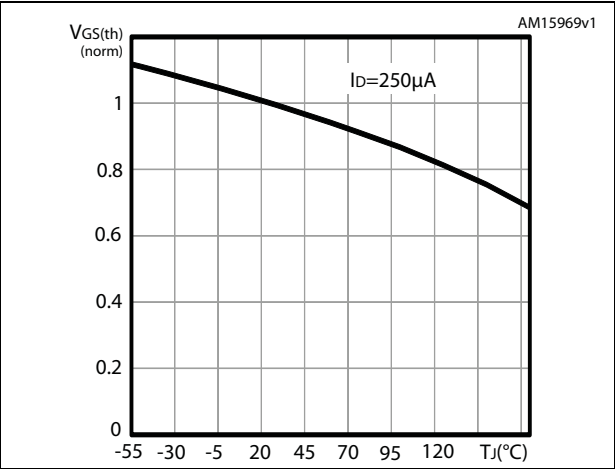


Figure 10. Normalized on-resistance vs temperature

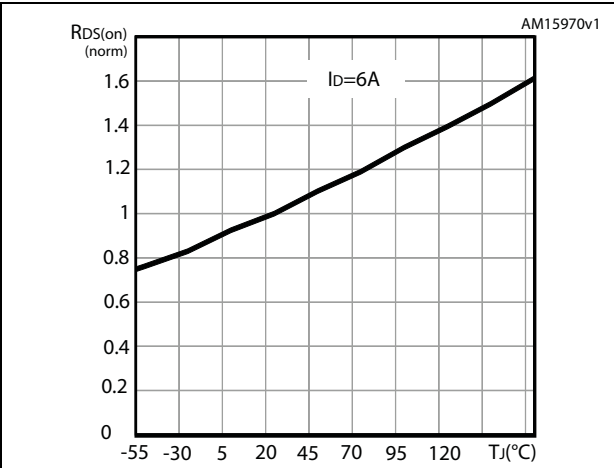


Figure 11. Normalized VDS vs temperature

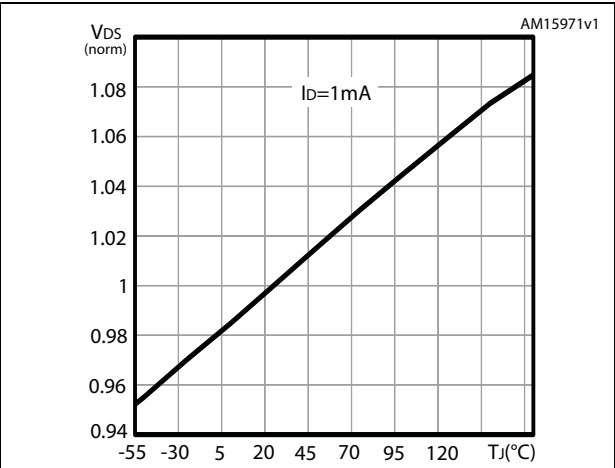
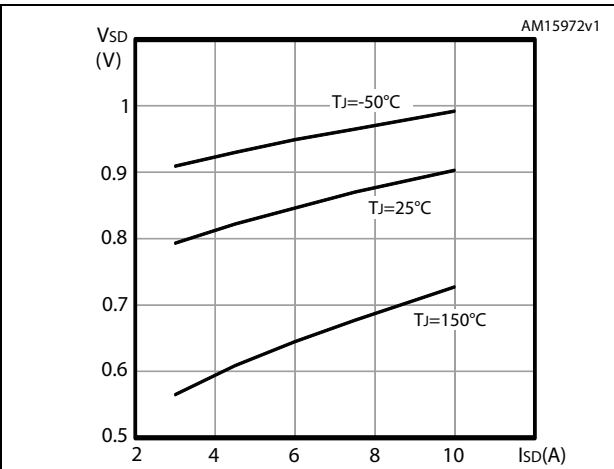


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

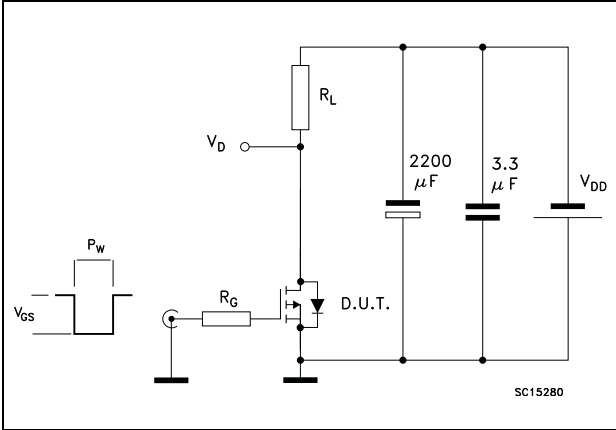


Figure 14. Gate charge test circuit

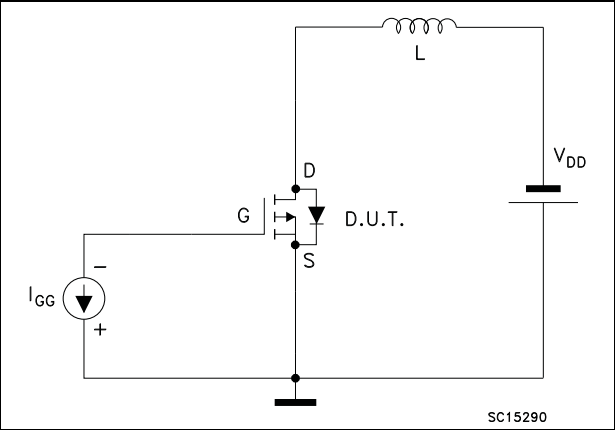
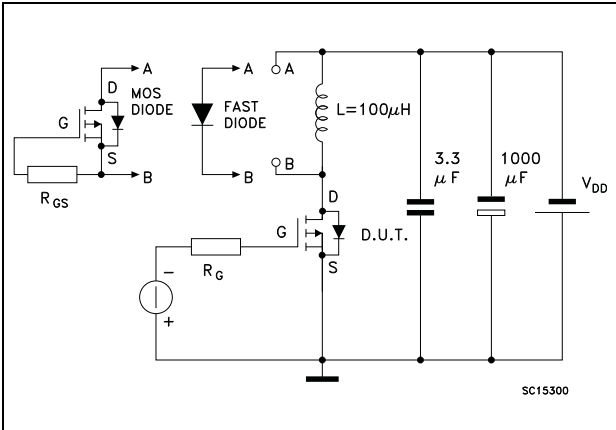


Figure 15. Test circuit for diode recovery behavior



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 16. DPAK (TO-252) drawing

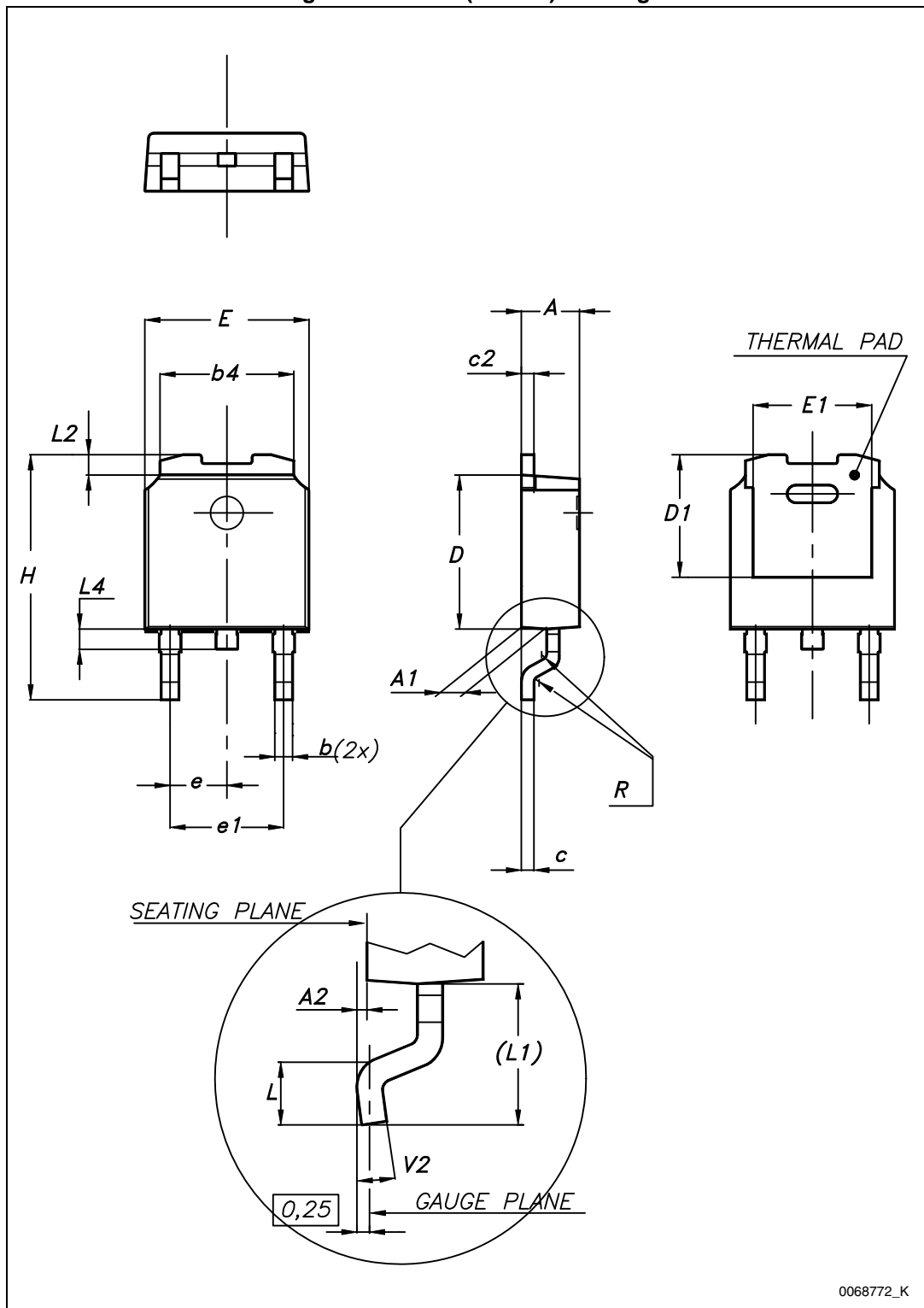
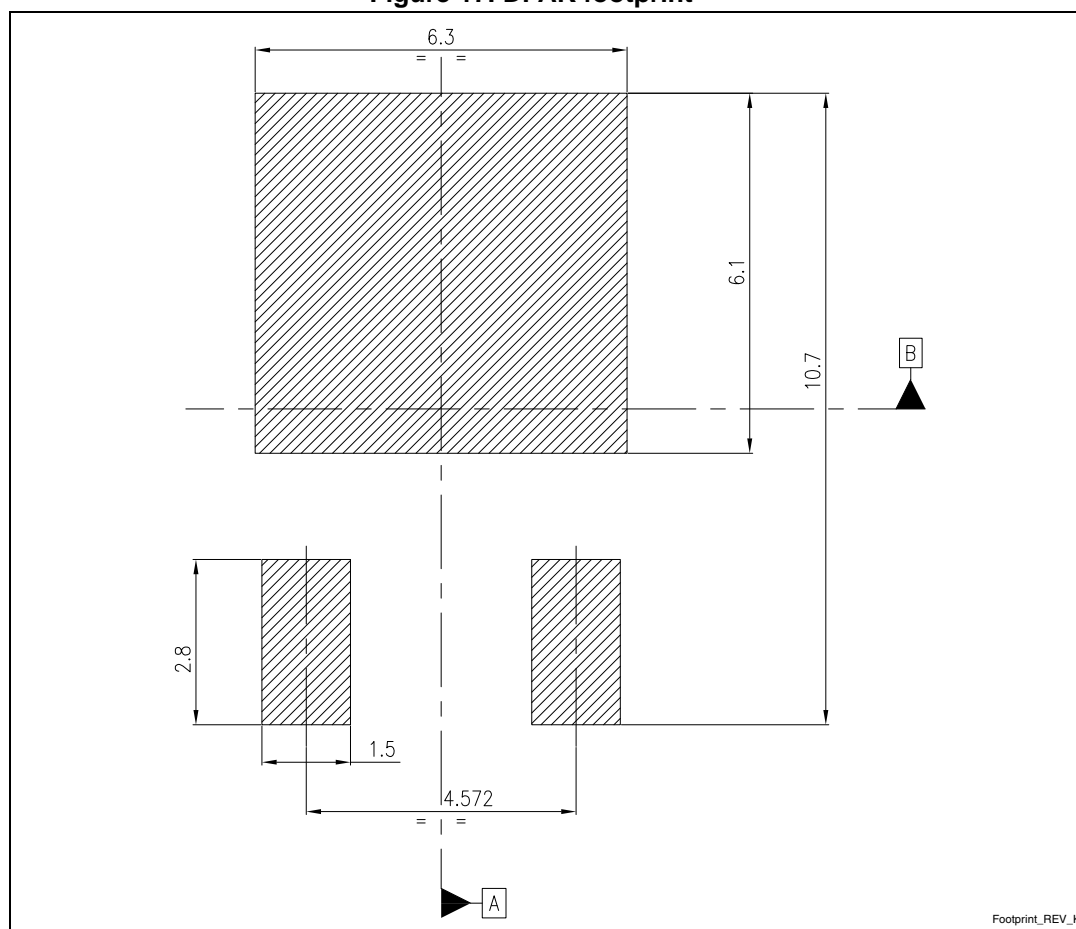


Figure 17. DPAK footprint (a)



a. All dimensions are in millimeters

5 Packaging mechanical data

Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 18. Tape for DPAK (TO-252)

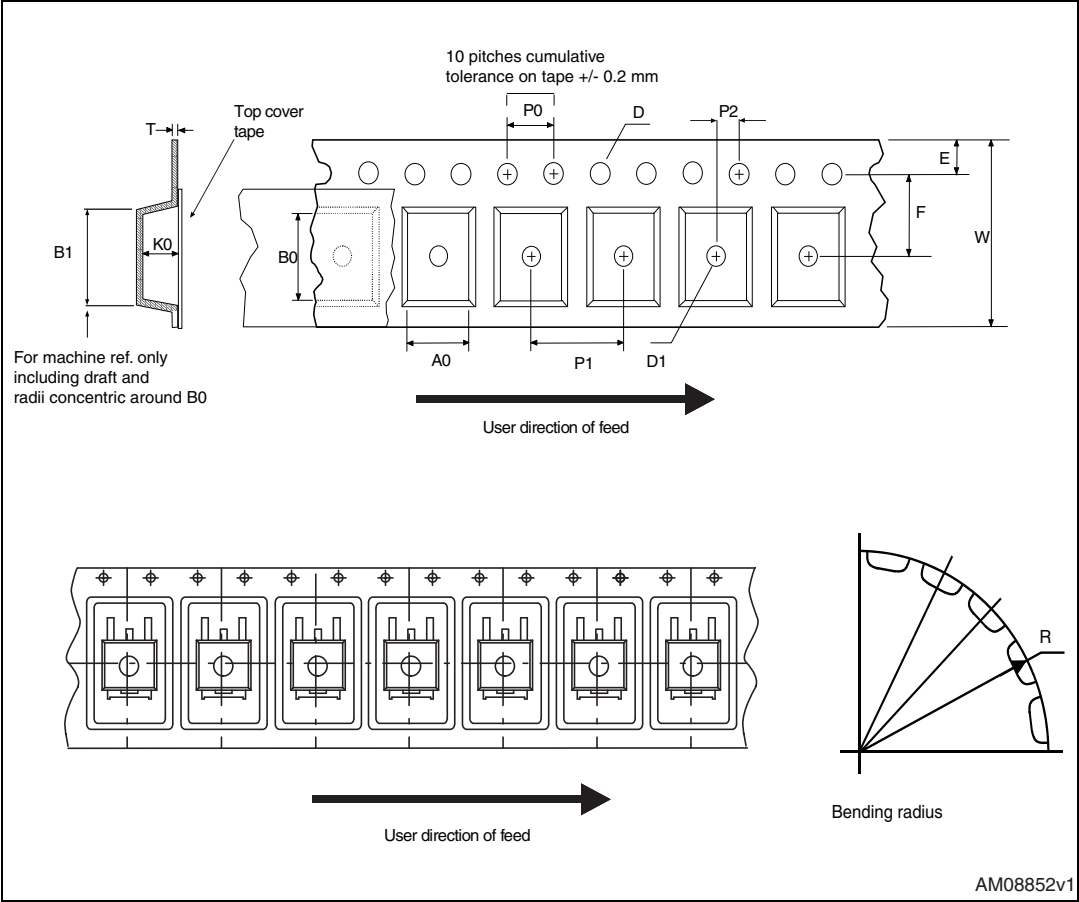
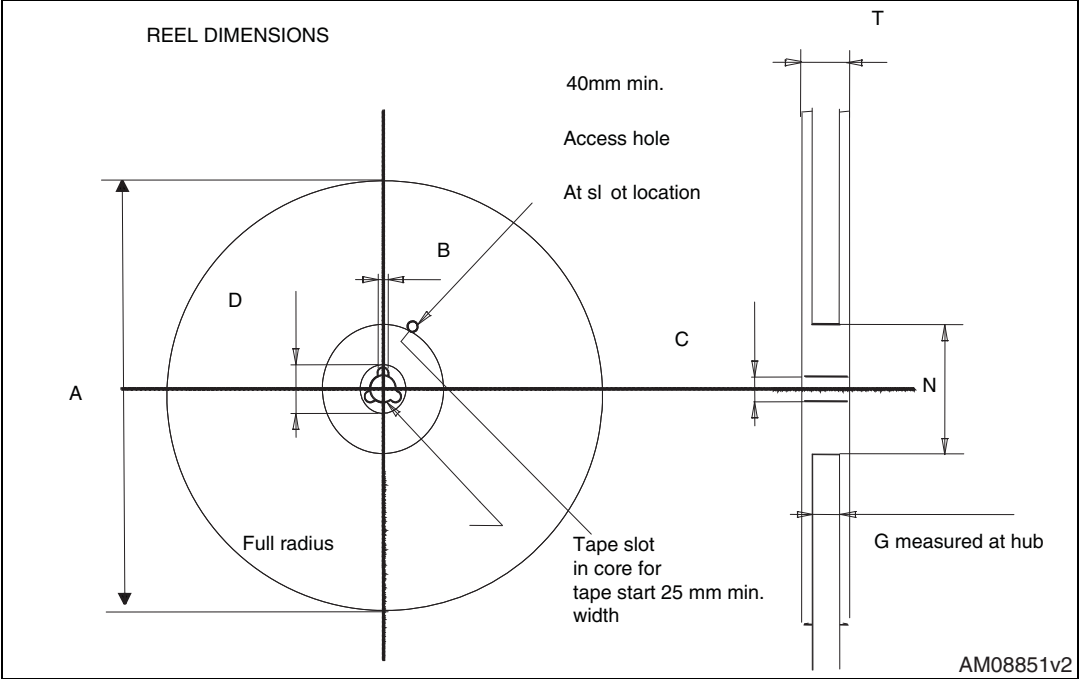


Figure 19. Reel for DPAK (TO-252)



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
22-Aug-2012	1	First release
31-Jan-2013	2	<ul style="list-style-type: none">– Modified: $R_{DS(on)}$ on the title, Features table and Table 4– Modified: typical values on Table 5, 6, 7– Modified: V_{SD} max value on Table 7– Updated: Section 4: Package mechanical data
16-Jul-2013	3	<ul style="list-style-type: none">– Modified: V_{GS} and $I_D=100$ °C values in Table 2– Modified: $R_{DS(on)}$ max value in Table 4, Figure 13, 14 and 15– Inserted: Section 2.1: Electrical characteristics (curves)
10-Sep-2013	4	<ul style="list-style-type: none">– Updated Q_g value in Table 5: Dynamic.

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