STD30NF04LT

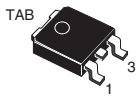
N-channel 40 V, 0.03 Ω typ., 30 A, STripFET™ II Power MOSFET in a DPAK package

Datasheet – production data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STD30NF04LT	40 V	< 0.03 Ω	30 A

- 100% avalanche tested
- Logic level gate drive



DPAK

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Figure 1. Internal schematic diagram

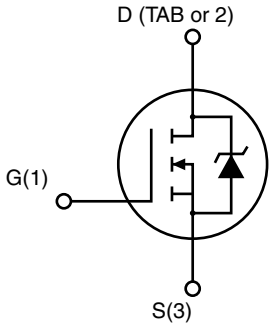


Table 1. Device summary

Order code	Marking	Package	Packaging
STD30NF04LT	D30NF04LT	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	40	V
V_{GS}	Gate- source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	30	A
I_D	Drain current (continuous) at T_C = 100 °C	21	A
I_{DM}	Drain current (pulsed)	120	A
P_{tot}	Total dissipation at T_C = 25 °C	50	W
	Derating factor	0.33	W/°C
dv/dt (2)	Peak diode recovery voltage slope	12.5	V/ns
E_{AS} (3)	Single pulse avalanche energy	340	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Current limited by package
2. I_{SD} ≤ 30 A, di/dt ≤ 300 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.
3. Starting T_j = 25 °C, I_D = 40 A, V_{DD} = 35 V

Table 3. Thermal data

Symbol	Parameter	Max value	Unit
Rthj-case	Thermal resistance junction-case max	3.0	°C/W
Rthj-pcb	Thermal resistance junction-ambient max	see *Section 3 on page 8*	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} =0	40	-		V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = 40 V V_{DS} = 4 V, T_C = 125 °C			-	10 100	µA µA
I_{GSS}(1)	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 15 A V_{GS} = 5 V, I_D = 15 A		-	0.03 0.05	Ω Ω

1. Tested @ VGS = ± 22 V at water level

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 15 A	-	18		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	720 220 45		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 20 V, I_D = 15 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 14*)	-	6 45 25 10		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 20 V, I_D = 30 A, V_{GS} = 10 V (see *Figure 15*)	-	17 3.8 4	25	nC nC nC

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		30 120	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 30 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 30 A, di/dt = 100 A/µs, V_{DD} = 20 V, T_j = 150 °C (see *Figure 16*)	-	30 60 4		ns nC A

1. Pulse width limited by safe operating area.
2. Starting T_j = 25 °C, I_D = 40 A, V_{DD} = 35 V

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

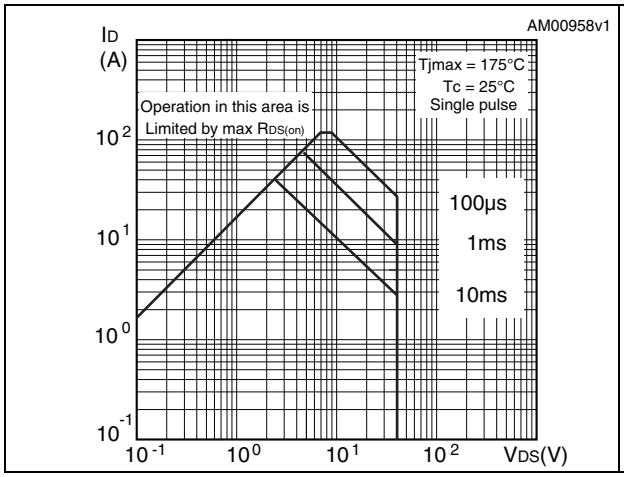


Figure 3. Thermal impedance

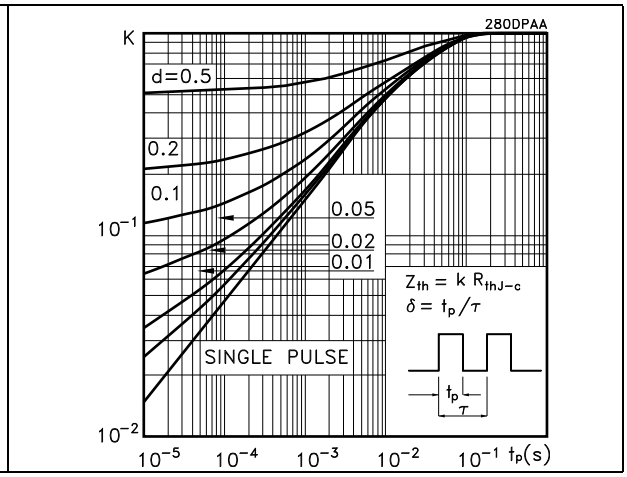


Figure 4. Output characteristics

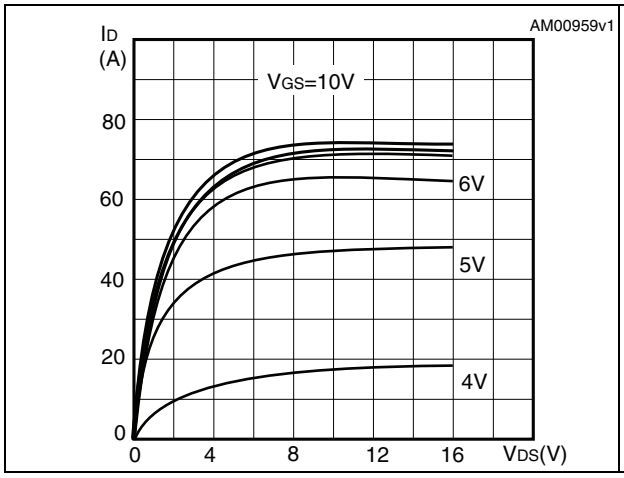


Figure 5. Transfer characteristics

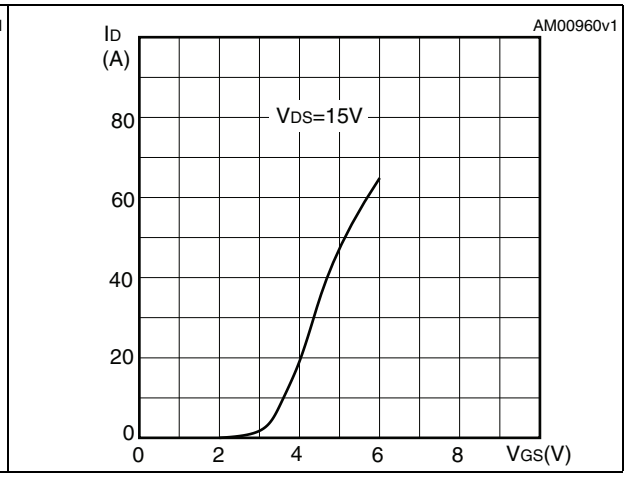


Figure 6. Transconductance

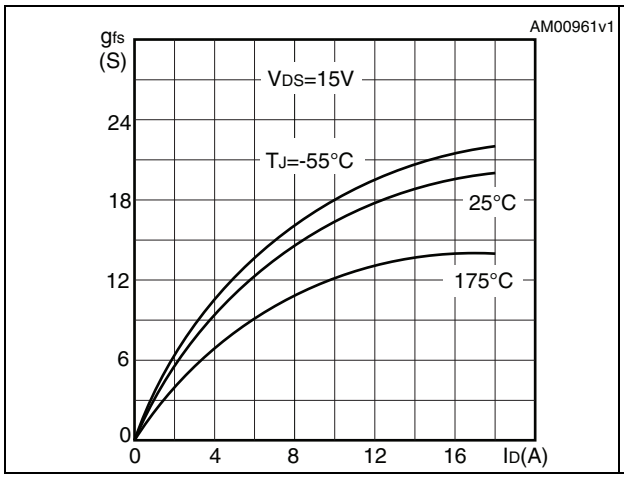


Figure 7. Static drain-source on-resistance

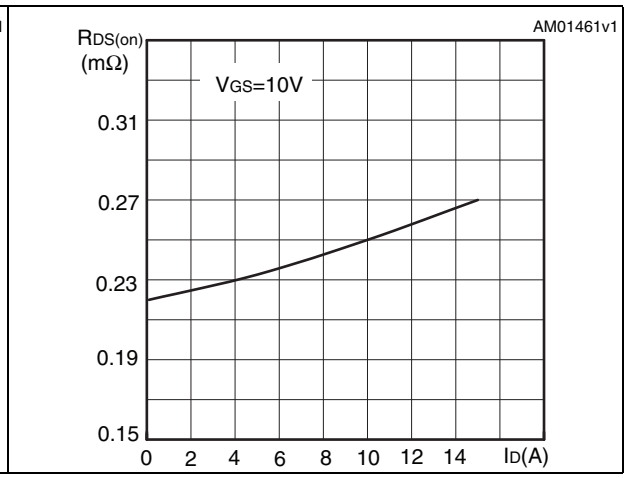


Figure 8. Gate charge vs. gate-source voltage

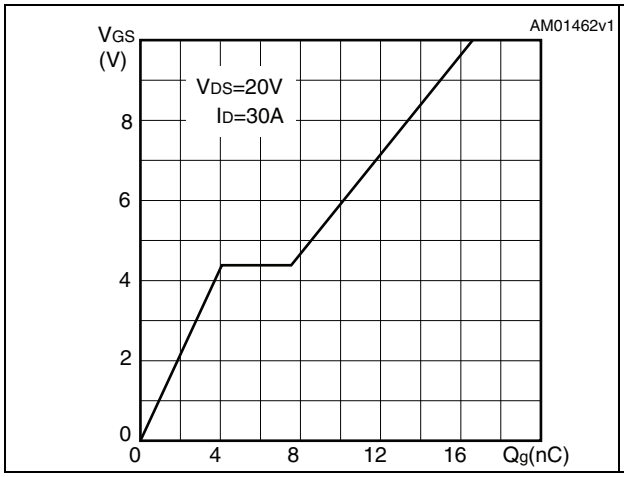


Figure 9. Capacitance variations

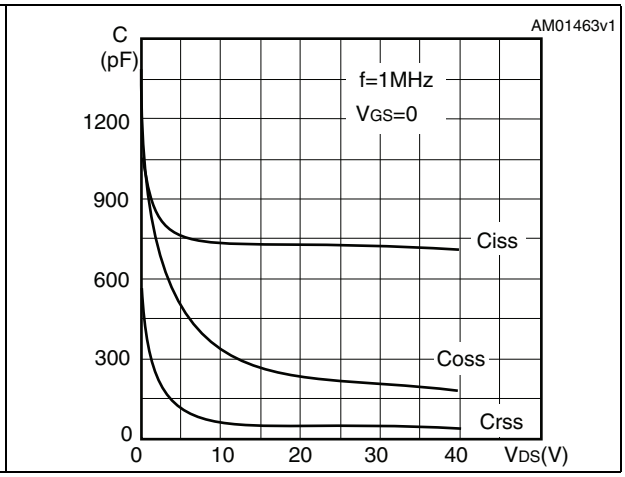


Figure 10. Normalized gate threshold voltage vs. temperature

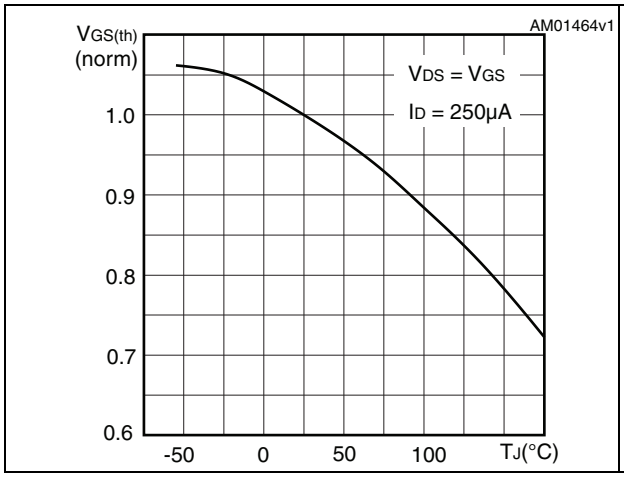


Figure 11. Normalized on resistance vs. temperature

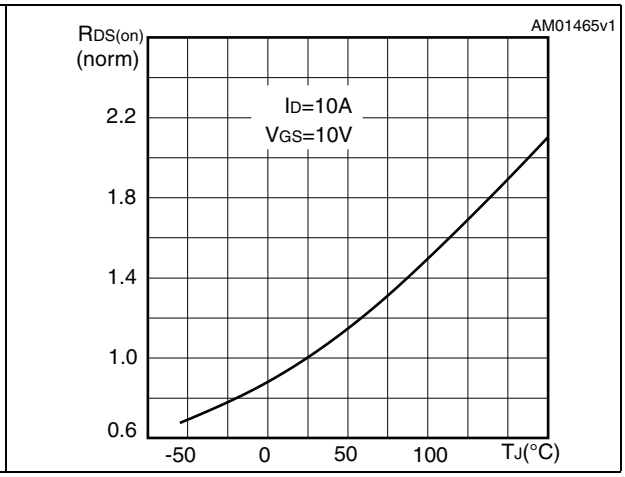


Figure 12. Source-drain diode forward characteristics

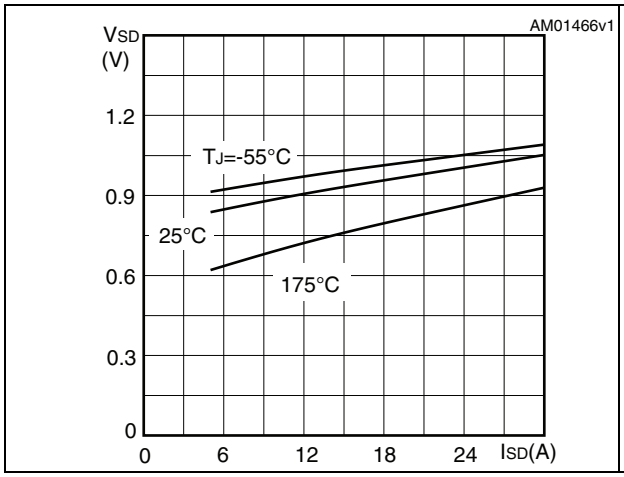
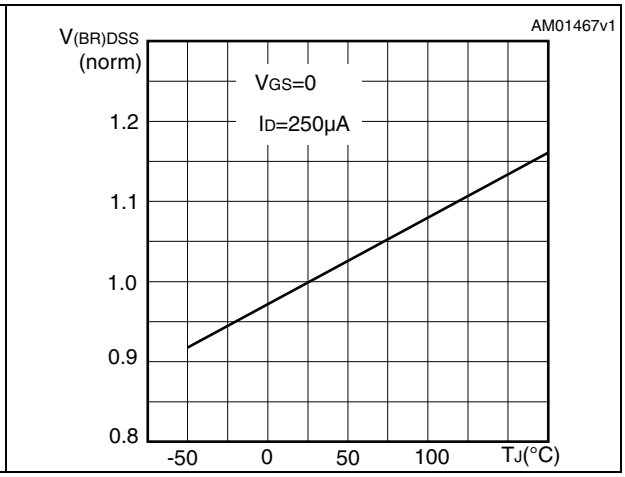


Figure 13. Normalized BV_{DSS} vs. temperature



3 Test circuit Package mechanical data

Figure 14. Switching times test circuit for resistive load

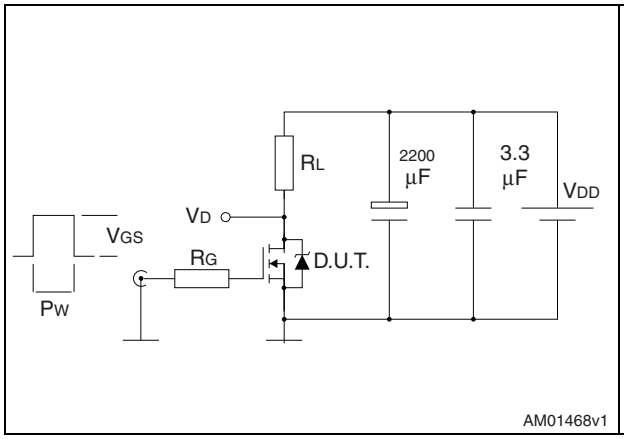


Figure 15. Gate charge test circuit

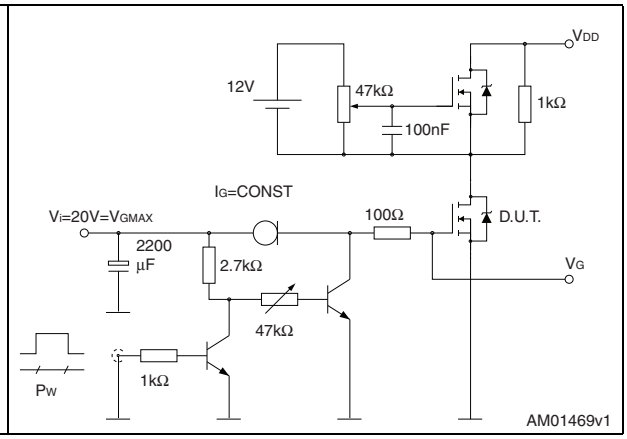


Figure 16. Test circuit for inductive load switching and diode recovery times

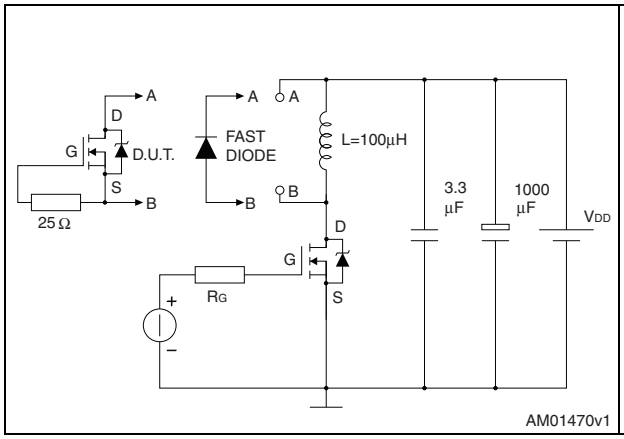


Figure 17. Unclamped Inductive load test circuit

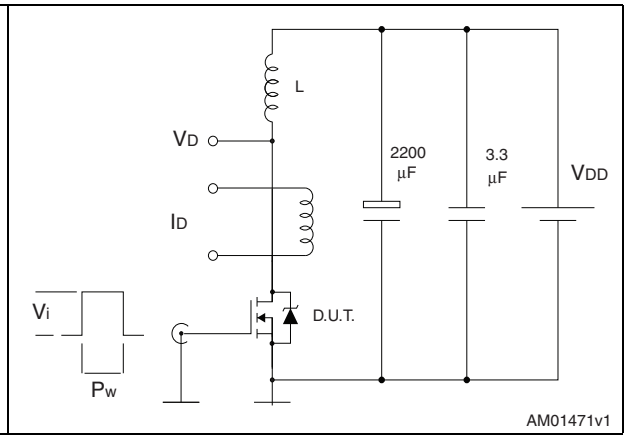


Figure 18. Unclamped inductive waveform

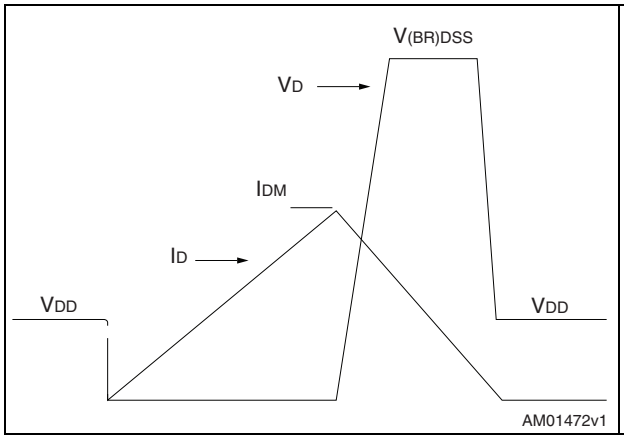
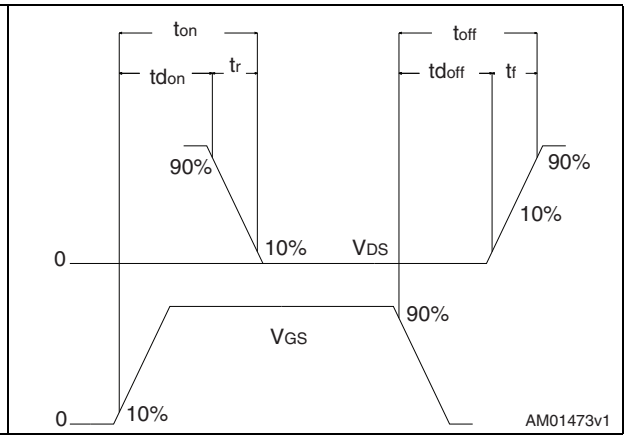


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 7. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) drawing

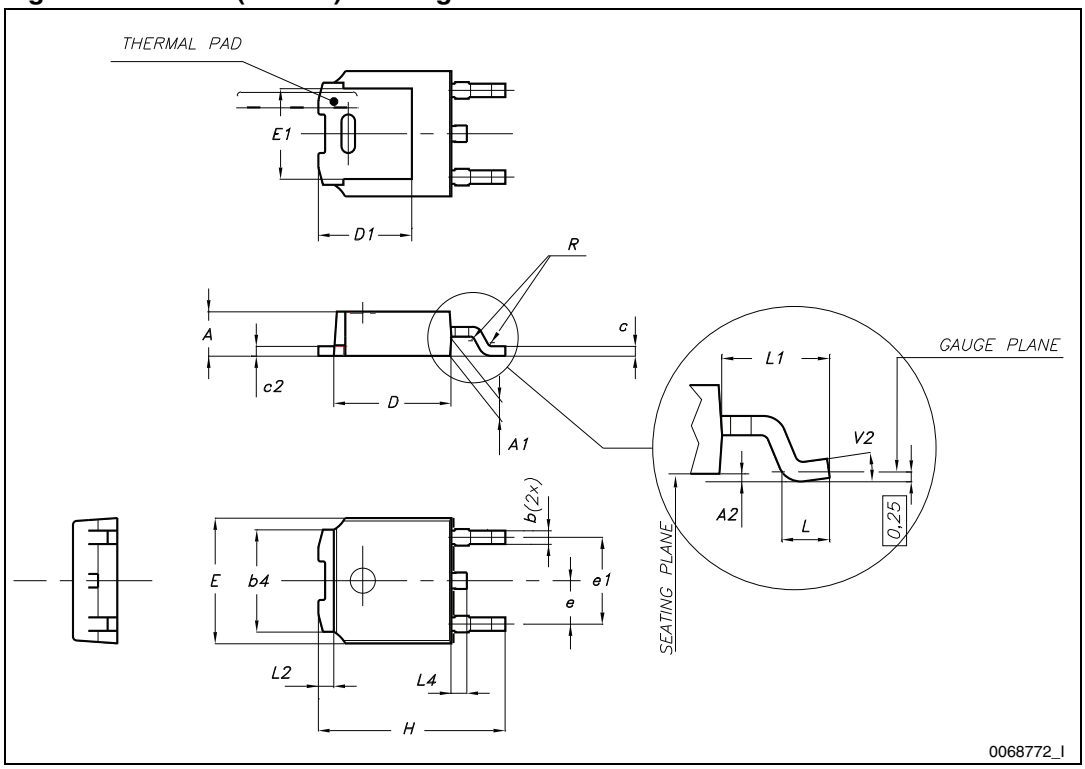
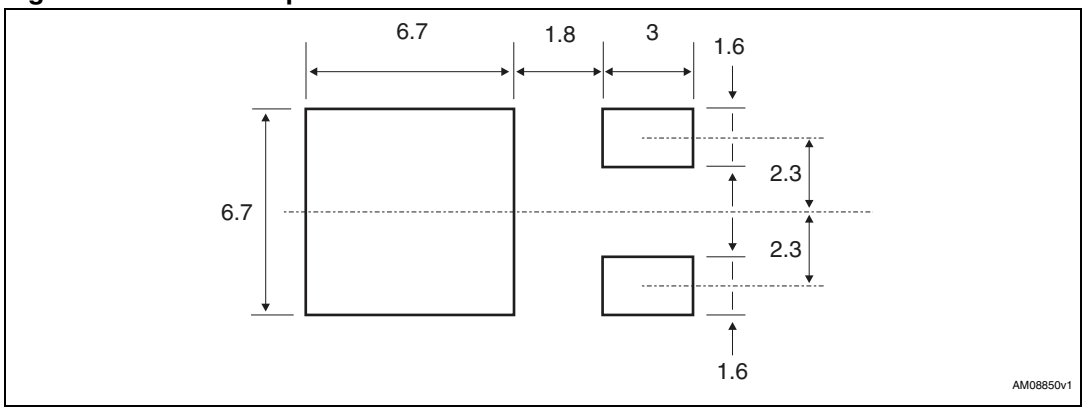


Figure 21. DPAK footprint[a]



a. All dimensions are in millimeters.

5 Packaging mechanical data

Table 8. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 22. Tape

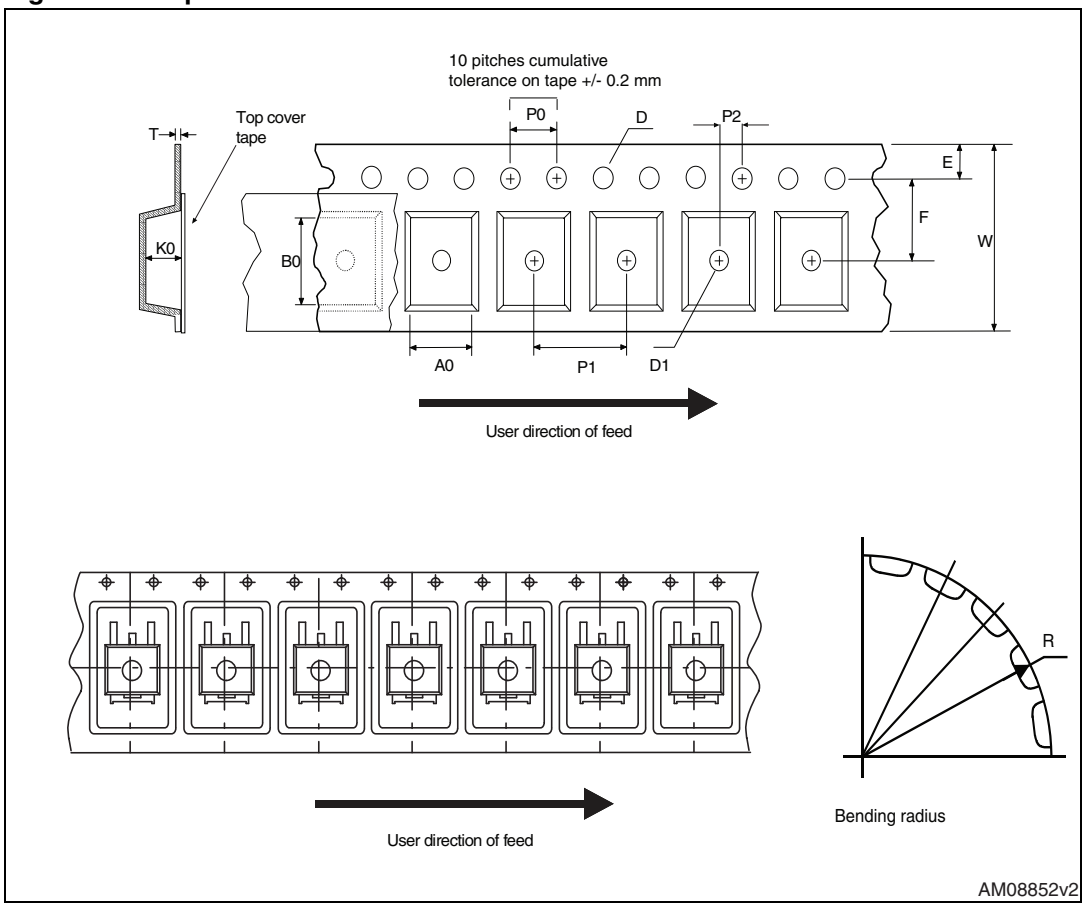
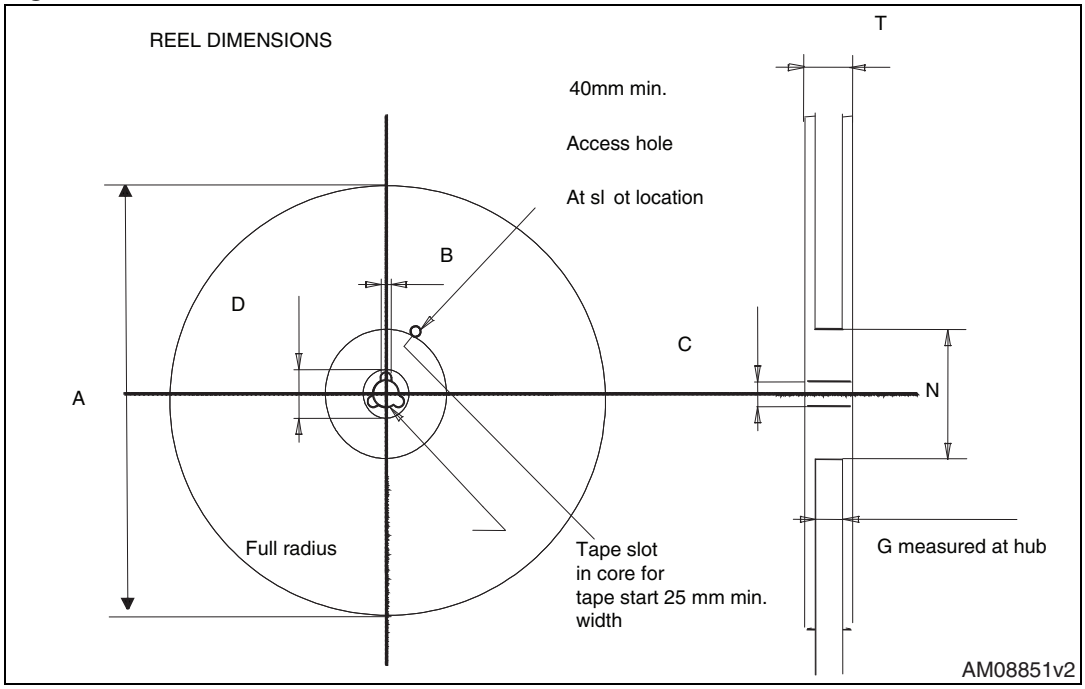


Figure 23. Reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
23-Nov-2012	1	First release.

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