

Automotive-grade N-channel 200 V, 0.10 Ω typ., 18 A STripFET™ low gate charge Power MOSFET in a DPAK package

Datasheet - production data

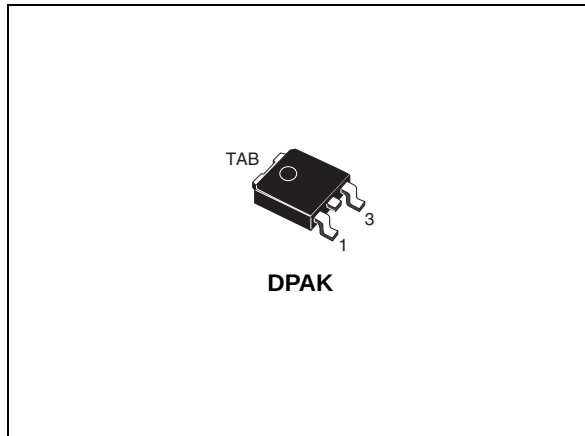
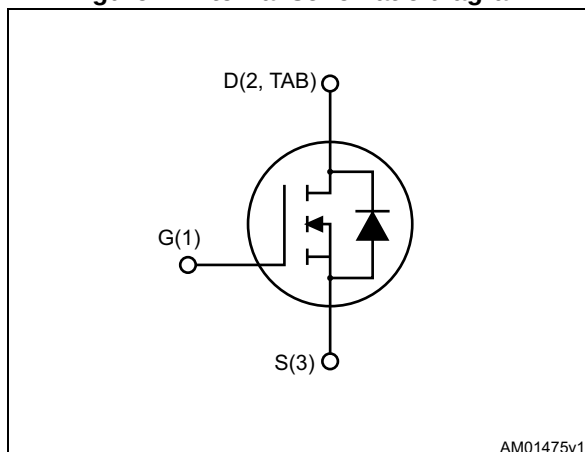


Figure 1. Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	I_D	P_{TOT}
STD25NF20	200 V	0.125 Ω	18 A	110 W

- Designed for automotive applications and AEC-Q101 qualified
- Extremely low gate charge
- Exceptional dv/dt capability
- Low gate input resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This N-channel enhancement mode Power MOSFET benefits from the latest refinement of STMicroelectronics' unique "single feature size" strip-based process, which decreases the critical alignment steps to offer exceptional manufacturing reproducibility. The result is a transistor with extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD25NF20	25NF20	DPAK	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	200	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	18	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(2)}$	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
	Derating factor	0.72	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. The value is rated according to $R_{thj-case}$.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 18\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$; $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.38	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50 ⁽¹⁾	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetitive (pulse width limited by T_{jmax})	18	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD}=50$)	110	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 200\text{ V}$			1	μA
		$V_{DS} = 200\text{ V}$, $T_C = 125\text{ °C}$			50	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.10	0.125	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	940		pF
C_{oss}	Output capacitance		-	197		pF
C_{rss}	Reverse transfer capacitance		-	30		pF
Q_g	Total gate charge	$V_{DD} = 160\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	28	39	nC
Q_{gs}	Gate-source charge		-	5.6		nC
Q_{gd}	Gate-drain charge		-	14.5		nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_d(on)$	Turn-on delay time	$V_{DD} = 100\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14 and Figure 17)	-	15	-	ns
$t_r(v)$	Voltage rise time		-	30	-	ns
$t_d(off)$	Turn-off-delay time		-	40	-	ns
$t_f(i)$	Fall time		-	10	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 27\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17)	-	155		ns
Q_{rr}	Reverse recovery charge		-	775		nC
I_{RRM}	Reverse recovery current		-	10		A
t_{rr}	Reverse recovery time	$I_{SD} = 27\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	183		ns
Q_{rr}	Reverse recovery charge		-	1061		nC
I_{RRM}	Reverse recovery current		-	11.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

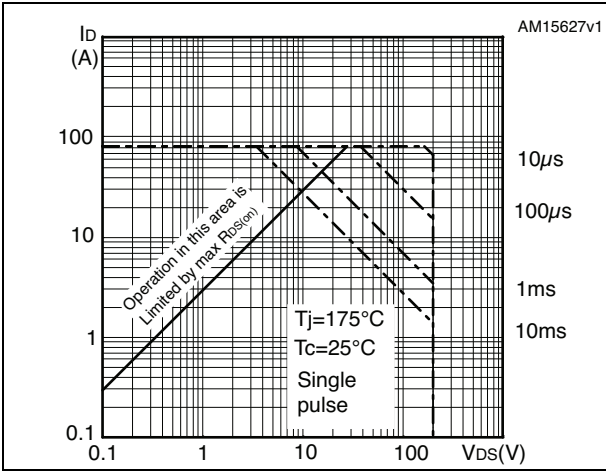


Figure 3. Thermal impedance

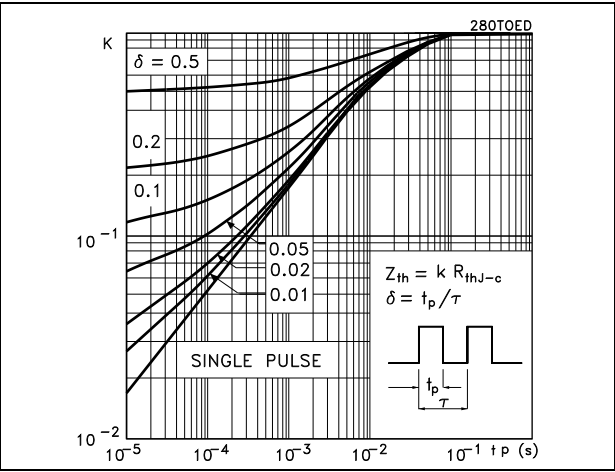


Figure 4. Output characteristics

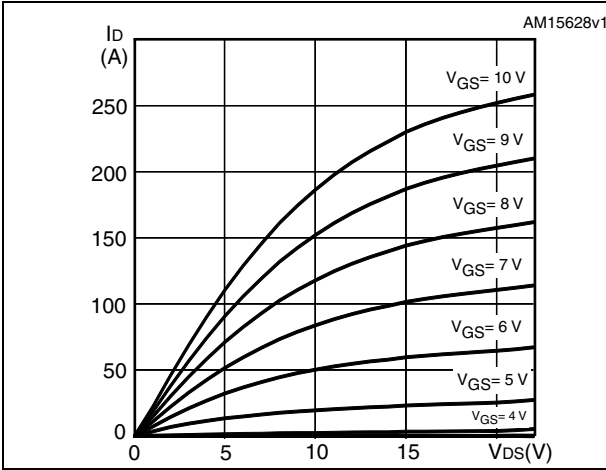


Figure 5. Transfer characteristics

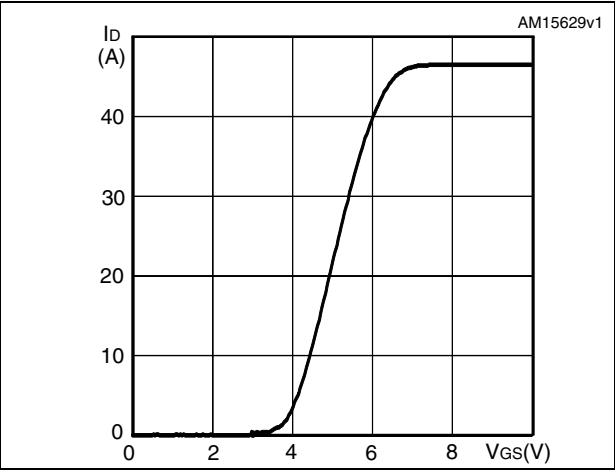


Figure 6. Gate charge vs gate-source voltage

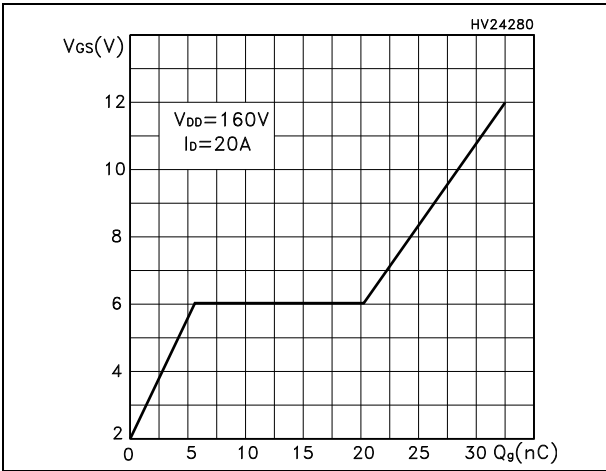


Figure 7. Static drain-source on-resistance

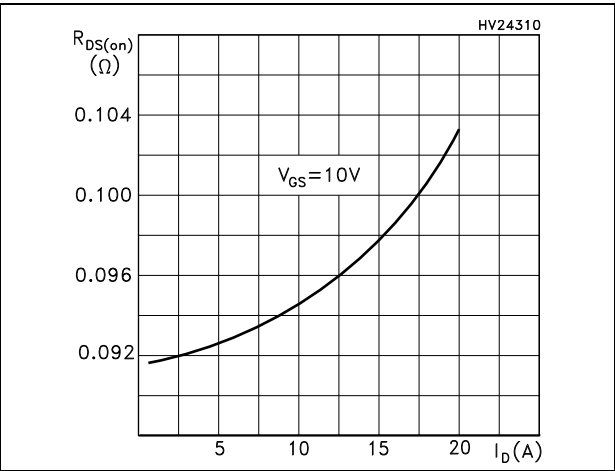


Figure 8. Capacitance variations

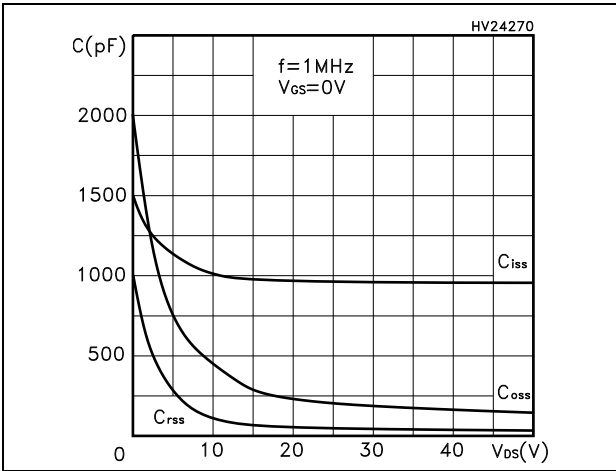


Figure 9. Source-drain diode forward characteristics

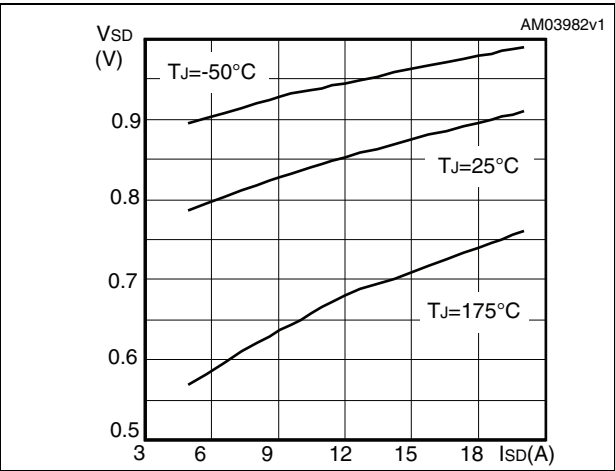


Figure 10. Normalized gate threshold voltage vs temperature

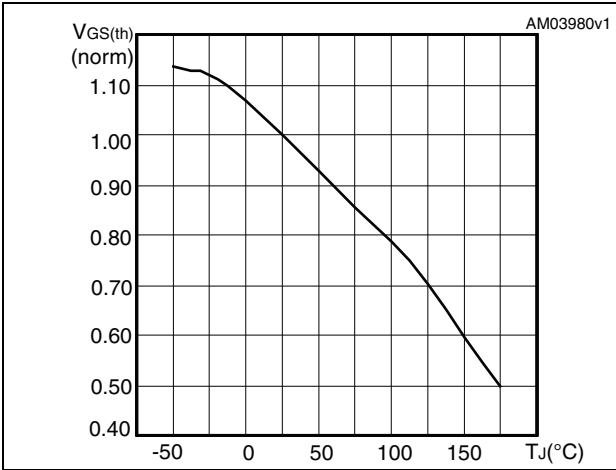
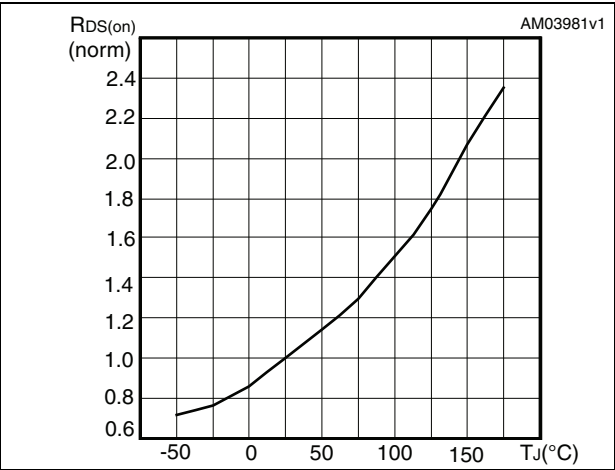


Figure 11. Normalized on-resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

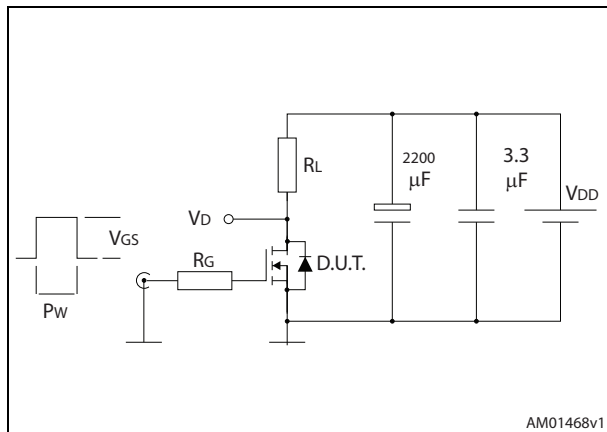


Figure 13. Gate charge test circuit

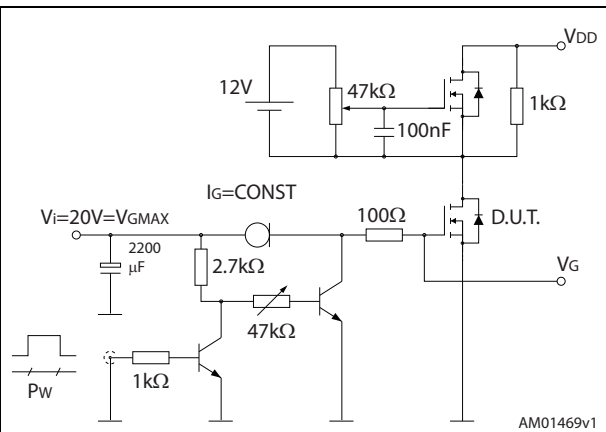


Figure 14. Test circuit for inductive load switching and diode recovery times

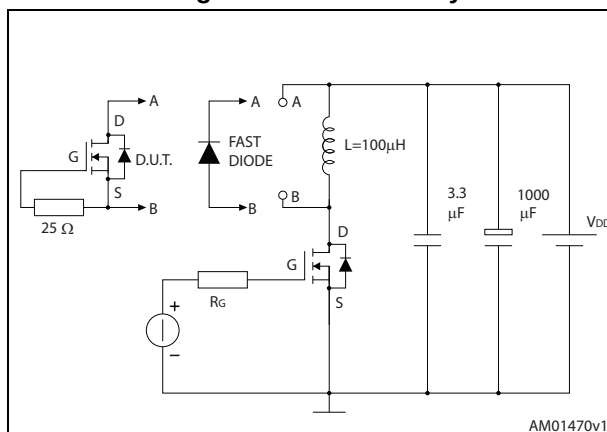


Figure 15. Unclamped inductive load test circuit

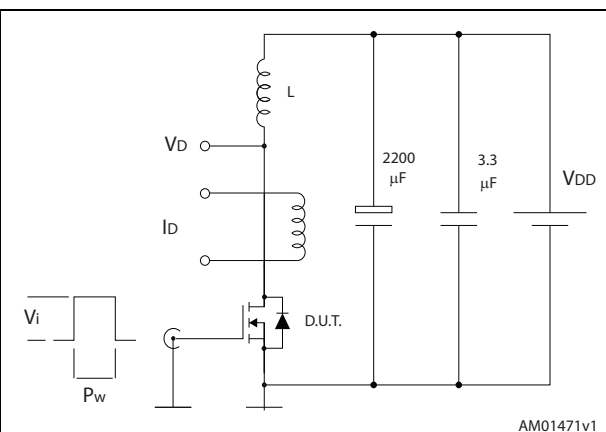


Figure 16. Unclamped inductive waveform

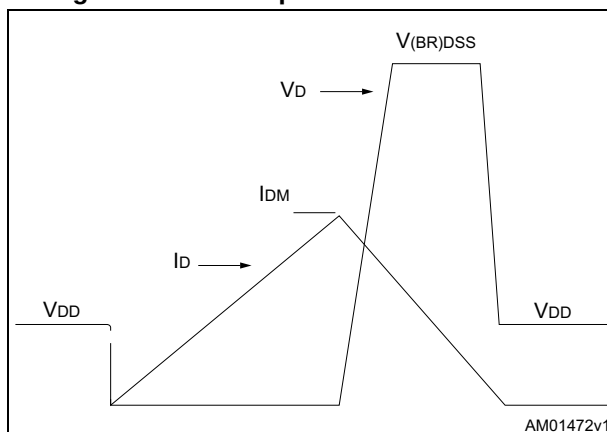
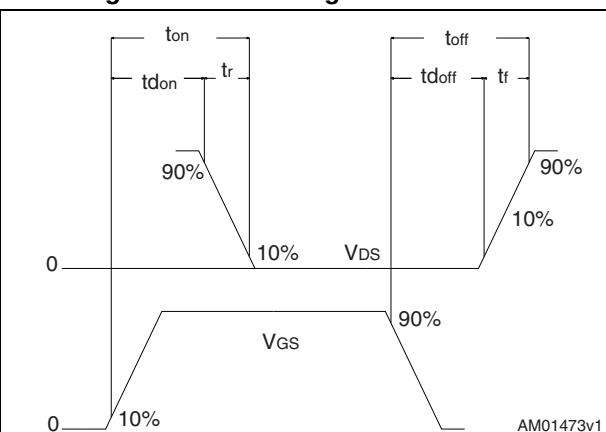


Figure 17. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 18. DPAK (TO-252) drawing

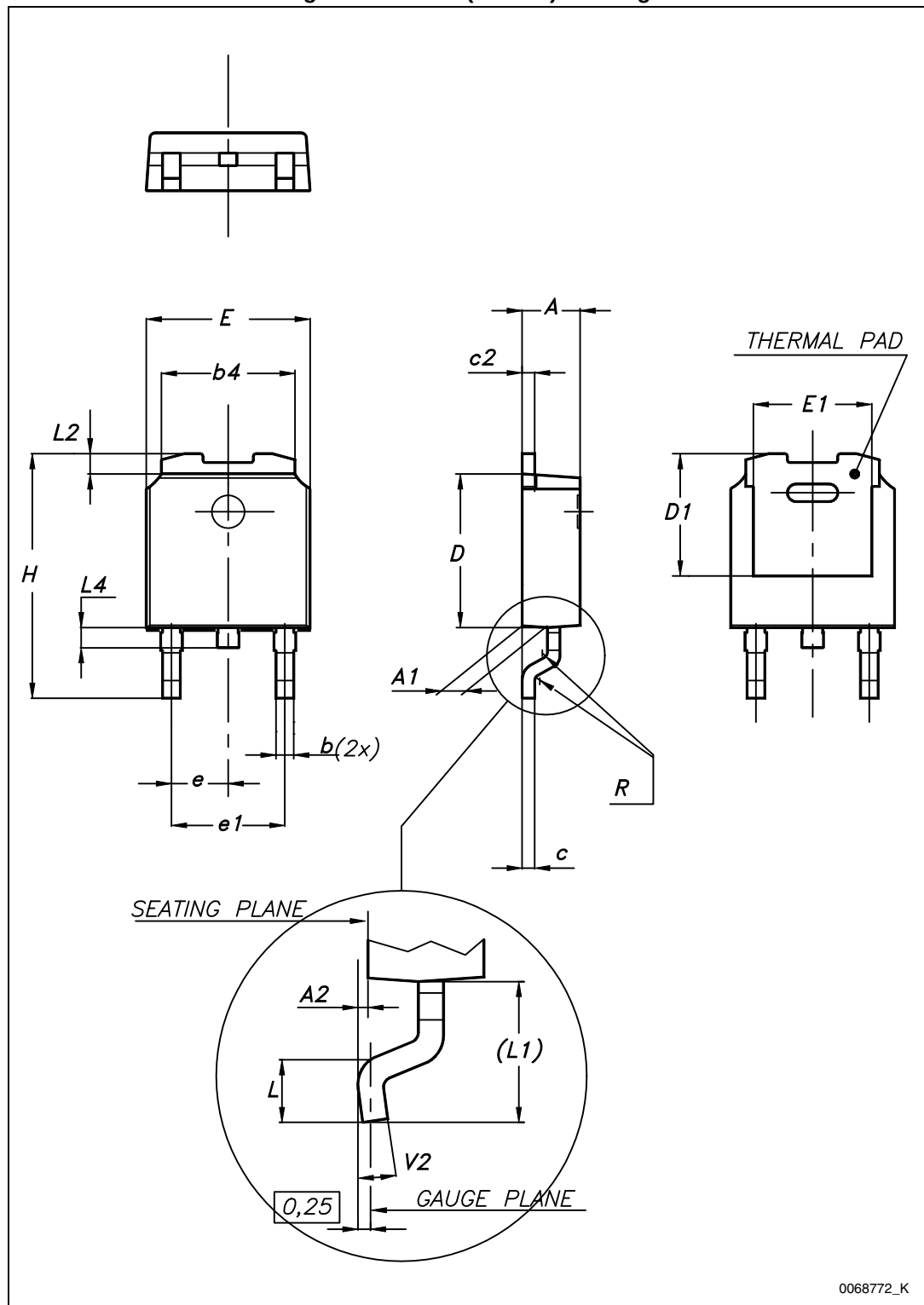
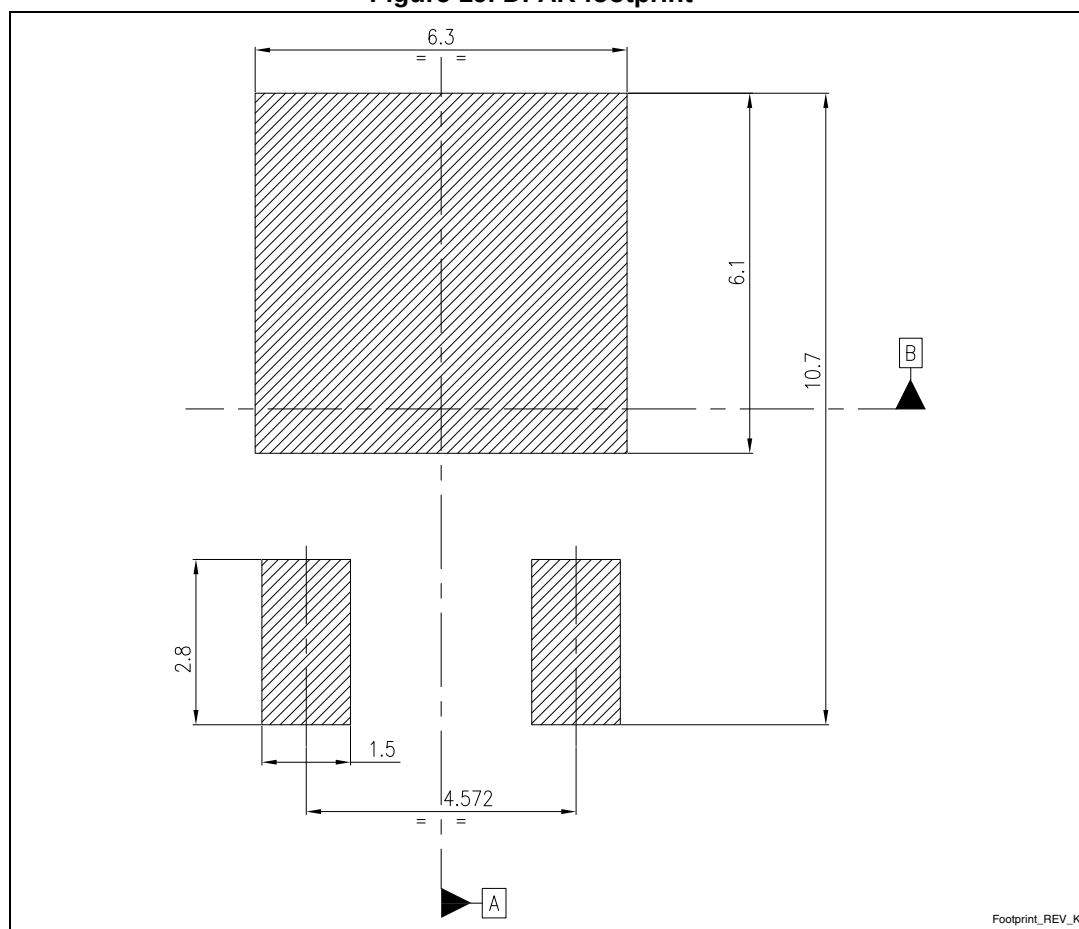


Figure 19. DPAK footprint (a)



a. All dimensions are in millimeters

5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 20. Tape for DPAK (TO-252)

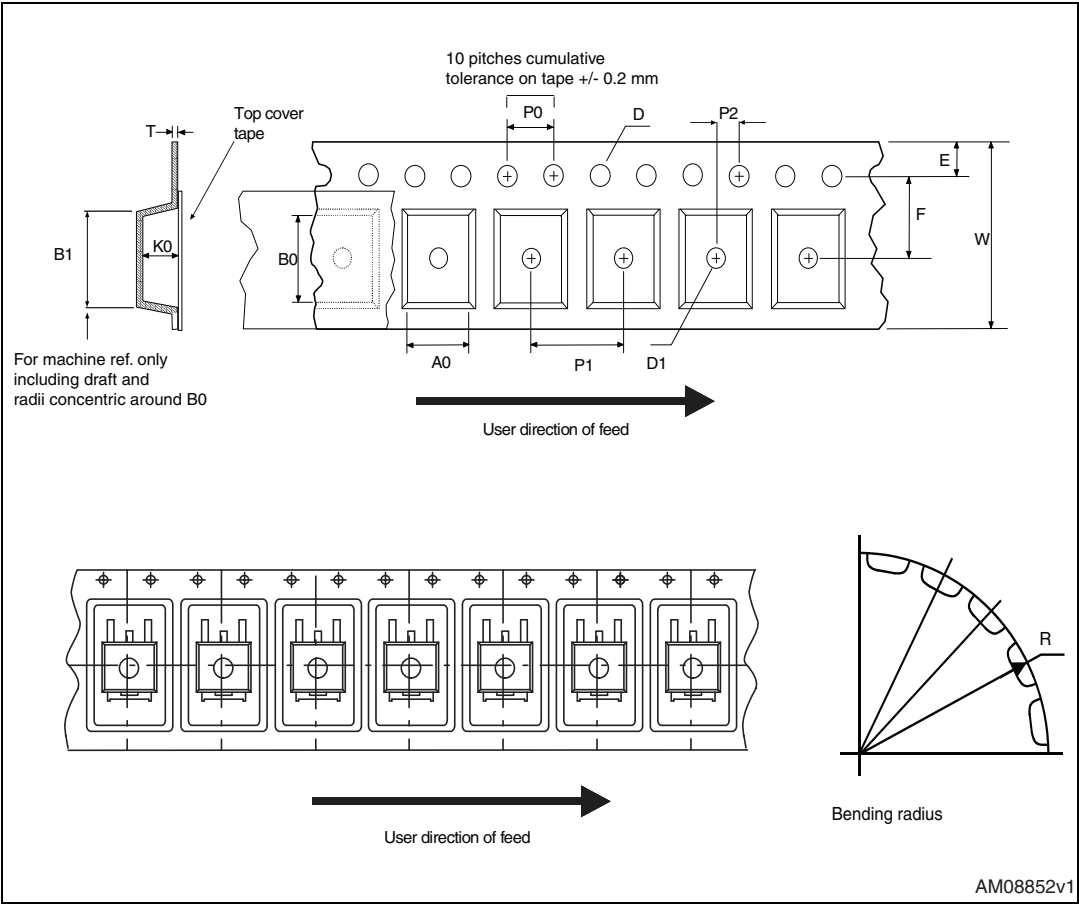
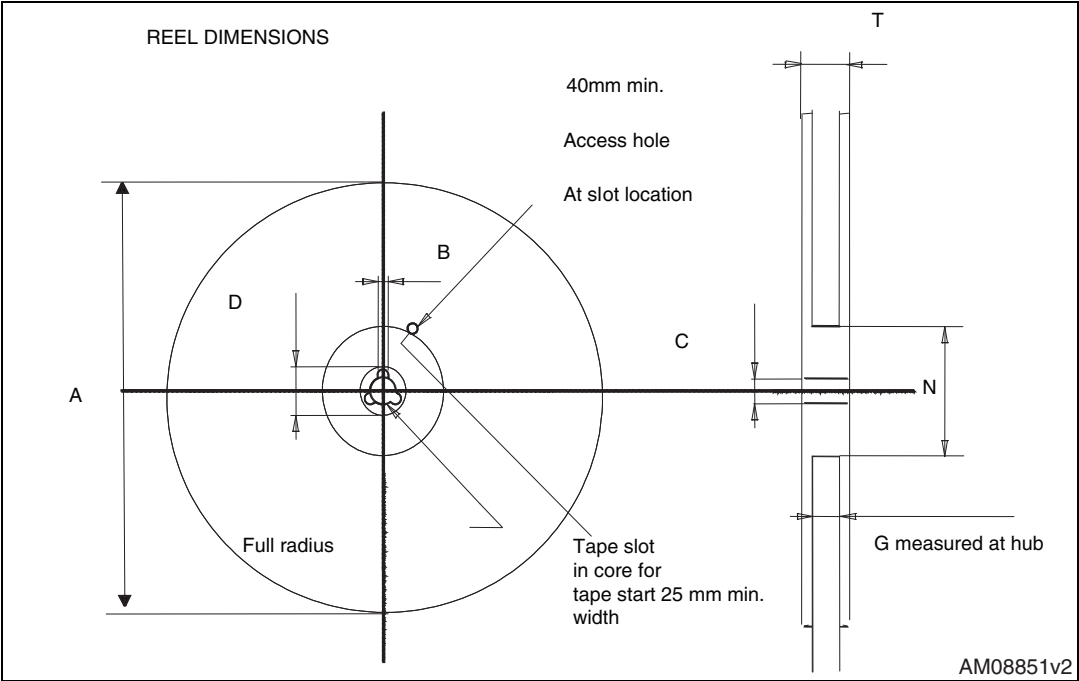


Figure 21. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
12-Mar-2013	1	First release.
03-Sep-2013	2	– Modified: title and <i>Features</i> in cover page – Modified: <i>Figure 12, 13, 14</i> and <i>15</i> – Minor text changes

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