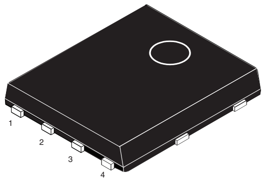
STL90N10F7

N-channel 100 V, 0.009 Ω typ., 16 A STripFET™ VII DeepGATE™ Power MOSFETs in a PowerFLAT™ 5x6 package

Datasheet - preliminary data



PowerFLAT™5x6

Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D	P_{TOT}
STL90N10F7	100 V	0.00105 Ω	16 A(1)	5 W

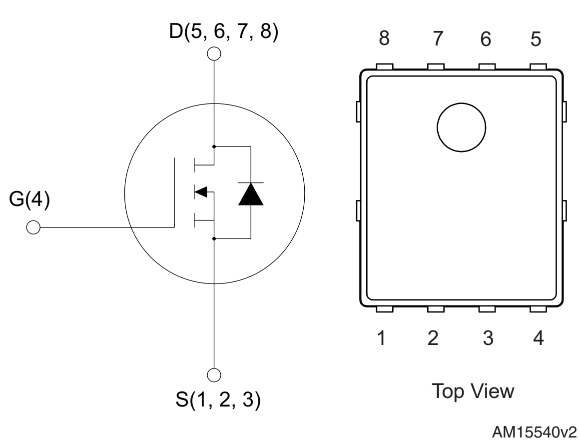
1. The value is rated according $R_{thj-pcb}$.

- Extremely low gate charge
- Ultra low on-resistance
- Low gate input resistance

Applications

- Switching applications

Figure 1. Internal schematic diagram



Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL90N10F7	90N10F7	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D(1)	Drain current (continuous)	70	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	50	A
I_D(2)	Drain current (continuous)	16	A
I_D(2)	Drain current (continuous) at T_C = 100 °C	11	A
I_{DM}(2)(3)	Drain current (pulsed)	64	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	100	W
P_{TOT}(2)	Total dissipation at T_C = 25 °C	5	W
T_{stg}	Storage temperature	-55 to 175 °C	°C
T_j	Max. operating junction temperature		

1. This value is rated according to R_{thj-c}
2. This value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-pcb max	31	°C/W
$R_{thj-case}$	Thermal resistance junction-case max	1.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V V_{DS} = 100 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = + 20 V			100	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8 A		0.009	0.0105	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	3550	-	pF
C_{oss}	Output capacitance		-	610	-	pF
C_{rss}	Reverse transfer capacitance		-	20	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 16 A, V_{GS} = 10 V (see *Figure 3*)	-	39	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 8 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 4* and *Figure 7*)	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	16	A
I_{SDM} (1)	Source-drain current (pulsed)		-	-	64	A
V_{SD} (2)	Forward on voltage	I_{SD} = 16 A, V_{GS} = 0	-	-	1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs V_{DD} = 80 V, T_j=150 °C (see *Figure 7*)	-	-		ns
Q_{rr}	Reverse recovery charge		-	-		nC
I_{RRM}	Reverse recovery current		-	-		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

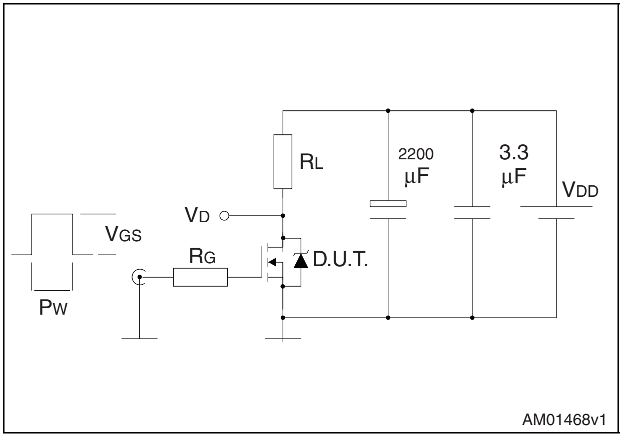


Figure 3. Gate charge test circuit

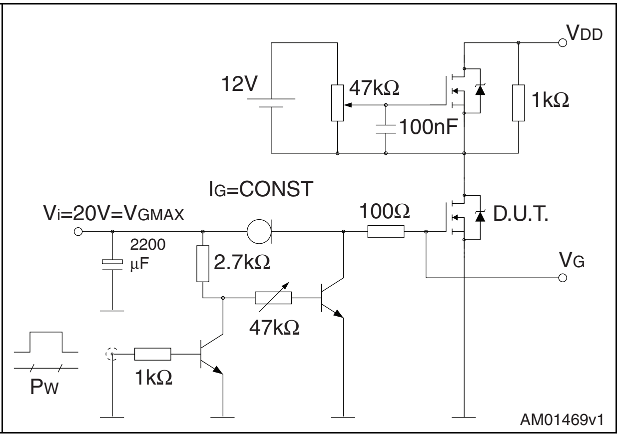


Figure 4. Test circuit for inductive load switching and diode recovery times

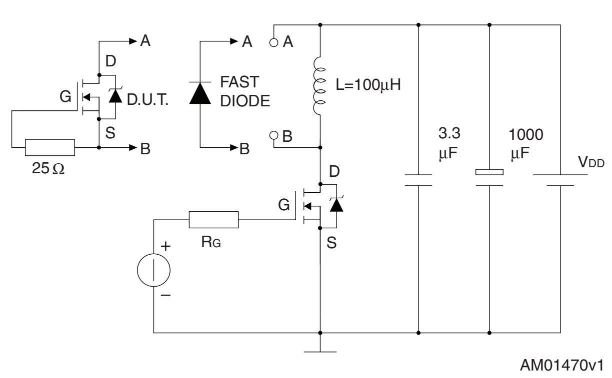


Figure 5. Unclamped inductive load test circuit

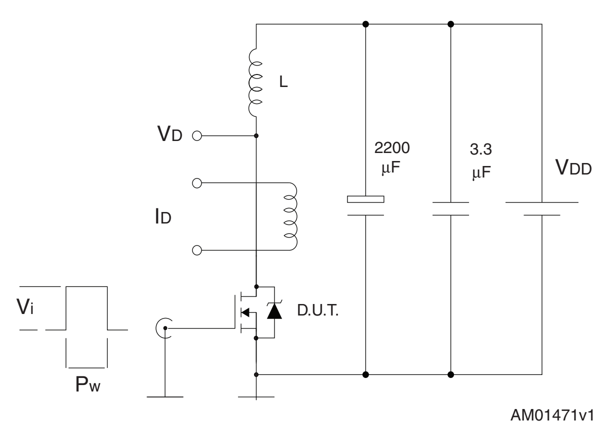


Figure 6. Unclamped inductive waveform

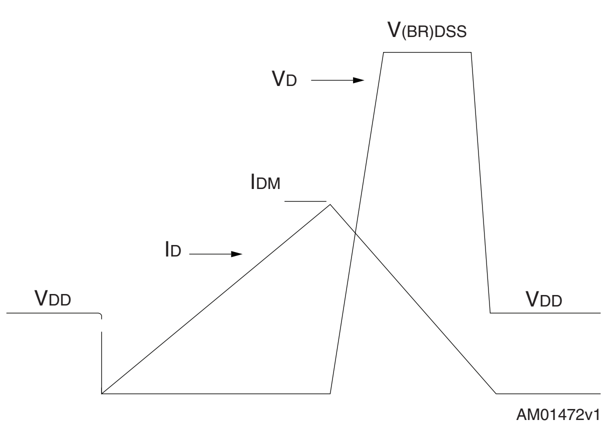
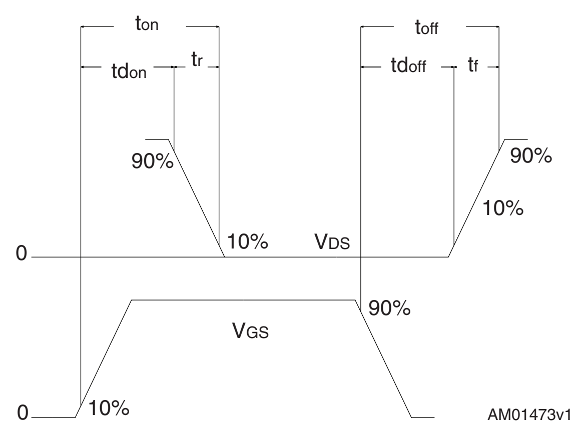


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. PowerFLAT 5x6 (Ribbon) type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 8. PowerFLAT 5x6 (Ribbon) type S-R drawing

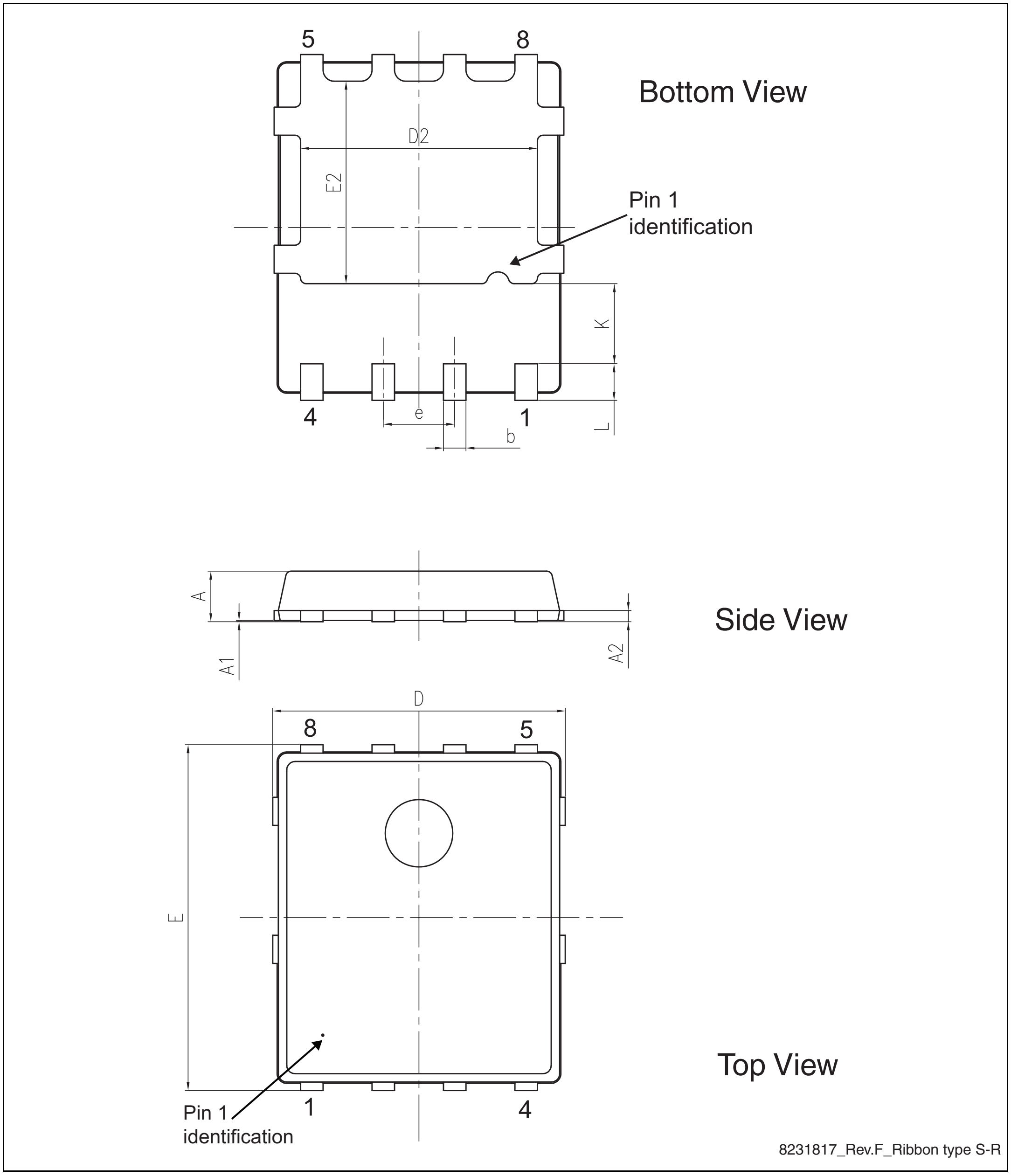
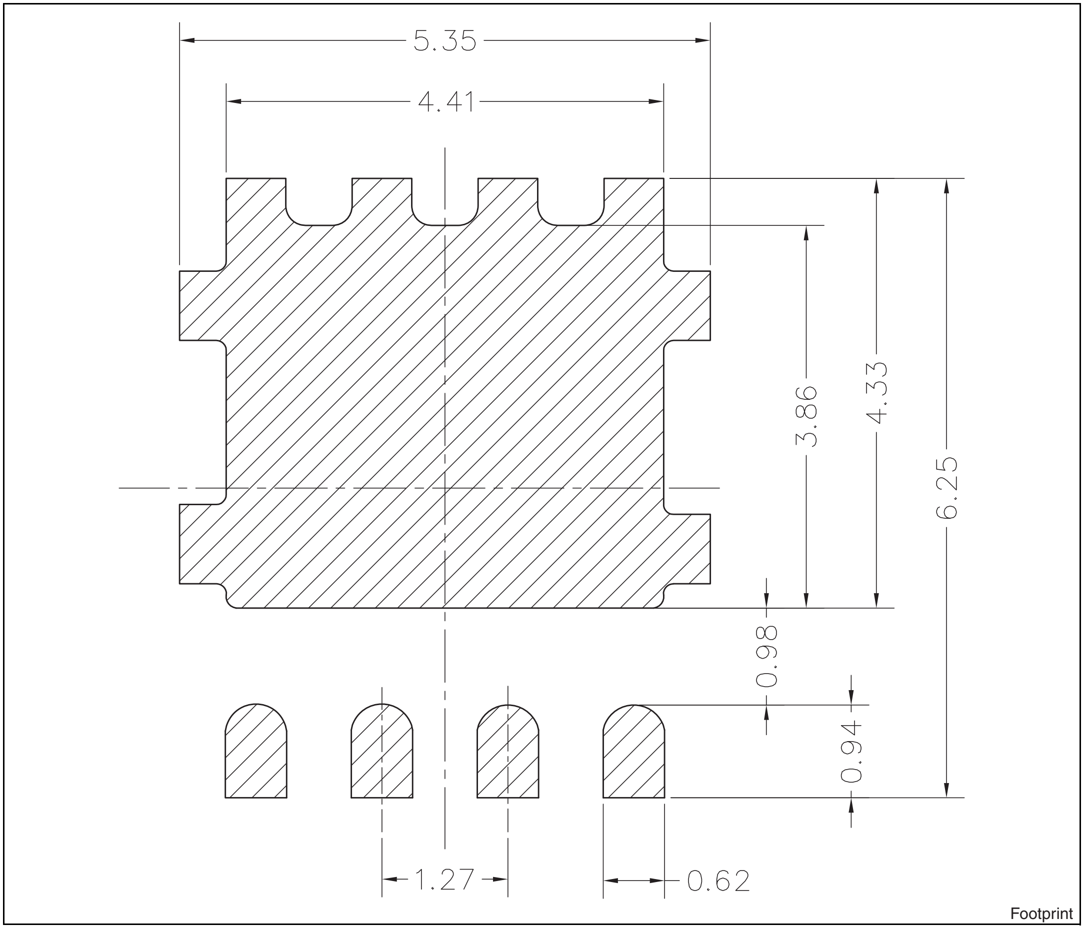
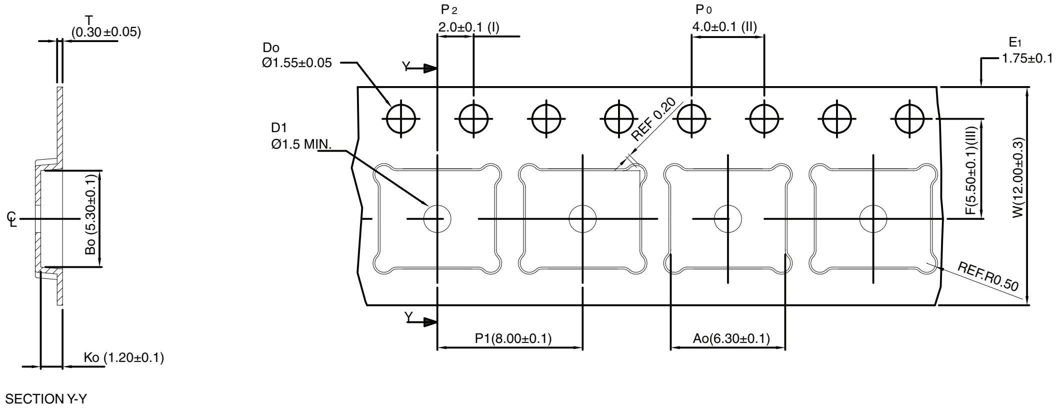


Figure 9. Recommended footprint



5 Packaging mechanical data

Figure 10. PowerFLAT™ 5x6 tape[a]



(I) Measured from centerline of sprocket hole to centerline of pocket.

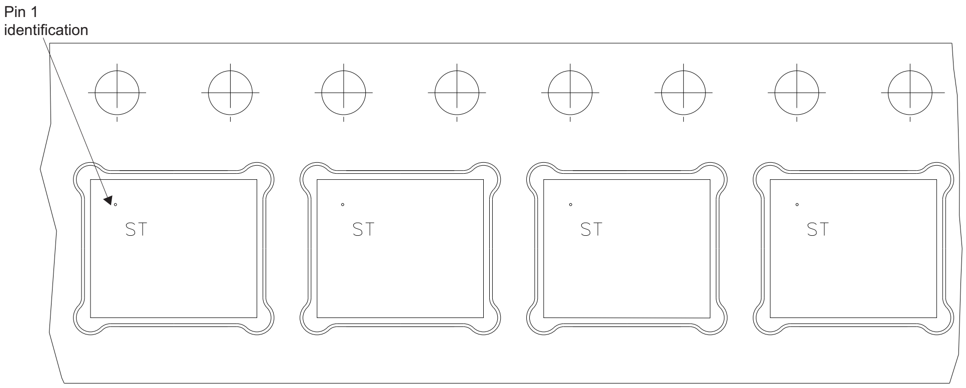
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centerline of sprocket hole to centerline of pocket.

Base and bulk quantity 3000 pcs

8234350_Tape_rev_C

Figure 11. PowerFLAT™ 5x6 package orientation in carrier tape.



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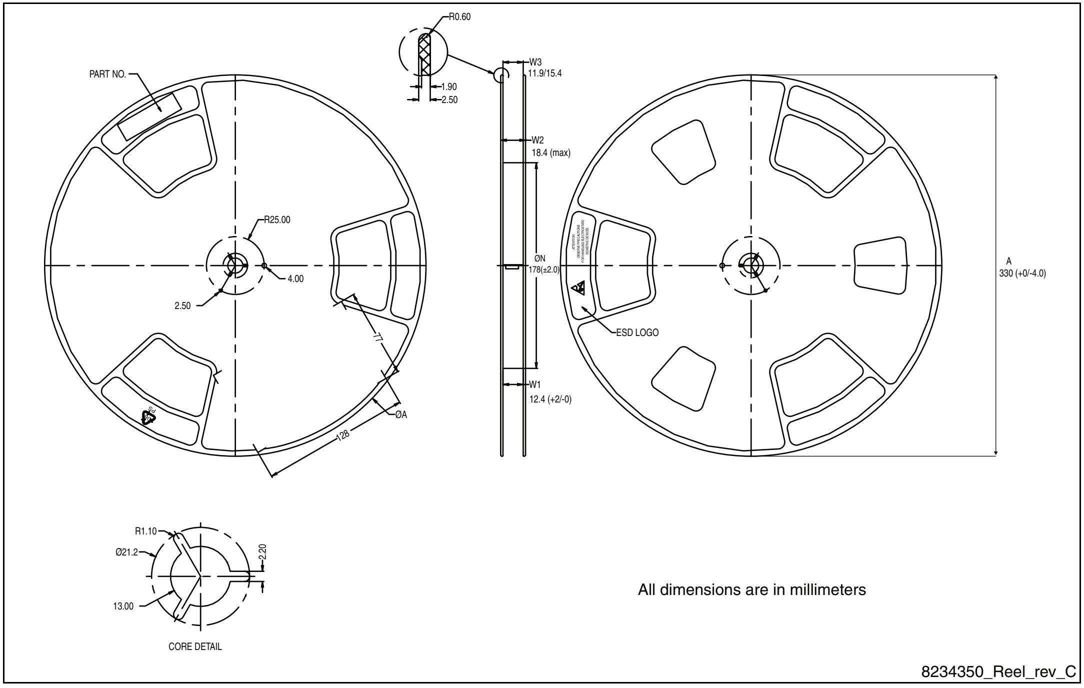
[a] All dimensions are in millimeters.

Figure 12. PowerFLAT™ 5x6 reel



All dimensions are in millimeters

8234350_Reel_rev_C

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Apr-2013	1	First release.

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