

STF6N60M2, STP6N60M2, STU6N60M2

N-channel 600 V, 1.06 Ω typ., 4.5 A MDmesh II PlusTM low Q_g
Power MOSFET in TO-220FP, TO-220 and IPAK packages

Datasheet - production data

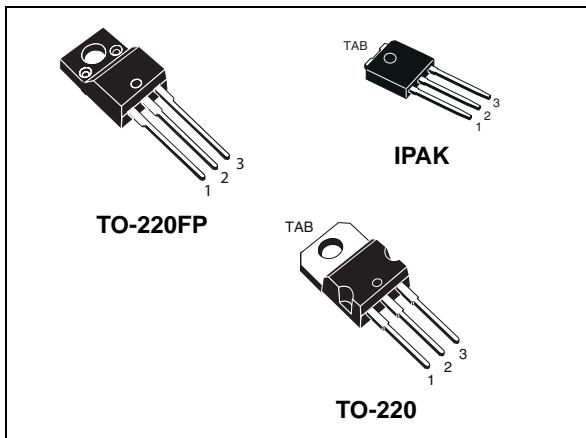
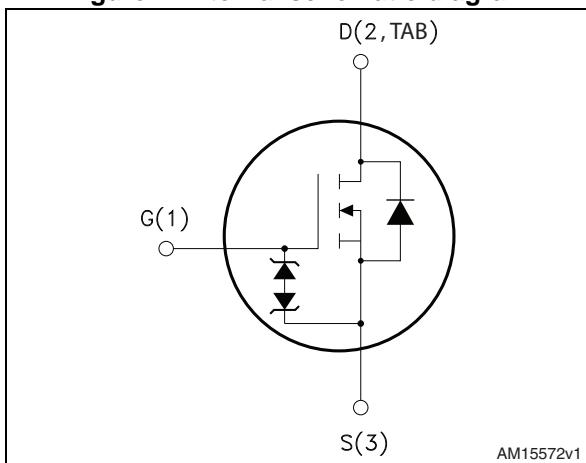


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS} @ T _{Jmax}	R _{DS(on)} max	I _D
STF6N60M2	650 V	1.2 Ω	4.5 A
STP6N60M2			
STU6N60M2			

- Extremely low gate charge
- Lower R_{DS(on)} x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmeshTM technology: MDmesh II PlusTM low Q_g. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF6N60M2	6N60M2	TO-220FP	Tube
STP6N60M2		TO-220	
STU6N60M2		IPAK	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220, IPAK	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4.5 ⁽¹⁾	4.5	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.9 ⁽¹⁾	2.9	A
$I_{DM}^{(2)}$	Drain current (pulsed)	18 ⁽¹⁾	18	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	20	60	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1$ s; $T_C=25^\circ\text{C}$)	2500		V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50		
T_{stg}	Storage temperature	- 55 to 150		$^\circ\text{C}$
T_j	Max. operating junction temperature			

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 4.5$ A, $di/dt \leq 400$ A/ μs ; V_{DS} peak < $V_{(BR)DSS}$, $V_{DD}=400$ V
4. $V_{DS} \leq 480$ V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220FP	TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	6.25	2.08		$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	100	$^\circ\text{C/W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value		Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})		1	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AR}$; $V_{DD}=50$)		86	mJ

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600 \text{ V}$			1	μA
		$V_{DS} = 600 \text{ V}, T_C = 125^\circ\text{C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			± 10	μA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 2.25 \text{ A}$		1.06	1.2	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	232	-	pF
C_{oss}	Output capacitance		-	14	-	pF
C_{rss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \text{ V}, V_{GS} = 0$	-	71	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz}$ open drain	-	6.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 4.5 \text{ A}, V_{GS} = 10 \text{ V}$ (see Figure 18)	-	8	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	4	-	nC

- $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 1.65 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 17 and Figure 22)	-	9.5	-	ns
t_r	Rise time		-	7.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	22.5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		18	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.5 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <i>Figure 19</i>)	-	274		ns
Q_{rr}	Reverse recovery charge		-	1.47		nC
I_{RRM}	Reverse recovery current		-	10.7		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 19</i>)	-	376		ns
Q_{rr}	Reverse recovery charge		-	1.96		nC
I_{RRM}	Reverse recovery current		-	10.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

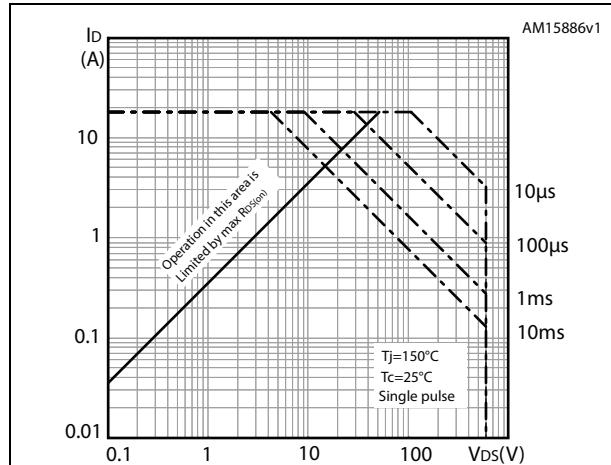


Figure 3. Thermal impedance for TO-220FP

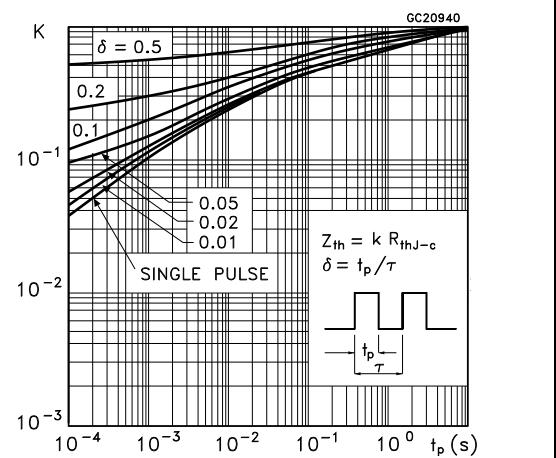


Figure 4. Safe operating area for TO-220

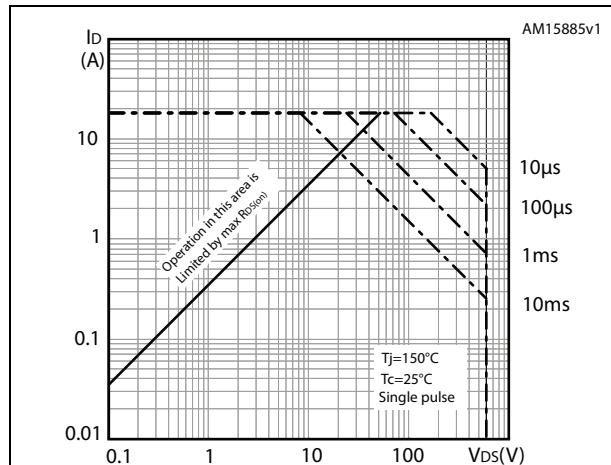


Figure 5. Thermal impedance for TO-220

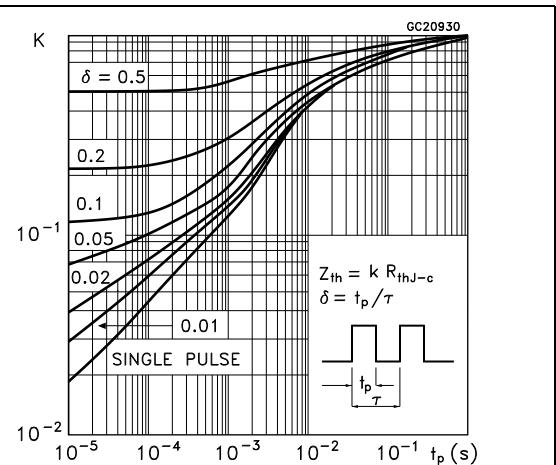


Figure 6. Safe operating area for IPAK

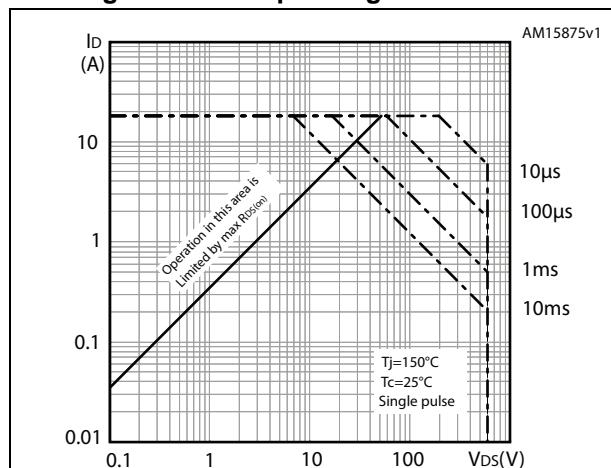


Figure 7. Thermal impedance for IPAK

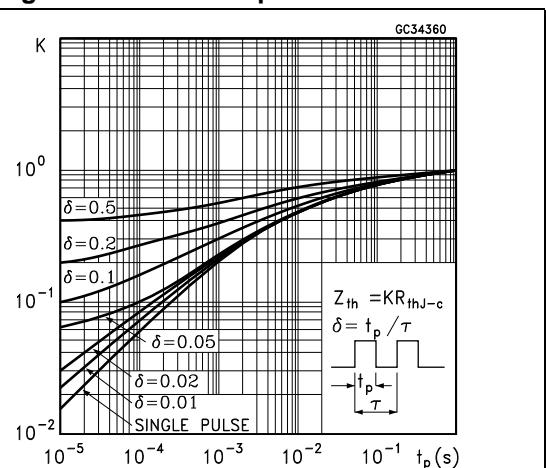


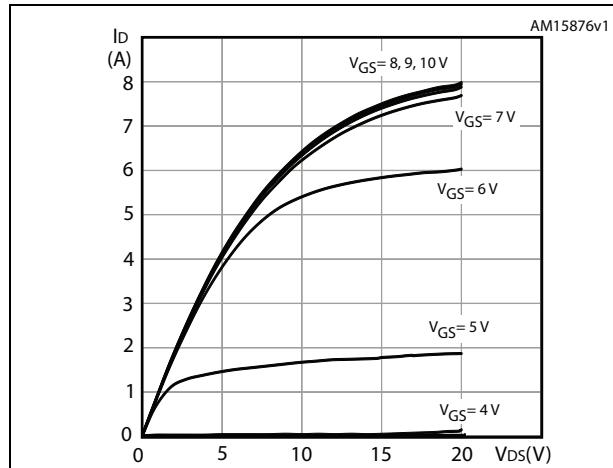
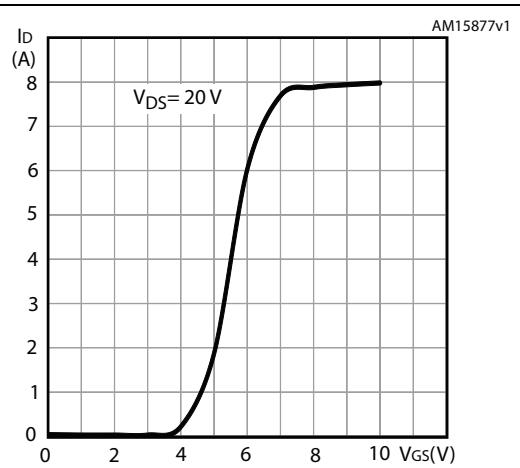
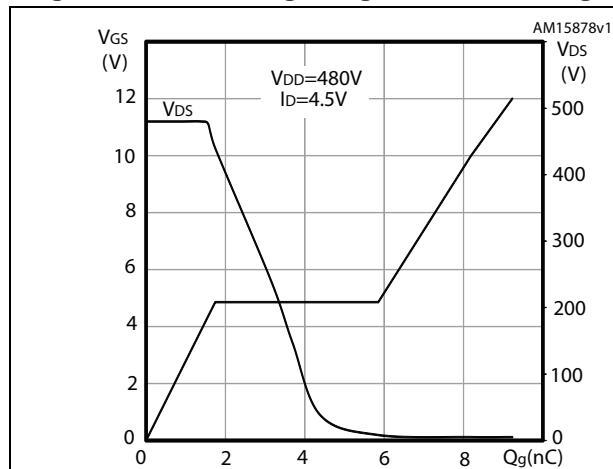
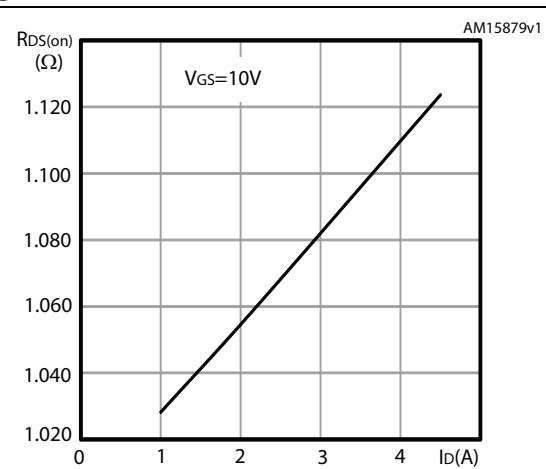
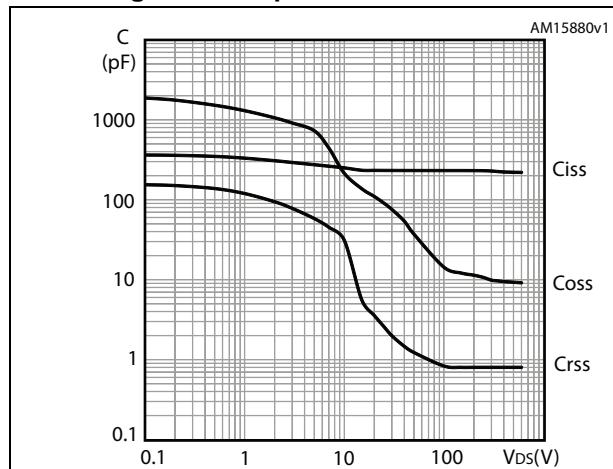
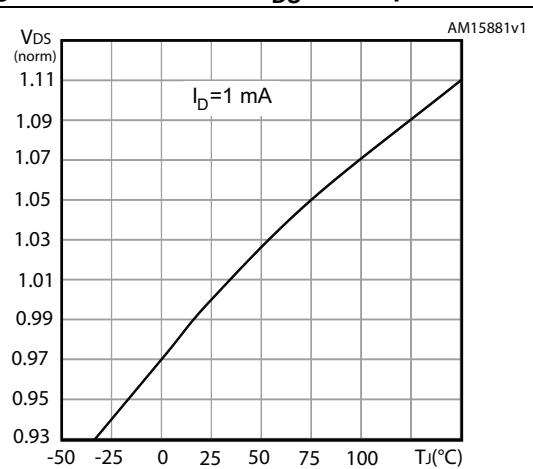
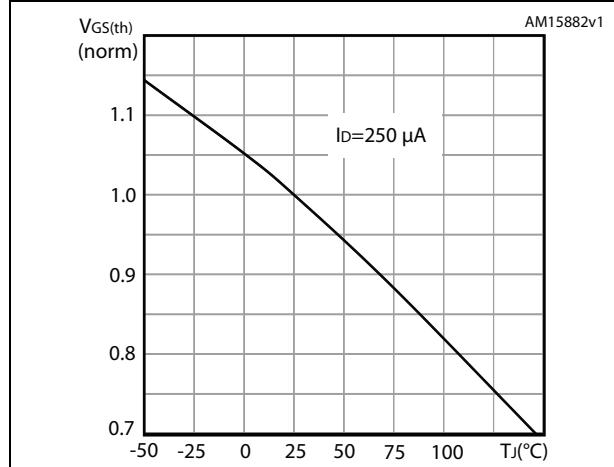
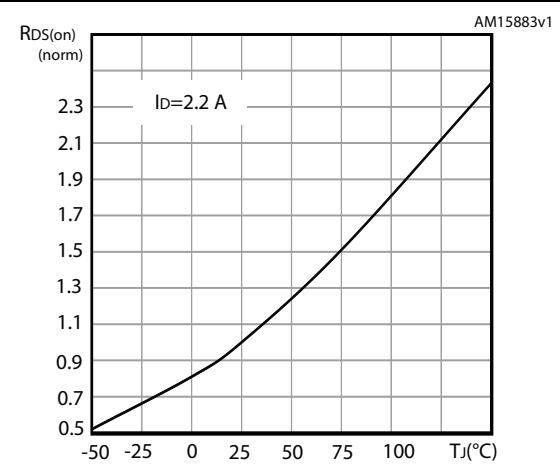
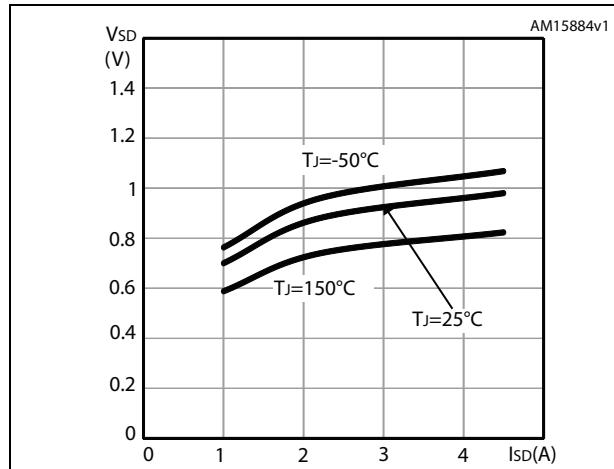
Figure 8. Output characteristics**Figure 9. Transfer characteristics****Figure 10. Gate charge vs gate-source voltage****Figure 11. Static drain-source on-resistance****Figure 12. Capacitance variations****Figure 13. Normalized V_{DS} vs temperature**

Figure 14. Normalized gate threshold voltage vs temperature**Figure 15. Normalized on-resistance vs temperature****Figure 16. Source-drain diode forward characteristics**

3 Test circuits

Figure 17. Switching times test circuit for resistive load



Figure 18. Gate charge test circuit

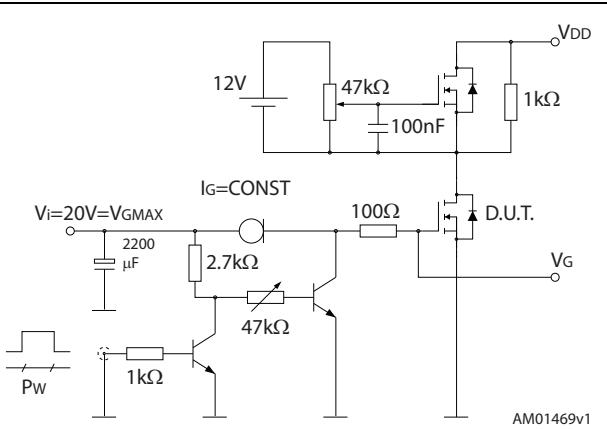


Figure 19. Test circuit for inductive load switching and diode recovery times



Figure 20. Unclamped inductive load test circuit

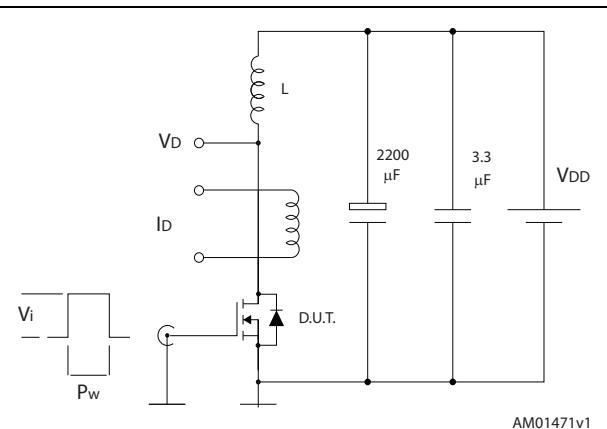


Figure 21. Unclamped inductive waveform

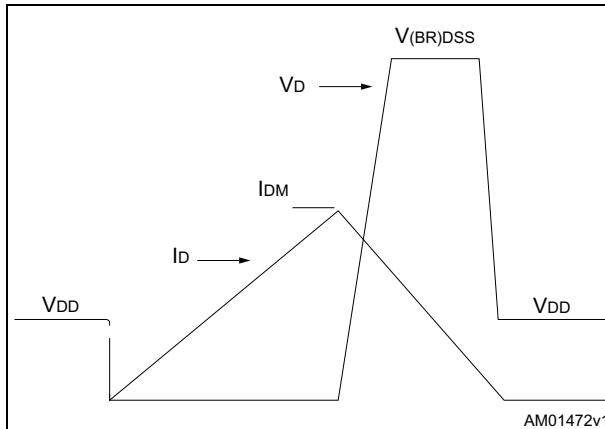
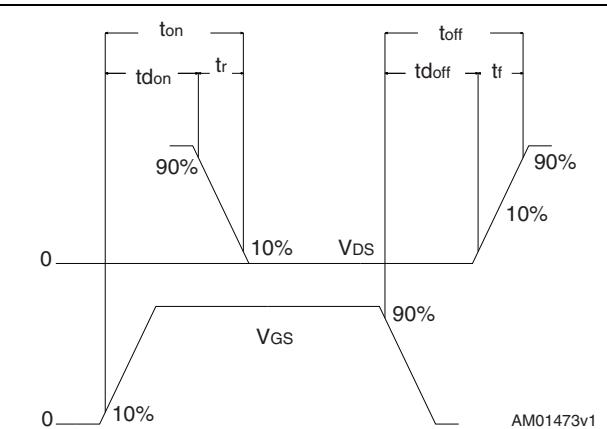


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
ECOPACK® is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing

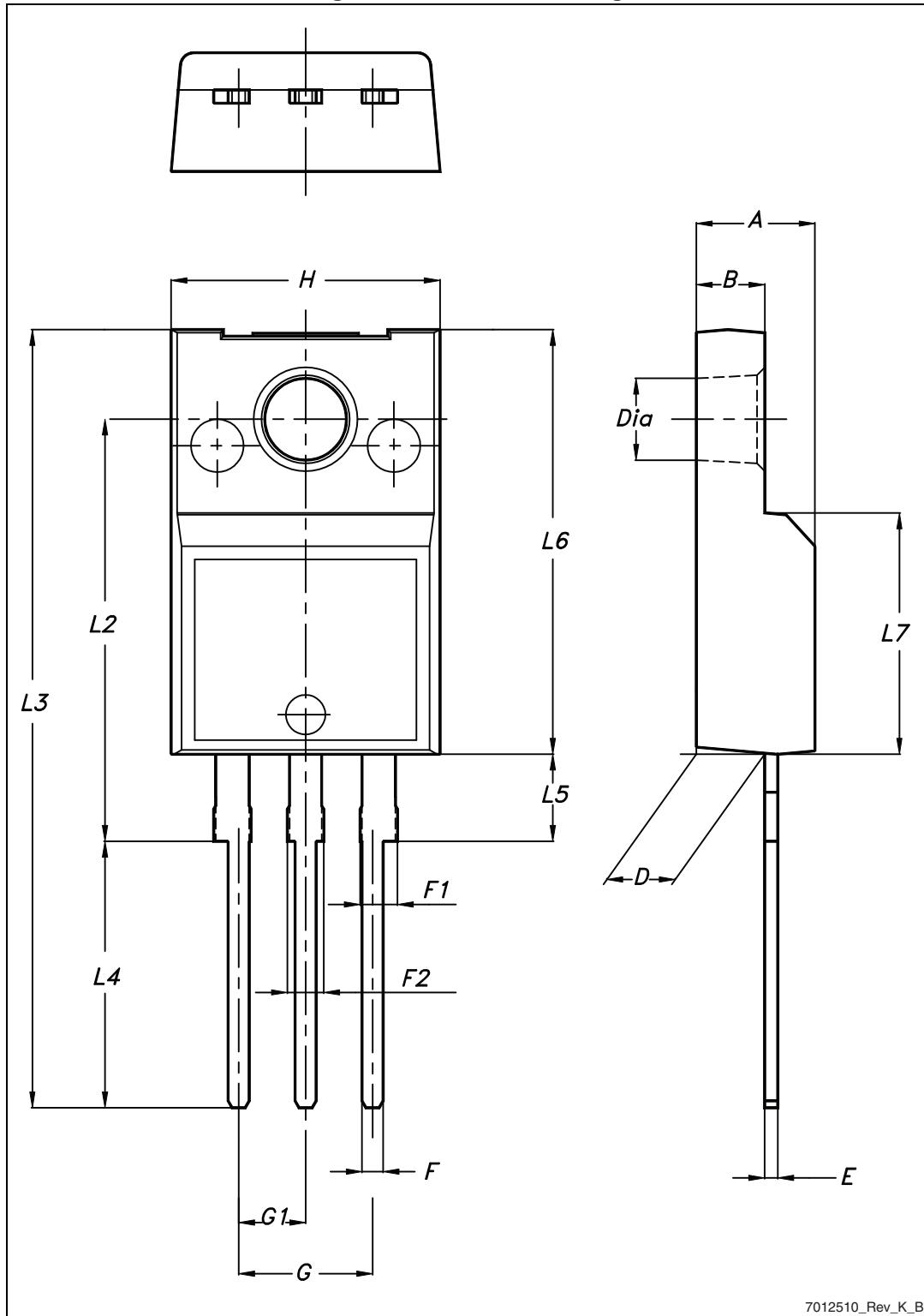


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220 type A drawing

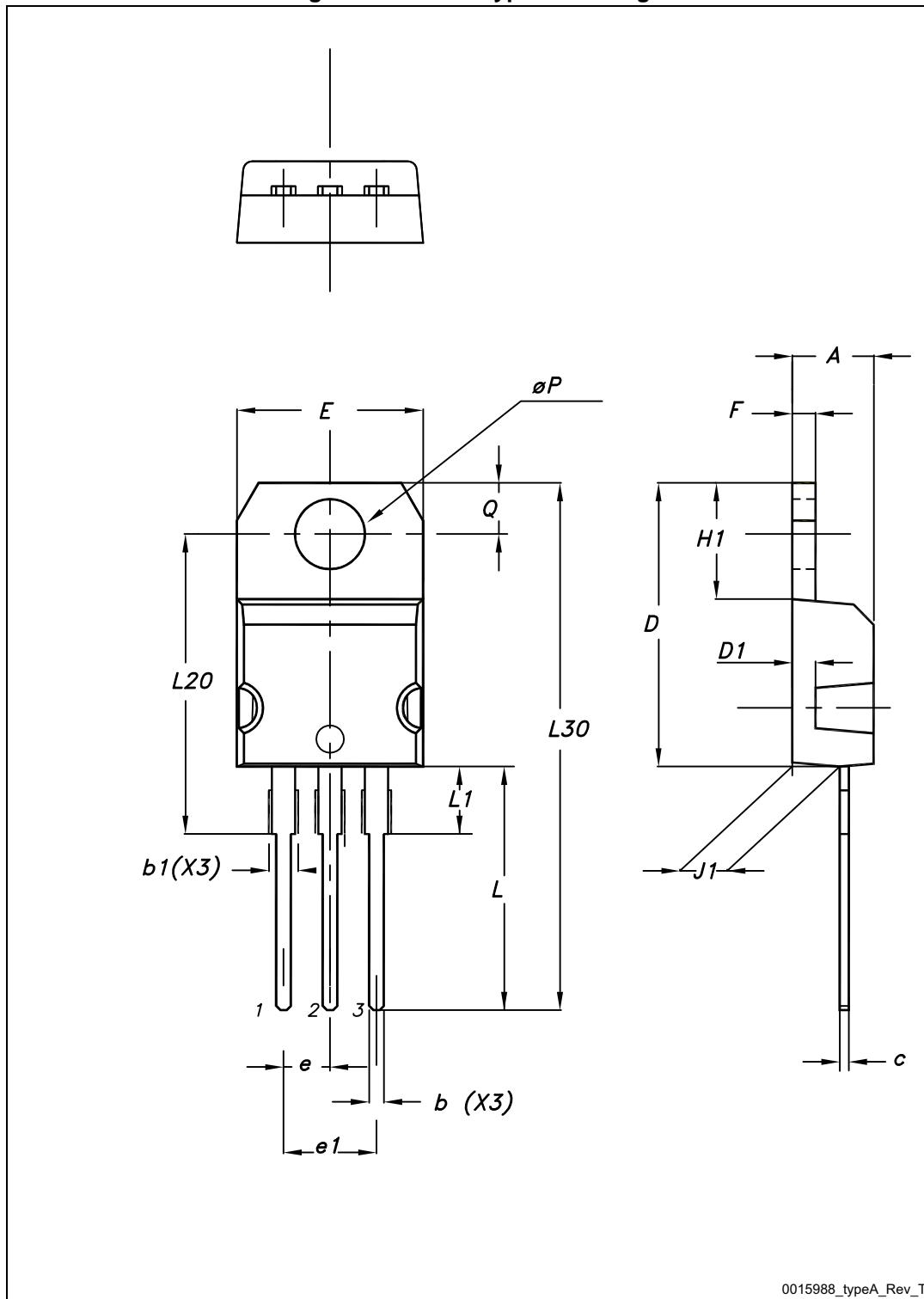
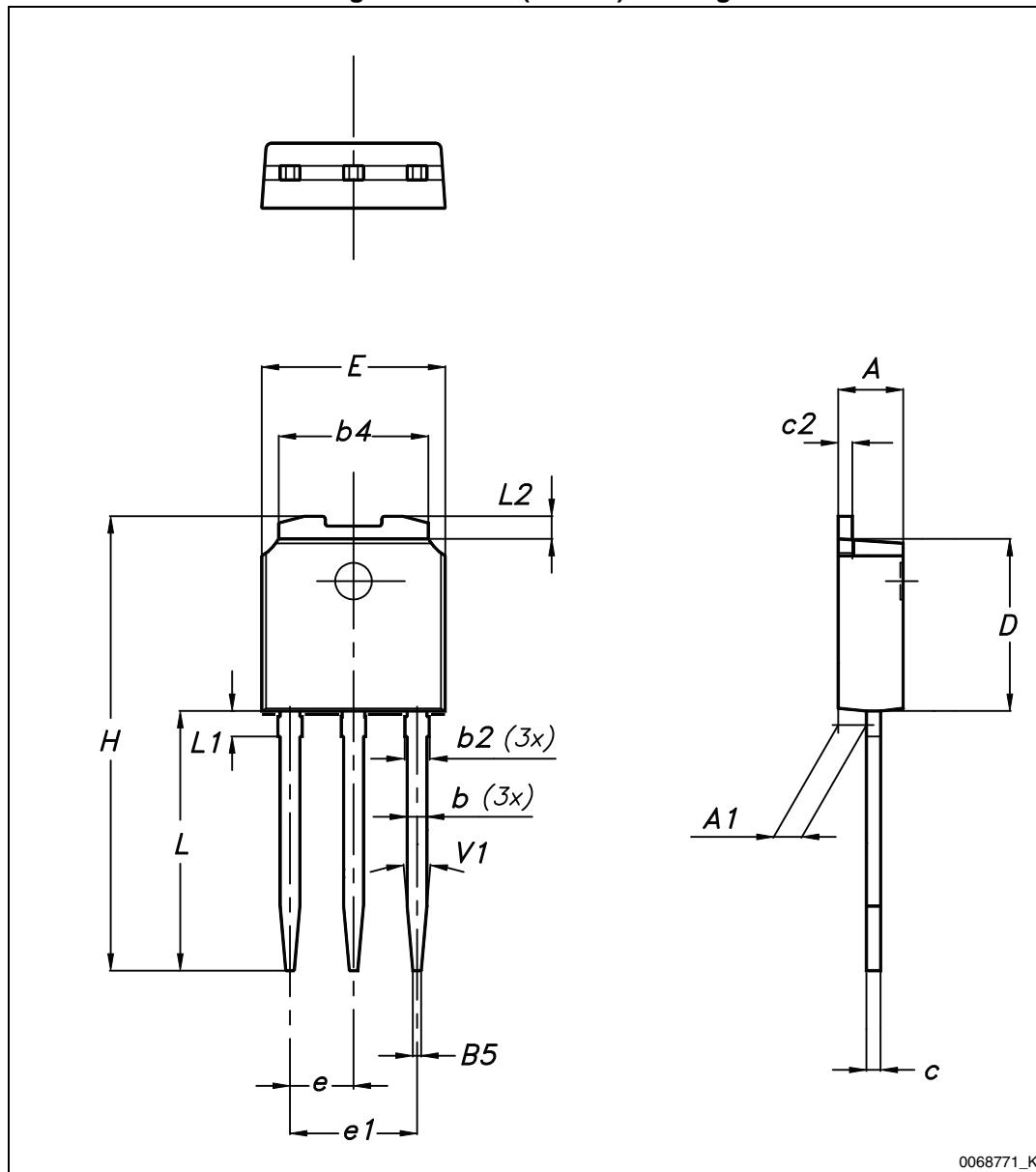


Table 11. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 25. IPAK (TO-251) drawing



5 Revision history

Table 12. Document revision history

Date	Revision	Changes
11-Jun-2013	1	First release.

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