DMC5610N

Silicon NPN epitaxial planar type

For digital circuits

■ Features

- High forward current transfer ratio h_{FE}
- Low collector-emitter saturation voltage $V_{CE(sat)}$
- Halogen-free / RoHS compliant
  (EU RoHS / UL-94 V-0 / MSL: Level 1 compliant)

■ Marking Symbol: S6

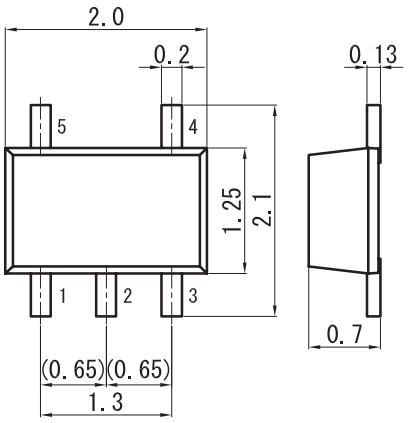
■ Basic Part Number

Dual DRC2143Z (Common emitter)

■ Packaging

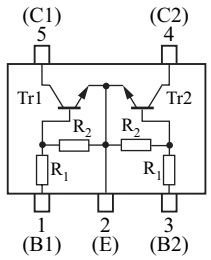
DMC5610N0R Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

Unit: mm



1: Base (Tr1) 4: Collector (Tr2)
2: Emitter (Common) 5: Collector (Tr1)
3: Base (Tr2)

Panasonic	SMini5-F3-B
JEITA	SC-113CB
Code	SOT-353



Resistance value	R_1	4.7	kΩ
	R_2	47	kΩ

■ Absolute Maximum Ratings $T_a = 25°C$

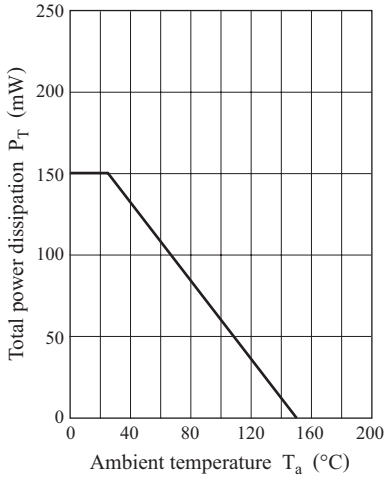
Parameter		Symbol	Rating	Unit
Tr1 Tr2	Collector-base voltage (Emitter open)	V_{CBO}	50	V
	Collector-emitter voltage (Base open)	V_{CEO}	50	V
	Collector current	I_C	100	mA
Overall	Total power dissipation	P_T	150	mW
	Junction temperature	T_j	150	°C
	Operating ambient temperature	T_{opr}	–40 to +85	°C
	Storage temperature	T_{stg}	–55 to +150	°C

■ Electrical Characteristics $T_a = 25°C \pm 3°C$

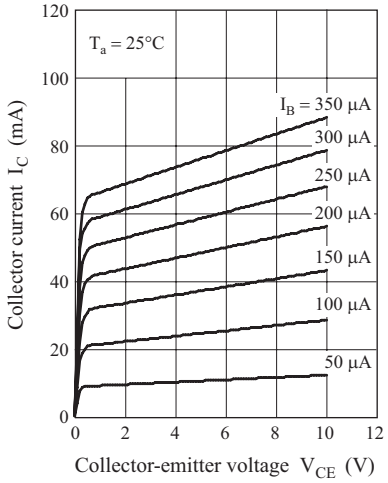
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = 10\ \mu A$, $I_E = 0$	50			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = 2$ mA, $I_B = 0$	50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 50$ V, $I_E = 0$			0.1	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = 50$ V, $I_B = 0$			0.5	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = 6$ V, $I_C = 0$			0.2	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = 10$ V, $I_C = 5$ mA	80		400	—
h_{FE} ratio *1	h_{FE} (Small/Large)	$V_{CE} = 10$ V, $I_C = 5$ mA	0.50	0.99		—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 10$ mA, $I_B = 0.5$ mA			0.25	V
Input voltage (ON)	$V_{I(on)}$	$V_{CE} = 0.2$ V, $I_C = 5$ mA	1.3			V
Input voltage (OFF)	$V_{I(off)}$	$V_{CE} = 5$ V, $I_C = 100\ \mu A$			0.4	V
Input resistance	R_1		–30%	4.7	+30%	kΩ
Resistance ratio	R_1 / R_2		0.08	0.10	0.12	—

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *1: Ratio between 2 elements

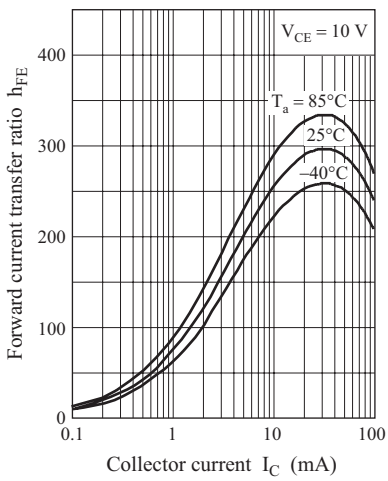
P_T — T_a



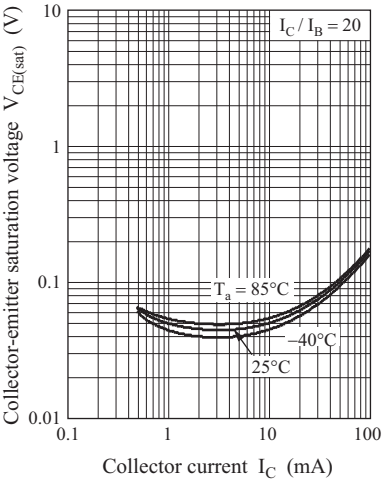
I_C — V_{CE}



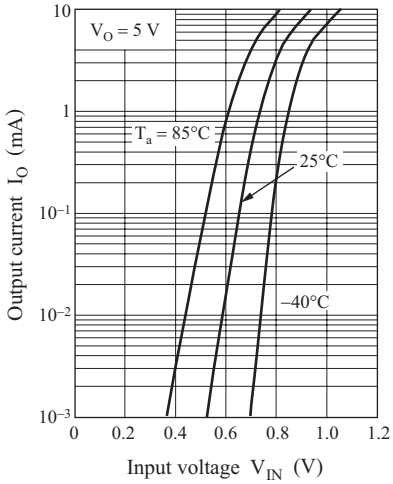
h_{FE} — I_C



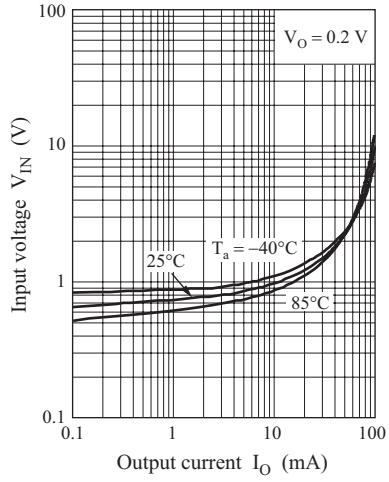
$V_{CE(sat)}$ — I_C



I_O — V_{IN}

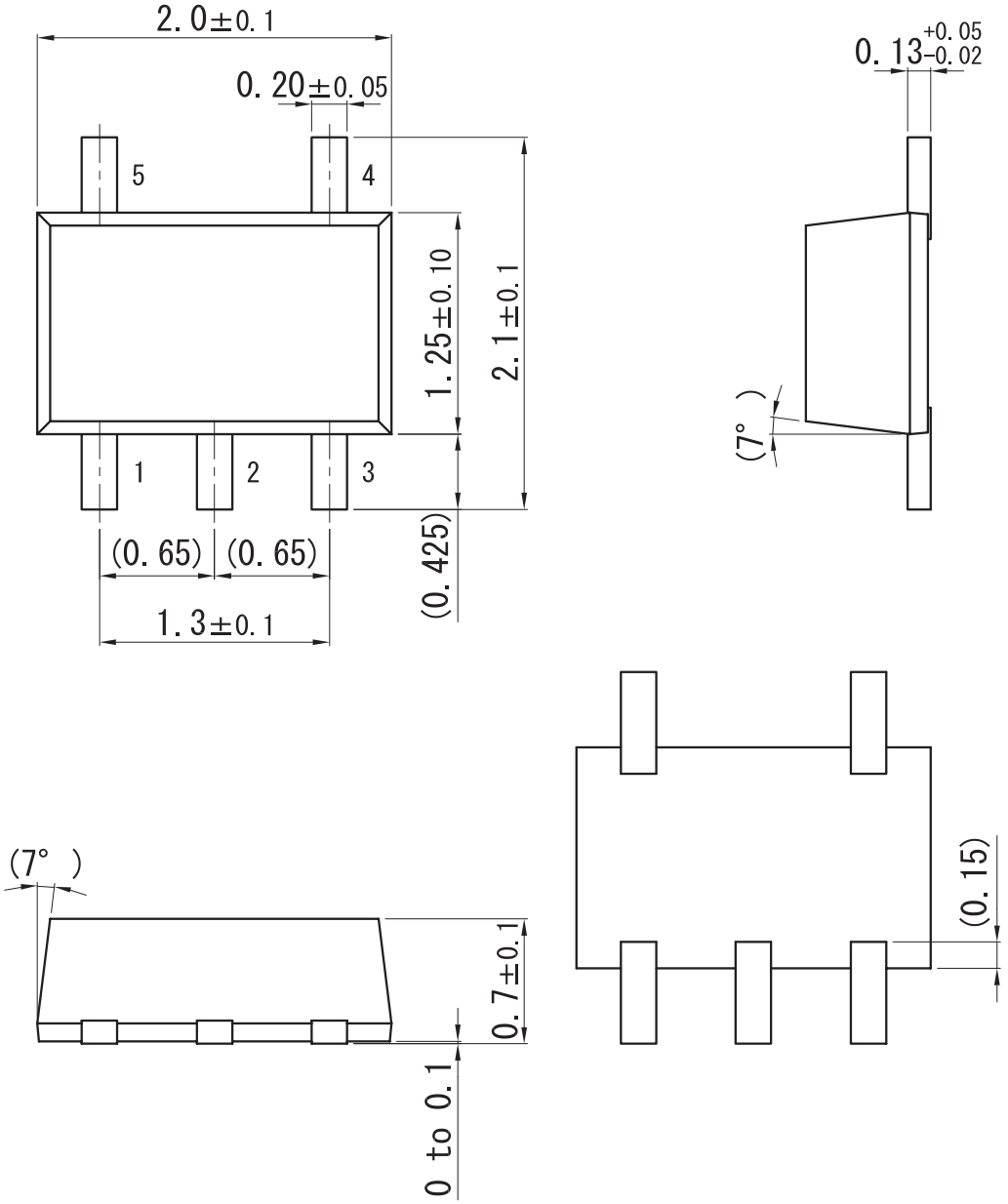


V_{IN} — I_O

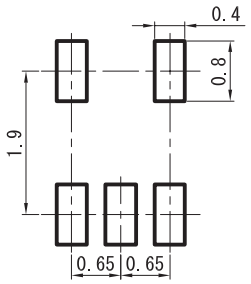


SMini5-F3-B

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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