

30V N-CHANNEL ENHANCEMENT MODE MOSFET WITH SCHOTTKY DIODE POWERDI®

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	Package	I_D $T_A = +25^\circ\text{C}$
30V	10mΩ @ $V_{GS} = 10\text{V}$	POWERDI 3333-8	12A
	15mΩ @ $V_{GS} = 4.5\text{V}$		9.5A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

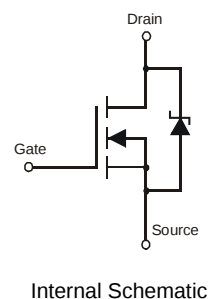
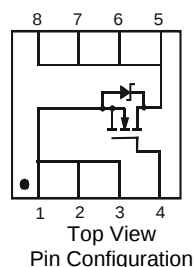
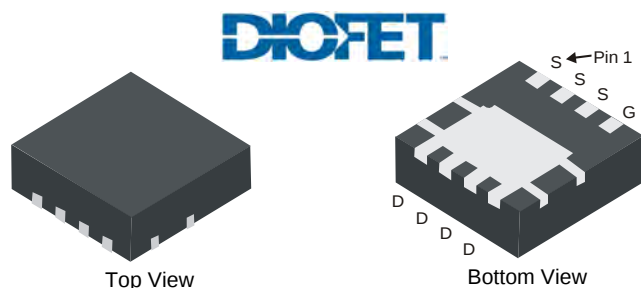
- Backlighting
- Power Management Functions
- DC-DC Converters

Features

- DIOFET utilizes a unique patented process to monolithically integrate a MOSFET and a Schottky in a single die to deliver:
 - Low $R_{DS(ON)}$ – minimize conduction losses
 - Low V_{SD} – reducing the losses due to body diode conduction
 - Low Q_{rr} – lower Q_{rr} of the integrated Schottky reduces body diode switching losses
 - Low gate capacitance (Q_g/Q_{gs}) ratio – reduces risk of shoot through or cross conduction currents at high frequencies
- Small form factor thermally efficient package enables higher density end products
- Occupies just 33% of the board area occupied by SO-8 enabling smaller end product
- 100% UIS (Avalanche) rated
- 100% Rg tested
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: POWERDI3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish - Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 
- Weight: 0.072 grams (approximate)

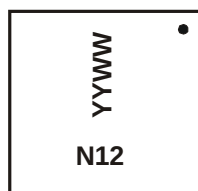


Ordering Information (Note 4)

Part Number	Case	Packaging
DMS3012SFG-7	POWERDI3333-8	2000/Tape & Reel
DMS3012SFG-13	POWERDI3333-8	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



N12 = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last digit of year (ex: 11 = 2011)
 WW = Week code (01 ~ 53)

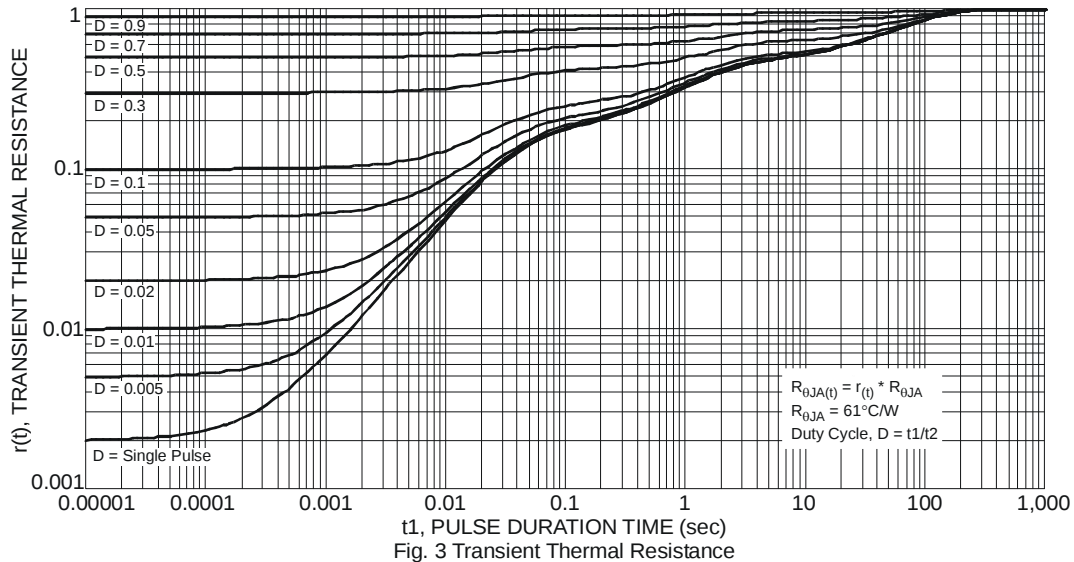
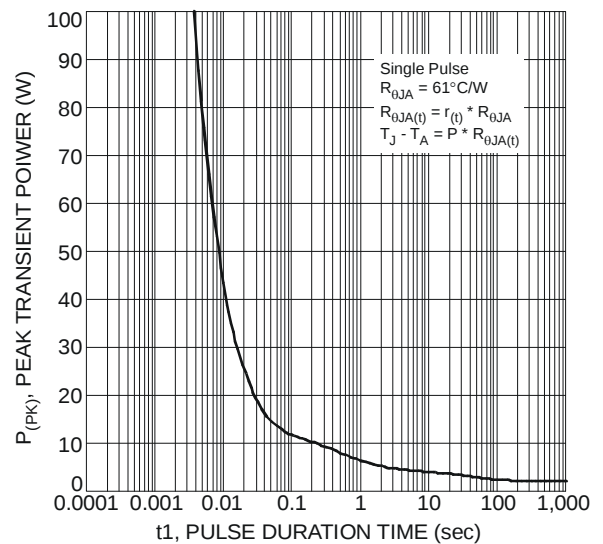
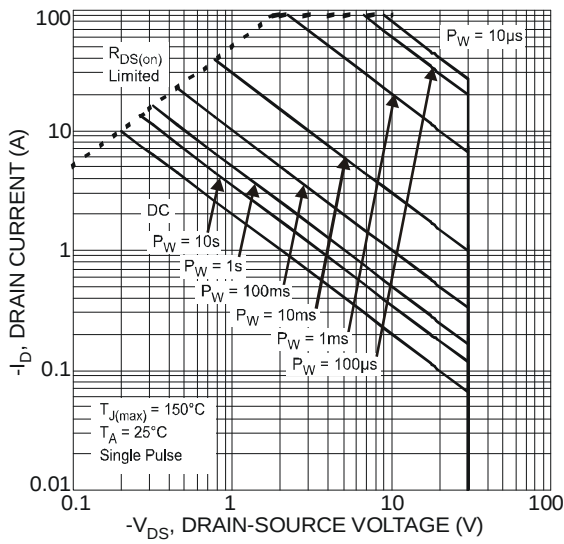
Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C T _A = +70°C	I _D	12 9.5	A
	t < 10s	T _A = +25°C T _A = +70°C	I _D	16.0 12.7	A
Continuous Drain Current (Note 6) V _{GS} = 4.5V	Steady State	T _A = +25°C T _A = +70°C	I _D	9.5 7.5	A
	t < 10s	T _A = +25°C T _A = +70°C	I _D	13.0 10.3	A
Pulsed Drain Current (10μs pulse, duty cycle = 1%)			I _{DM}	90	A
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	3.5	A
Avalanche Current (Note 7) L = 0.1mH			I _{AR}	17	A
Repetitive Avalanche Energy (Note 7) L = 0.1mH			E _{AR}	43	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	T _A = +25°C	P _D	0.89	W
	T _A = +70°C		0.55	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	R _{θJA}	145	°C/W
	t < 10s		74	
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	2.2	W
	T _A = +70°C		1.3	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	58	°C/W
	t < 10s		31	
Thermal Resistance, Junction to Case (Note 6)		R _{θJC}	11	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

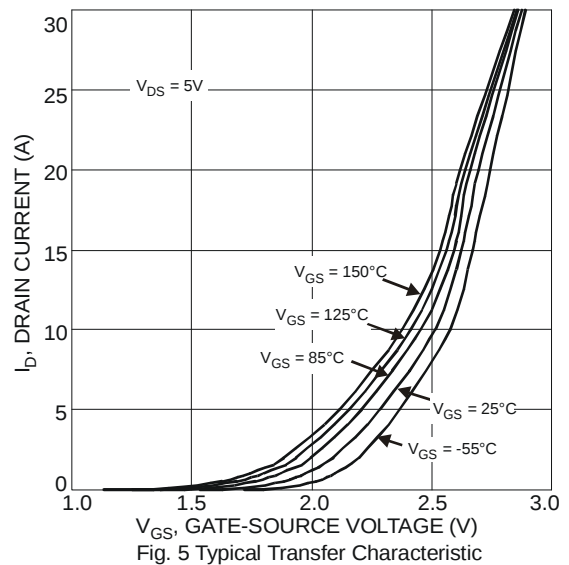
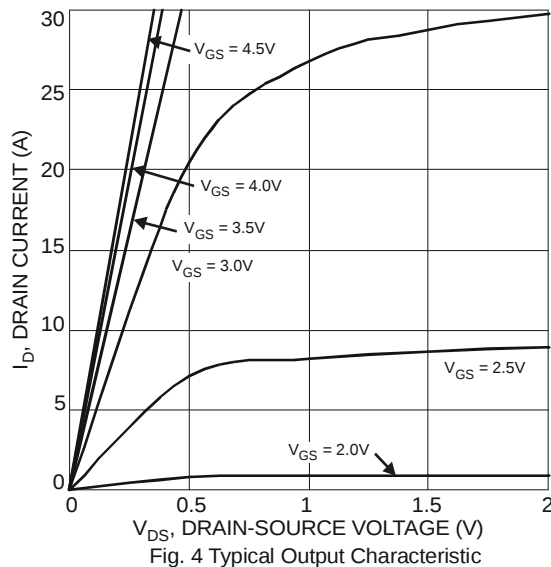
Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 7. I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep T_J = +25°C

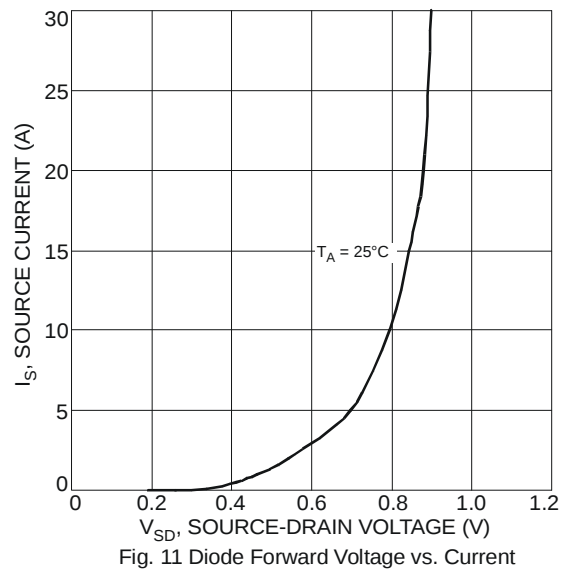
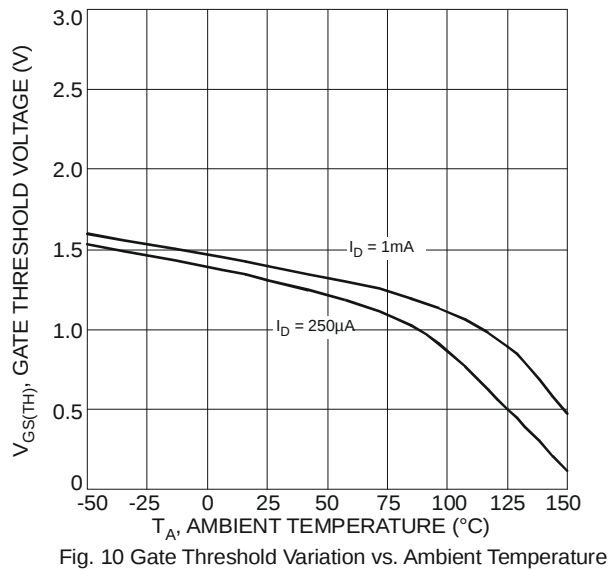
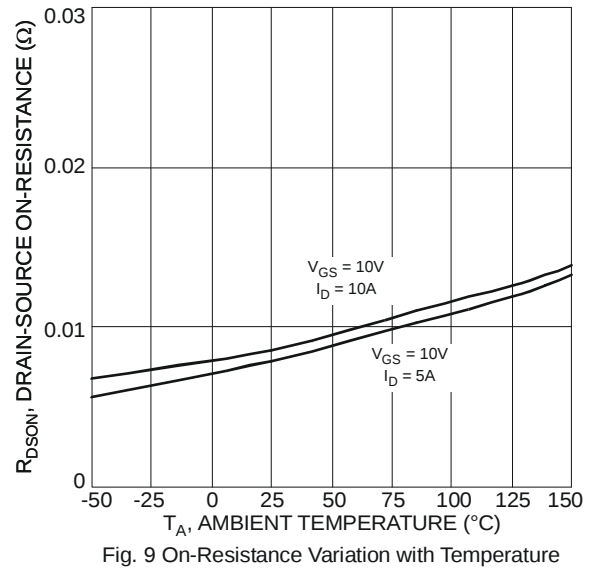
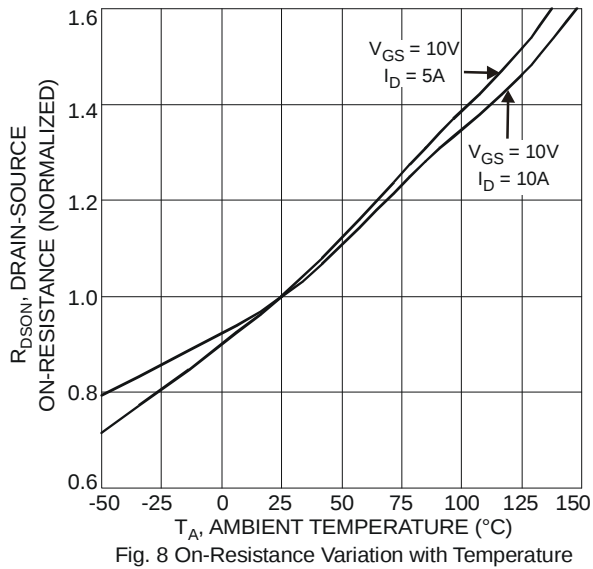
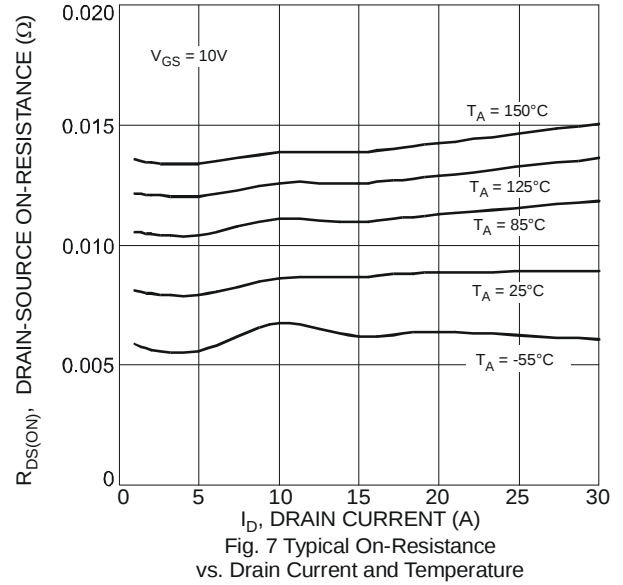
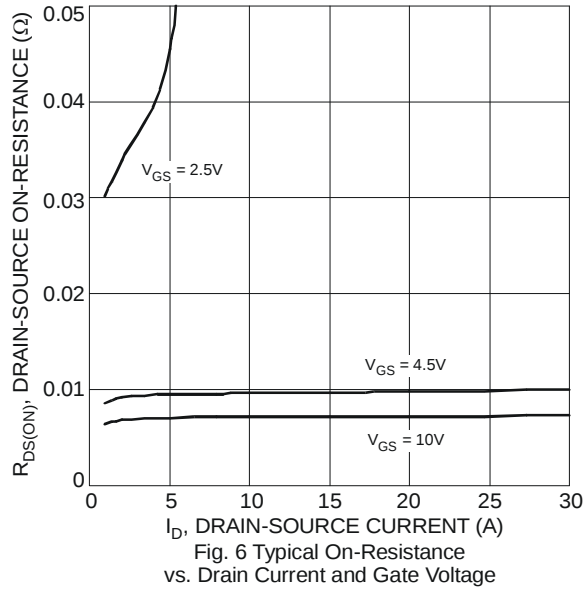


Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	100	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	1.0	1.5	2.5	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	7.3	10	mΩ	V _{GS} = 10V, I _D = 13.5A
		—	10	15		V _{GS} = 4.5V, I _D = 11A
Forward Transfer Admittance	Y _{fs}	—	30	—	S	V _{DS} = 5V, I _D = 10.0A
Diode Forward Voltage	V _{SD}	—	0.45	0.55	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	1296	4310	pF	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	415	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	204	—	pF	
Gate Resistance	R _g	0.26	1.6	2.6	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge V _{GS} = 4.5V	Q _g	—	14.7	—	nC	V _{DS} = 15V, V _{GS} = 10V, I _D = 13.5A
Total Gate Charge V _{GS} = 10V	Q _g	—	31.6	—	nC	
Gate-Source Charge	Q _{gs}	—	3.5	—	nC	
Gate-Drain Charge	Q _{gd}	—	5.0	—	nC	
Turn-On Delay Time	t _{D(on)}	—	15.8	—	ns	V _{GS} = 10V, V _{DS} = 15V, R _G = 3Ω, I _D = 8.8A
Turn-On Rise Time	t _r	—	27.8	—	ns	
Turn-Off Delay Time	t _{D(off)}	—	29.7	—	ns	
Turn-Off Fall Time	t _f	—	13.6	—	ns	
Reverse Recovery Time	t _{rr}	—	13.1	—	ns	I _F = 13.5A, di/dt = 100A/μs
Reverse Recovery Charge	Q _{rr}	—	4.3	—	nC	I _F = 13.5A, di/dt = 100A/μs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.





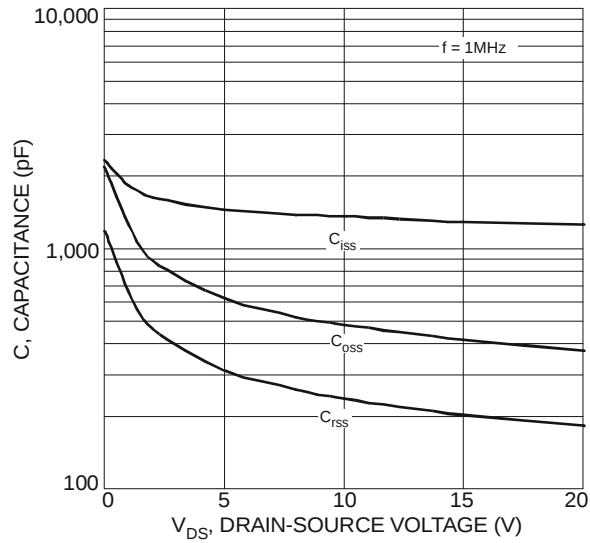


Fig. 12 Typical Total Capacitance

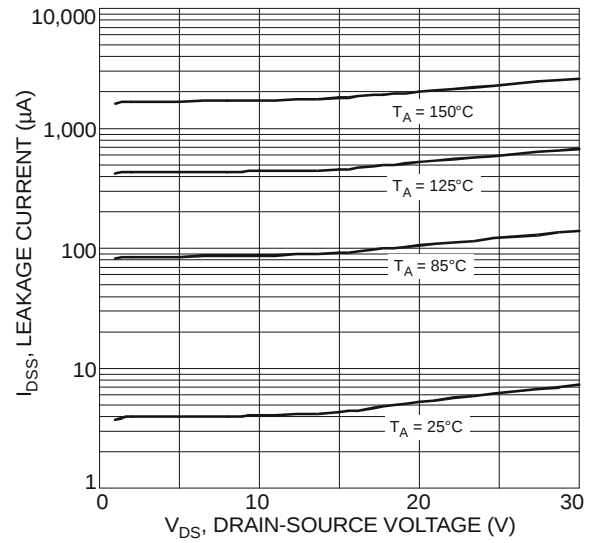


Fig. 13 Typical Leakage Current vs. Drain-Source Voltage

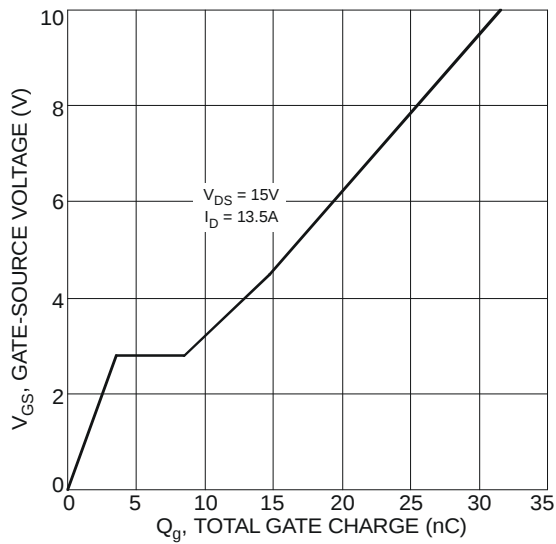
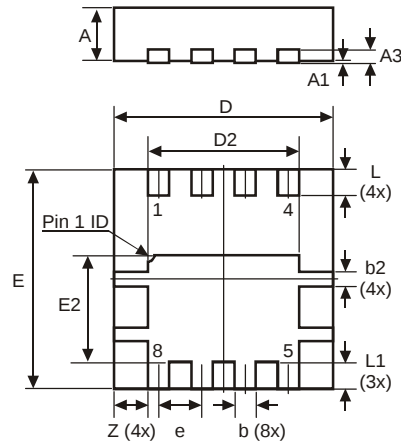


Fig. 14 Gate-Source Voltage vs. Total Gate Charge

Package Outline Dimensions

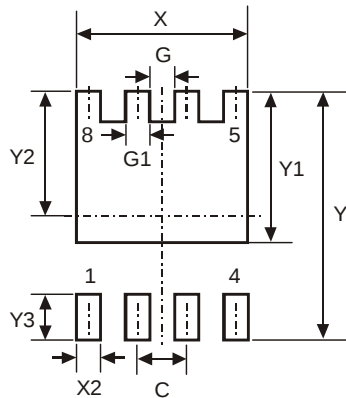
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



POWERDI3333-8			
Dim	Min	Max	Typ
D	3.25	3.35	3.30
E	3.25	3.35	3.30
D2	2.22	2.32	2.27
E2	1.56	1.66	1.61
A	0.75	0.85	0.80
A1	0	0.05	0.02
A3	—	—	0.203
b	0.27	0.37	0.32
b2	—	—	0.20
L	0.35	0.45	0.40
L1	—	—	0.39
e	—	—	0.65
Z	—	—	0.515
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.650
G	0.230
G1	0.420
Y	3.700
Y1	2.250
Y2	1.850
Y3	0.700
X	2.370
X2	0.420

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