Thursday 25 August, 2005/POrrell

Evaluation Board for Fractional-N PLL Frequency Synthesizer

Evaluation Board Tech Note

EVAL-ADF4193EB2

FEATURES

Self-Contained Board Including Synthesizer
User selectable VCO
Dual VCO footprint allows flexible choice of VCO
Accompanying Software Allows Complete Control of Synthesizer Functions from PC
ADIsimPLL files assist user to design own loop filter
Requires external 9V supply
Typical Phase Noise Performance of -103 dBc/Hz @ 1 kHz Offset from Carrier

GENERAL DESCRIPTION

This board is designed to allow the user to evaluate the performance of the ADF4193 Frequency Synthesizer for PLL's (Phase Locked Loops). The board is shown below. It contains the ADF4193 synthesizer, a PC connector, and input for the reference input, SMA connectors RF output and 4mm connectors for the 9V supply.

The evaluation board does not have a VCO or loop filter. These must be selected, designed and fitted to the board by the user. If the user needs a complete solution then the Eval ADF4193 EB1 is a more suitable

A cable is included with the board to connect to a pc printer port.

The package also contains windows software (2000 and XP compatible) to allow easy programming of the synthesizer.

ADF4193 Evaluation Board

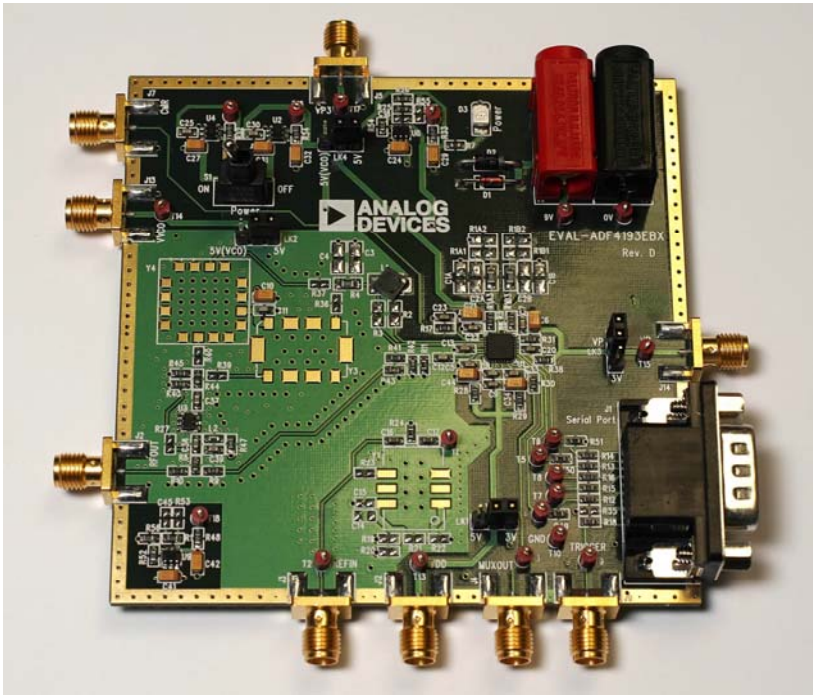

Figure 1.

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Fax: 781.326.8703

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HARDWARE

OVERVIEW

The evaluation board comes with a cable for connecting to the printer port of a PC. An external power supply of 9V is needed and an external reference is needed An RF source of 104MHz with an amplitude of 5dBm would be suitable. Lower frequencies can be used if the reference slew rate is met. Please consult the datasheet

The evaluation board has the flexibility to accept an alternative VCO footprint if the user wishes.

The cable diagram for the evaluation board is shown below. The board schematic is shown on pages 4 and 5.

POWER SUPPLIES

The board is powered from a single 9V battery. The power supply circuitry allows the user to choose different voltages for Vdd and the VCO supply

On the board there are 4 jumper settings which are used to configure the various power supply options. The default settings are as follows:-

LK1= 3V (Vdd supply)

LK2= 5V(VCO) (VCO supply)

LK3= 5V (Vp supply)

LK4= 5V (Differential Amplifier Supply)

The EV board is switched on with the on/off power switch

VCO CHOICES

The evaluation board can except two industry standard VCOs with different footprint. These VCOs are labelled Y4 and Y3. If Y4 footprint (“The square one”) is used then 0 ohms resistors R40 and R37 must be fitted with R44 and R36 omitted. This is the default setting. If Y3 footprint is used then R44 and R36 must be 0 ohms with R40 and R37 omitted

LOCAL OSCILLATOR COMPONENTS

All components necessary for Local Oscillator (LO) generation are included on the board. An SMA connector is provided for the Reference Input.

The user must select a VCO and design a loop filter. On the CD there is a tech note to aid this design, and also the ADF4193 is fully supported in simPLL v2.7 and later

The output is available at RFOUT through a standard SMA connector. Note that an external REFIN is required.

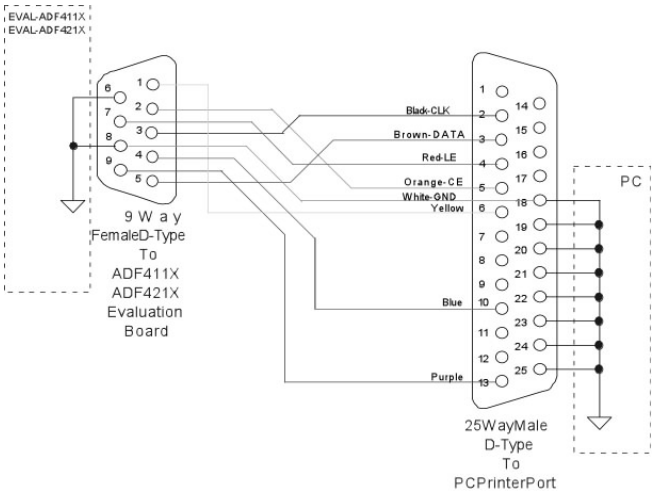

Figure 3. PC Cable Diagram

SCHEMATICS

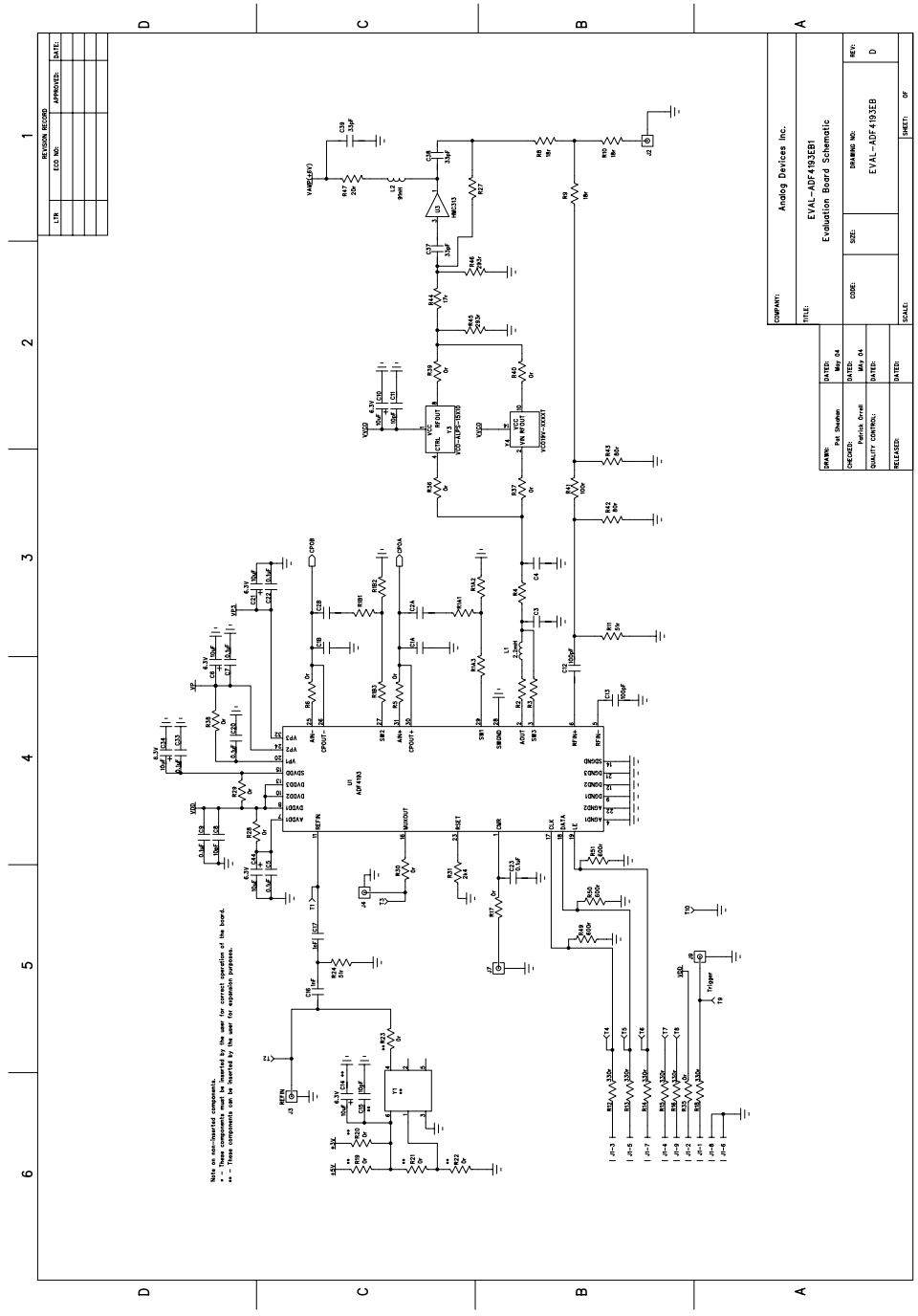

Figure 4. Evaluation Board Schematic (Page 1)

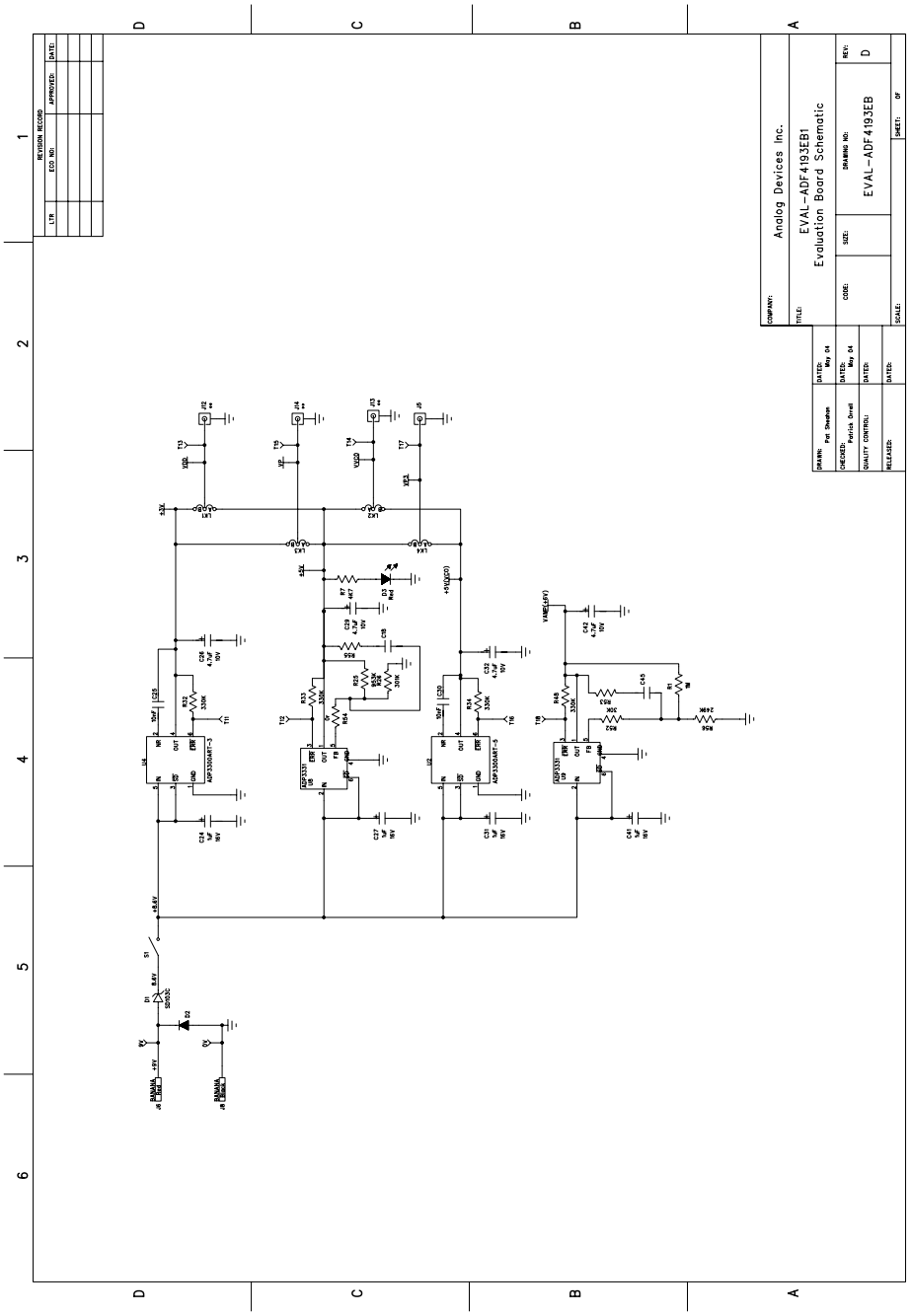

Figure 5. Evaluation Board Schematic (Page 2)

BILL OF MATERIALS

This is the same as the ADF4193 EB1 but with the following components removed. Y4 (VCO) ,R37,R40(zero ohm links), C1A,C2A,C2B,C1B (loop filter caps) The EB2 needs a loop filter and VCO added to make a complete system. Refer to the data sheet and tech notes on the CD.

Please refer to CD for EB1 tech note for full BOM

TEST SET UP

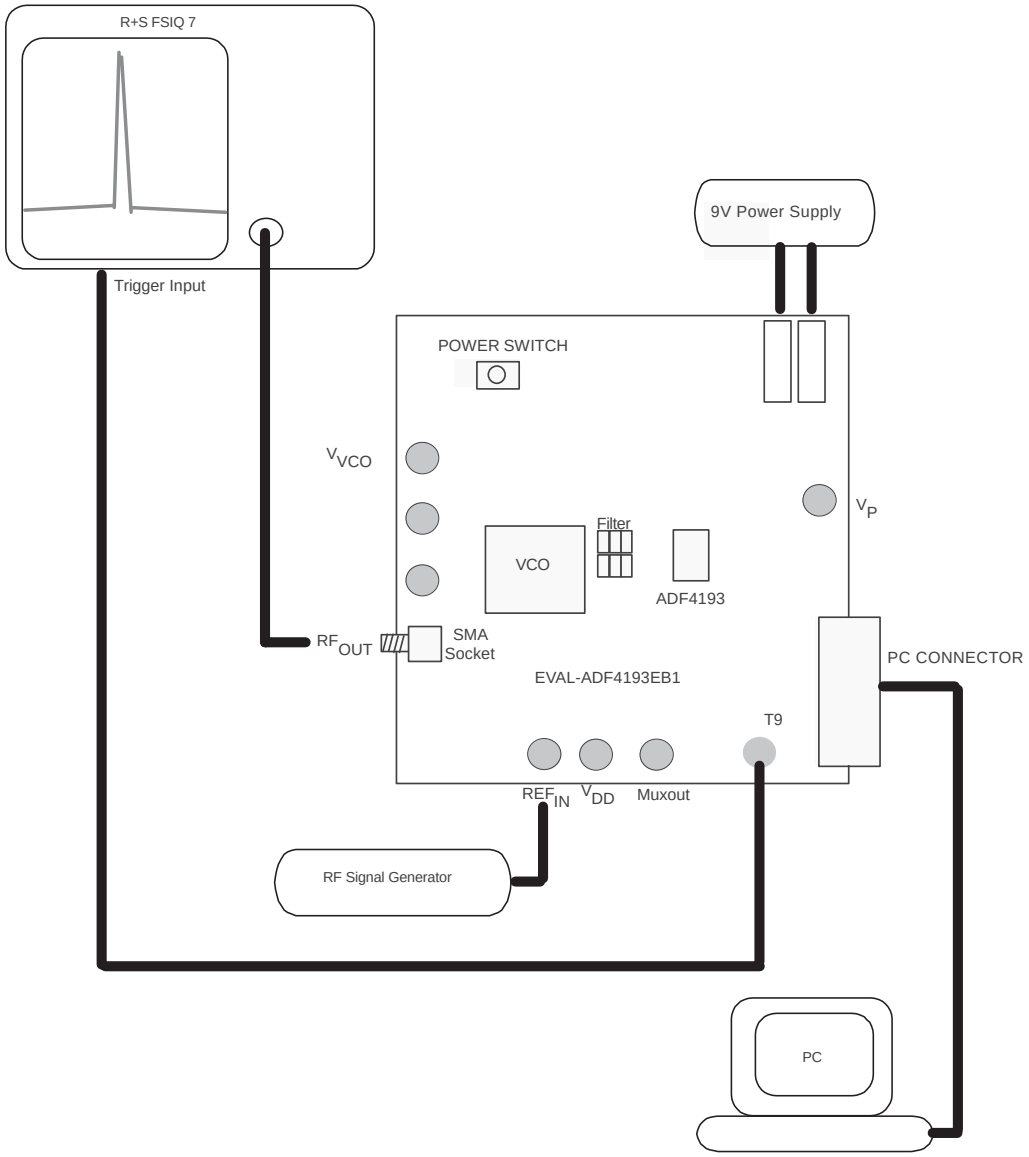

Figure 6. Test Set Up

SOFTWARE

INSTALLATION

The control software for EVAL-ADF4193EB1 is on the CD which accompanies the board.

STEP 1: There are the required phase codes on the CD for optimal lock time and spurious. **These are located in the directory \Phase_Codes. on the CD. They must be manually copied onto the host computer in the directory of choice**

The phase codes included on the CD are as follows

gsm1800tx_phase_codes.txt: -ADF4193EB1 eval board and GSM 1800 TX systems

gsm1800rx_phase_codes.txt: GSM 1800 RX systems

gsm900tx_phase_codes.txt: GSM 900 TX systems

gsm900rx_phase_codes.txt: GSM 900 RX systems

26M_60K_phase_codes.txt: Old GSM 1800 TX table for systems designed with 26MHz PFD

STEP2: On the CD run the setup.exe to start the install shield. If the install shield asks to modify the installation chose remove and run the setup.exe again.

RUNNING THE PROGRAM

Choose the ADF4193 program from the Start Menu. located under the Analog Devices menu. The program is **called ADF4193 Rev 4.0** Before the main software screen appears, the user is given the choice to load a phase table or use manual settings. If manual setup is chosen then the default values for the ADF4193 EB1 will be loaded with phase values of 5 for each frequency. This will work fine but more optimal settling time and spurious results can be obtained by using the phase tables

The user then accepts his choice. The Main Interface Window will now appear (Figure 7). Note just below the Analog Devices logo the software will remind you of the file that you have loaded., or if no file is loaded at all The user must now enter the Frequency Control Section and enter the frequencies of choice. (Fig 8) and Update R0 and R1 (Normal Mode). Now exit the window and the main interface will now appear again as in Figure 7 but with the large Initialisation Sequence button now visible. Press the Initialisation Button. The light to the left of the dialogue will glow red then green(fig 9) C lick on "Update All Registers" and an RF spectrum should appear at the output.

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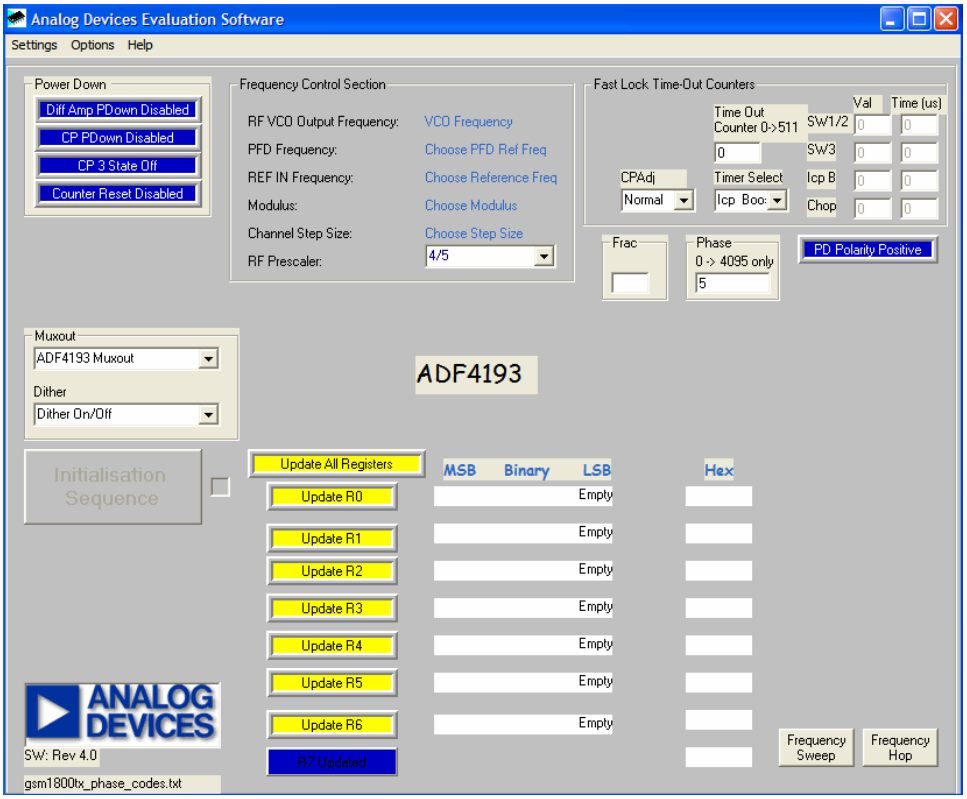


Figure 7 . Software Front Panel

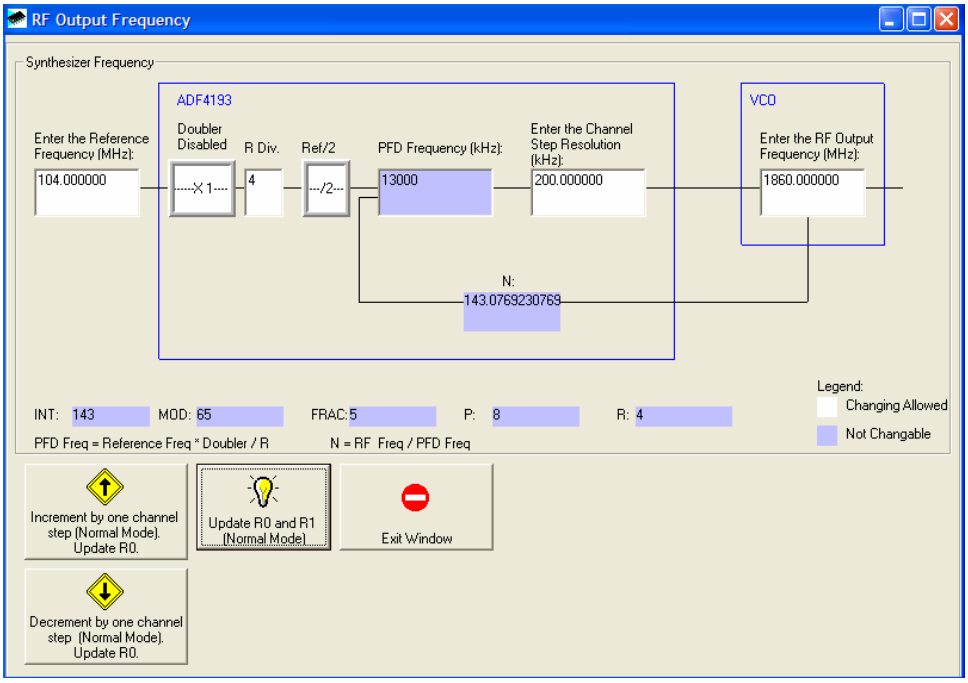


Figure 8 . RF front panel

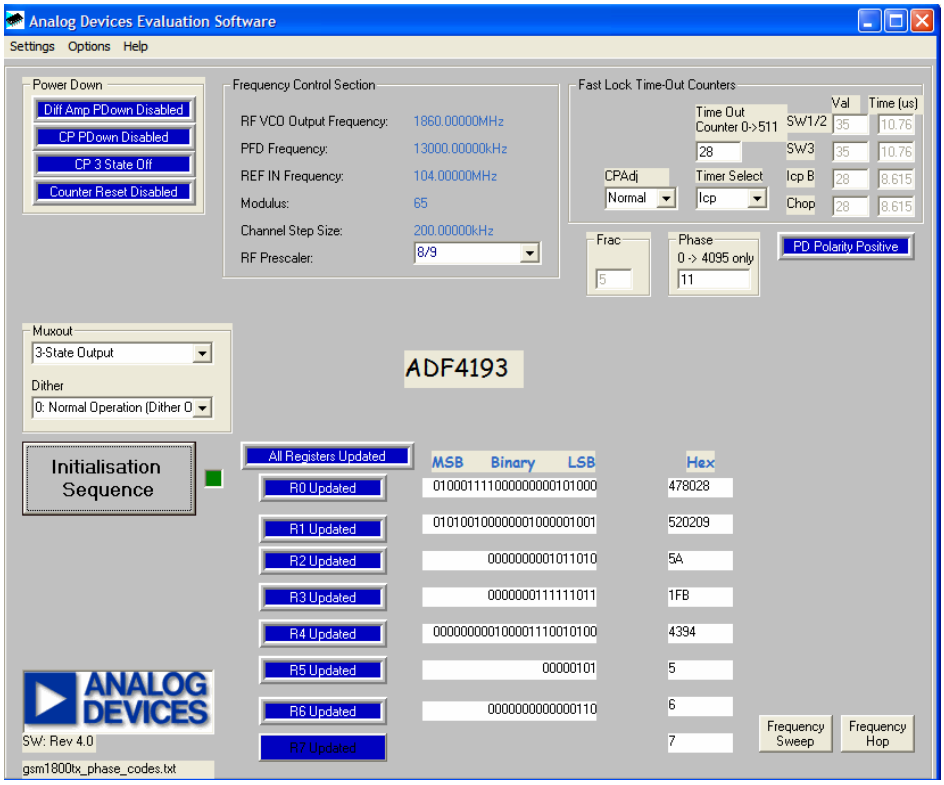
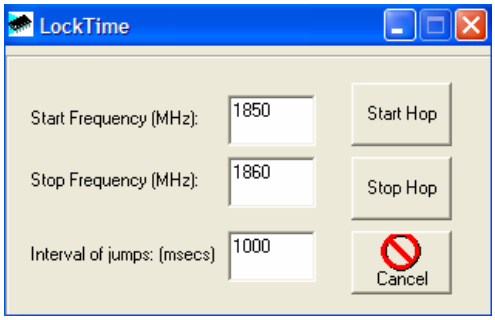


Figure 9 . Software front panel

FREQUENCY HOPPING

To frequency hop between two frequencies, click on the frequency hop button and the

following panel should appear

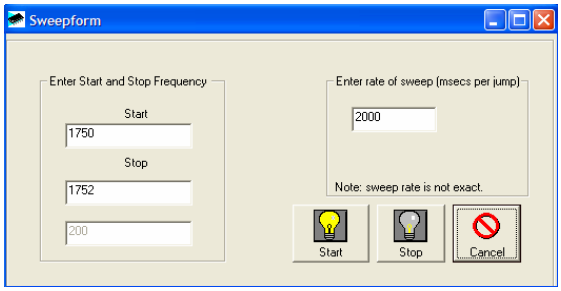


Enter start ,stop frequencies and interval of the jump in milliseconds and then click on the “start hop”. To stop the hopping click on the “stop” and then “cancel” to return to the main form. As the ADF4193 is writing to phase registers before it writes the frequency information there will be more than one LE pulse for each frequency write.

A feature of the software is an extra trigger signal from the computer to make the lock time measurements easier. This signal is a copy of the last latch enable and can be monitored on T9 on the evaluation board. The LE enable pulse can still be monitored on T6

FREQUENCY SWEEPING

To frequency sweep the user clicks on the “frequency sweep” button. The following panel should appear

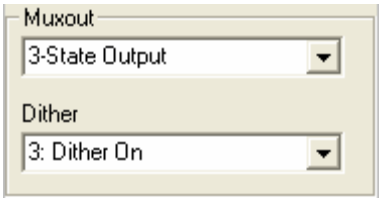


Start and stop frequencies are entered with the rate of sweep in milliseconds. The resolution of the sweep is taken from the channel already set on the main form and shown underneath the “stop” display

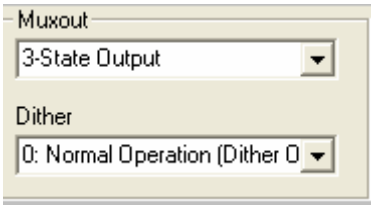
DITHER ON AND OFF

Inside the ADF4193 sigma-delta core, a technique called dithering is used to reduce spurious. When dithering is enabled the spurious power is spread over frequency and appears in the noise in the noise. As a result of the dithering there will be a slight degradation to the phase noise. Dither Off is recommended for normal use

To select dither on set the MuxOut third row to “dither on”



To switch off dither set the MuxOut third row to “Normal Operation(dither off)”



In both cases you will need to update the Register 6 and Register 2 after the dither mode has been selected. Register 2 is updated as a different phase values is used for dither off and on. The software will load Dither Off as default.

POWER DOWN PANEL

Here various parts functions of ADF4193 can be shut down eg diff amp and charge pump. Also the charge pump can be placed in tri state mode with the CP3 State Off button If you want to use an external op-amp instead of the built ADF4193 amplifier you will need to power down the diff amp.

Below are shown the default values

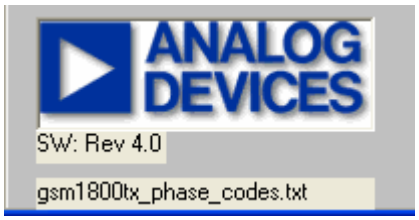
ADJUSTING THE CHARGE PUMP CURRENT (CPADJ)

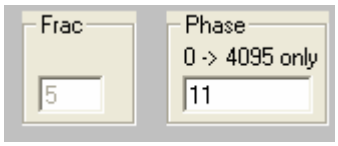
In some cases the uses may wish to use another PFD other than the recommended 13MHz or 26MHz eg 20.8MHz. In such a case to maintain the same loop bandwidth and settling time the current can be boosted by 25% by using the CPAdj toggle

After updating the toggle please update R1 to activate this setting. Please note that by decreasing the PFD you will extend the timer counter values that will have to be modified to keep the original settling time requirements.

THE PHASE LOOK UP TABLE

Software files have been supplied that contain optimal phase values for both spurious and lock time requirements. For each Fraction used there is a phase associated with it that must be programmed. For the different fractions there is a valid phase. When a file is loaded its name is displayed below the logo as shown below along with the valid phase and frac on the front panel.



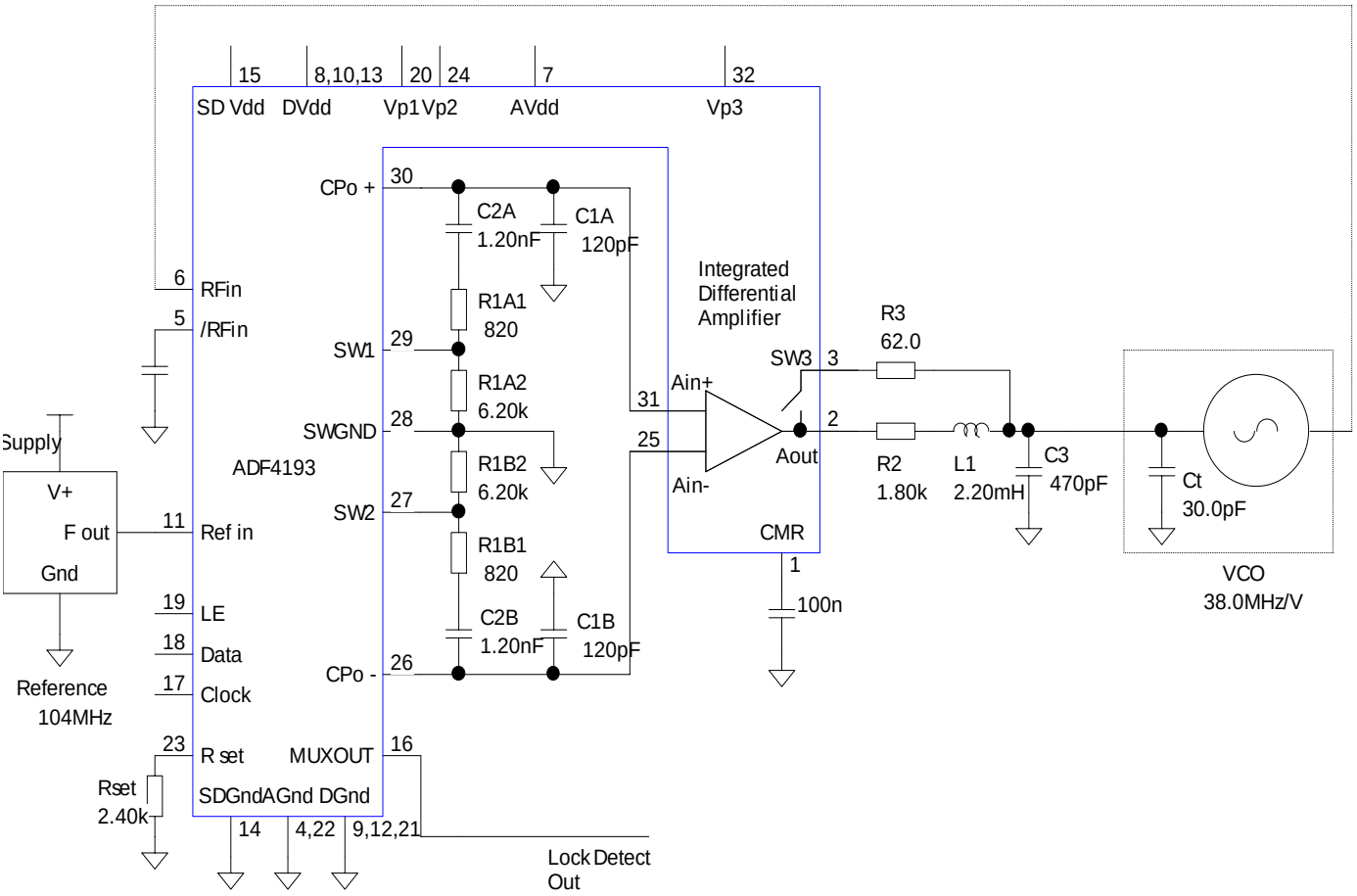


To load a new lookup table you will need to close and re-start the software. The phase tables also contain the basic setup information for the PLL eg PFD, Modulus, timer settings, dither mode. An example of such a table is listed below. An excel sheet has been supplied so that these tables can be created. If the tables are modified in manual form it is important that **tabs** are used to seperate the phase and the frac values. An example of a table is shown below:-

*** ADF4193 Phase Table for DCS1800 / PCS1900 TX**
* with a 13MHz PFD and a ~60kHz Loop BW
*
* File Name: gsm1800tx_phase_codes.txt
* Version: 1.0
* Date: 30-Nov-04
*
* Setup Values:
$PFD= 13
$MOD=65
$CHOP= 13
$ICP= 28
$SW12=35
$SW3= 35
$P= 8
$Dither=0
*
*
* FRAC PHASE
0 13
1 60
2 53
3 50

PLL SIMULATIONS

The ADF4193 performance can be simulated using ADI simPLL v2.7 On the CD three simulations have been supplied included the evaluation board that shows the performance of the evaluation board. The latest version of ADI simPll can be downloaded at www.analog.com/pll For instructions on how to setup the ADF4193 with ADIsimPLL please refer to the tech note **ADF4193-TN-001** that is also supplied on the CD. Below are shown some plots from the ADF4193 simulation file.



Notes:
1. Chip Scale Package pin numbers shown
2. AVdd Analog Power supply
3. DVdd Digital Power Supply
4. SD Vdd Sigma Delta Power Supply
5. Vp1,2 Charge Pump power supply
6. Vp3 Diff Amp Power Supply
7. Consult manufacturer's data sheet for full details

Figure 10 . ADIsimPLL Schematic

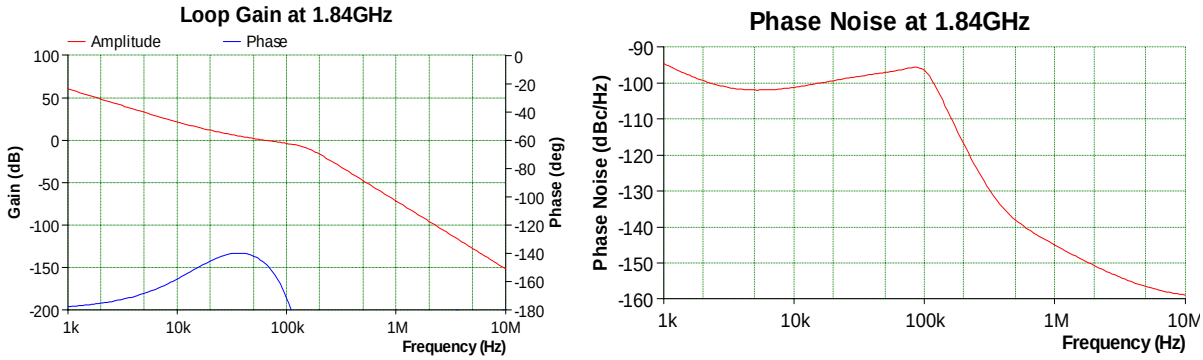


Figure 11 . ADIsimPLL Frequency Domain plots

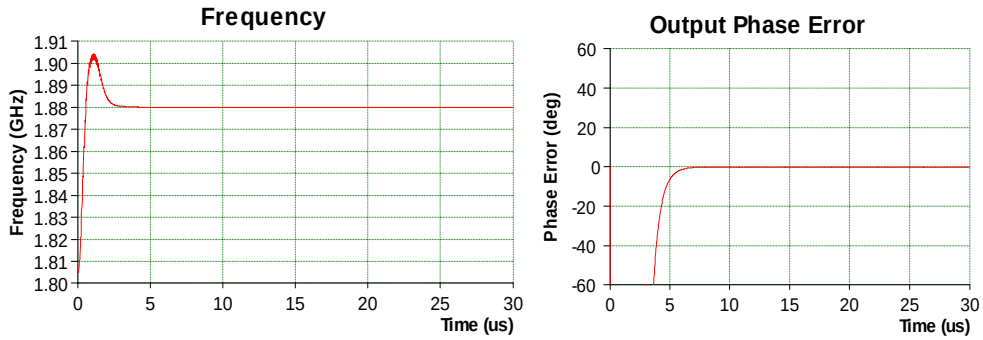


Figure 12 . ADIsimPLL Time Domain plots