FAIRCHILD SEMICONDUCTOR®

April 2008

FDD3510H

Dual N & P-Channel PowerTrench® MOSFET

N-Channel: 80V, 13.9A, 80mΩ P-Channel: -80V, -9.4A, 190mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 80mΩ at V_{GS} = 10V, I_D = 4.3A
- Max $r_{DS(on)}$ = 88mΩ at V_{GS} = 6V, I_D = 4.1A

Q2: P-Channel

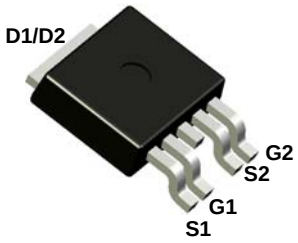
- Max $r_{DS(on)}$ = 190mΩ at V_{GS} = -10V, I_D = -2.8A
- Max $r_{DS(on)}$ = 224mΩ at V_{GS} = -4.5V, I_D = -2.6A
- 100% UIL Tested
- RoHS Compliant

General Description

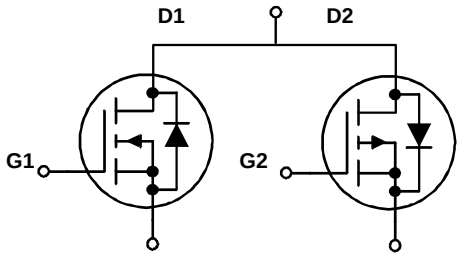
These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Applications

- Inverter
- H-Bridge



Dual DPAK 4L



N-Channel P-Channel

MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		80	-80	V
V_{GS}	Gate to Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	T_C = 25°C	13.9	-9.4	A
	- Continuous	T_A = 25°C	4.3	-2.8	
	- Pulsed		20	-10	
P_D	Power Dissipation for Single Operation	T_C = 25°C (Note 1)	35	32	W
		T_A = 25°C (Note 1a)	3.1		
		T_A = 25°C (Note 1b)	1.3		
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	37	54	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q1 (Note 1)	3.5	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q2 (Note 1)	3.9	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3510H	FDD3510H	TO-252-4L	13”	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D =250μA, V_{GS} = 0V I_D = -250μA, V_{GS} = 0V	Q1 Q2	80 -80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = -250μA, referenced to 25°C	Q1 Q2		84 -67		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64V, V_{GS} = 0V V_{DS} = -64V, V_{GS} = 0V	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	Q1 Q2			±100 ±100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA V_{GS} = V_{DS}, I_D = -250μA	Q1 Q2	2.0 -1.0	2.6 -1.6	4.0 -3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = -250μA, referenced to 25°C	Q1 Q2		-6.7 4.6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 4.3A V_{GS} = 6.0V, I_D = 4.1A V_{GS} = 10V, I_D = 4.3A, T_J = 125°C	Q1		64 70 121	80 88 152	mΩ
		V_{GS} = -10V, I_D = -2.8A V_{GS} = -4.5V, I_D = -2.6A V_{GS} = -10V, I_D = -2.8A, T_J = 125°C	Q2		153 184 259	190 224 322	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 4.3A V_{DD} = -5V, I_D = -2.8A	Q1 Q2		15 6.8		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = 40V, V_{GS} = 0V, f = 1MHZ	Q1 Q2		600 660	800 880	pF
C_{oss}	Output Capacitance	Q2 V_{DS} = -40V, V_{GS} = 0V, f = 1MHZ	Q1 Q2		56 50	75 70	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		27 25	41 40	pF
R_g	Gate Resistance	f = 1MHz	Q1 Q2		1.7 7.2		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 40V, I_D = 4.3A, V_{GS} = 10V, R_{GEN} = 6Ω Q2 V_{DD} = -40V, I_D = -2.8A, V_{GS} = -10V, R_{GEN} = 6Ω	Q1 Q2		7 6	13 11	ns
t_r	Rise Time		Q1 Q2		2 3	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		16 25	29 40	ns
t_f	Fall Time		Q1 Q2		2 5	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 V_{GS} = 10V, V_{DD} = 40V, I_D = 4.3A Q2 V_{GS} = -10V, V_{DD} = -40V, I_D = -2.8A	Q1 Q2		13 14	18 20	nC
Q_{gs}	Gate to Source Charge		Q1 Q2		2.3 1.9		nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		3.2 2.9		nC

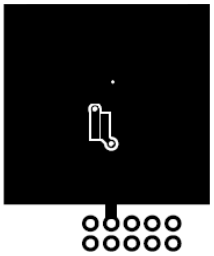
Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.6A (Note 2) V_{GS} = 0V, I_S = -2.6A (Note 2)	Q1 Q2		0.8 -0.8	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 4.3A, di/dt = 100A/s	Q1 Q2		29 30	46 48	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = -2.8A, di/dt = 100A/s	Q1 Q2		28 30	45 48	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Q1

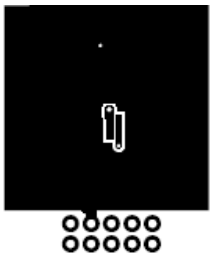


a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper

Scale 1 : 1 on letter size paper

b. 96°C/W when mounted on a minimum pad of 2 oz copper

Q2



a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper

Scale 1 : 1 on letter size paper

b. 96°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting T_J = 25°C, N-ch: L = 3mH, I_{AS} = 5A, V_{DD} = 80V, V_{GS} = 10V; P-ch: L = 3mH, I_{AS} = -6A, V_{DD} = -80V, V_{GS} = -10V.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

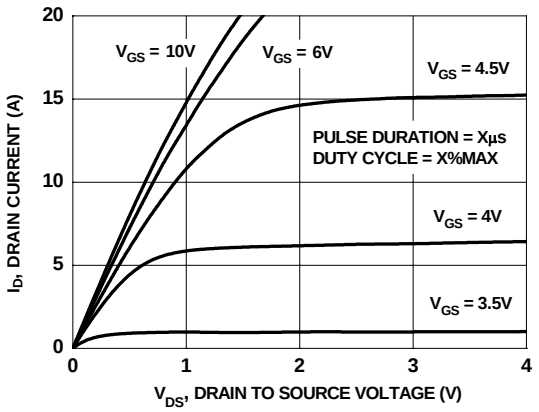


Figure 1. On Region Characteristics

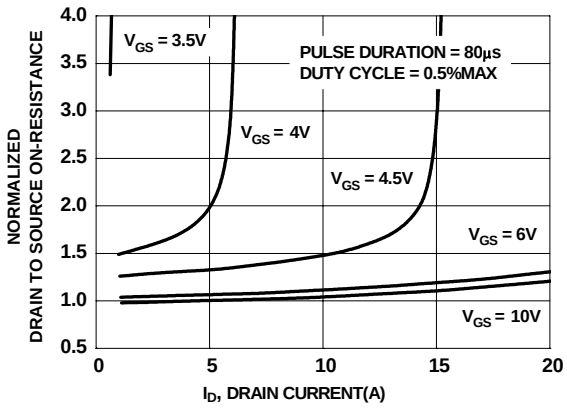


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

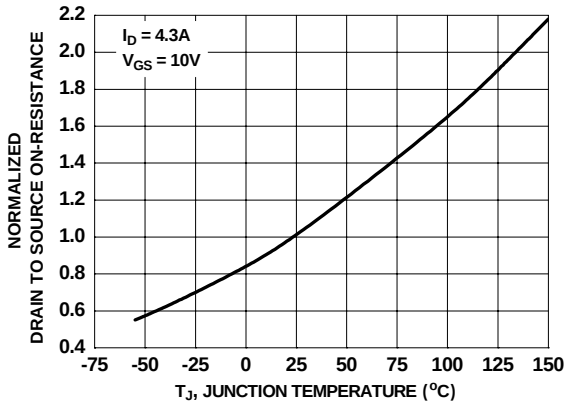


Figure 3. Normalized On Resistance vs Junction Temperature

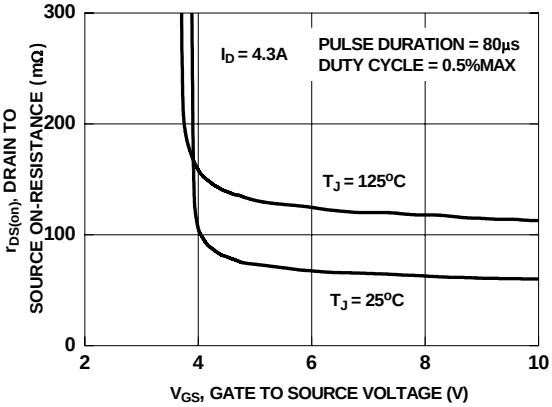


Figure 4. On-Resistance vs Gate to Source Voltage

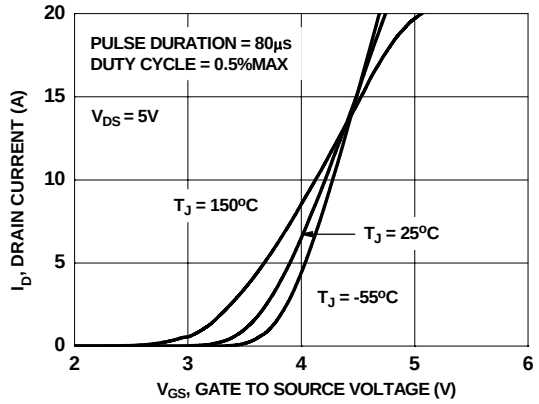


Figure 5. Transfer Characteristics

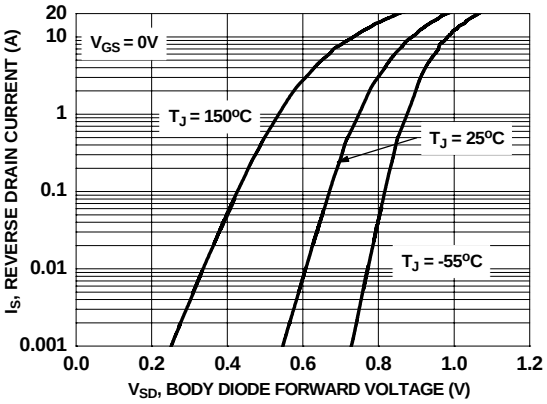


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

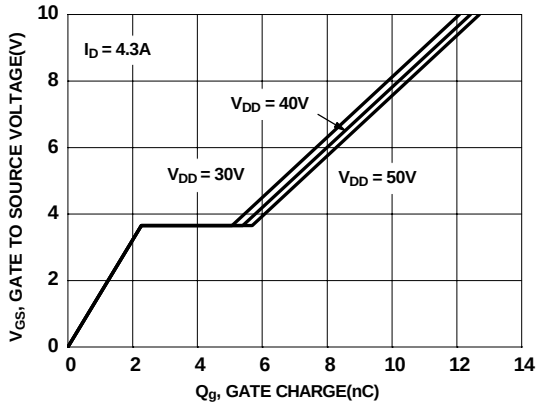


Figure 7. Gate Charge Characteristics

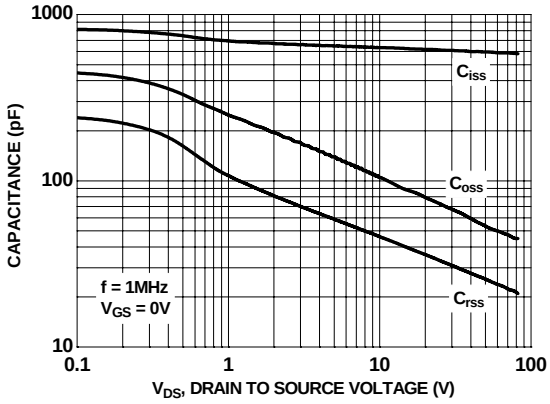


Figure 8. Capacitance vs Drain to Source Voltage

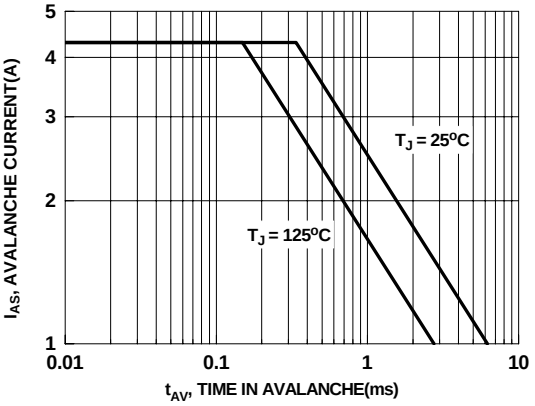


Figure 9. Unclamped Inductive Switching Capability

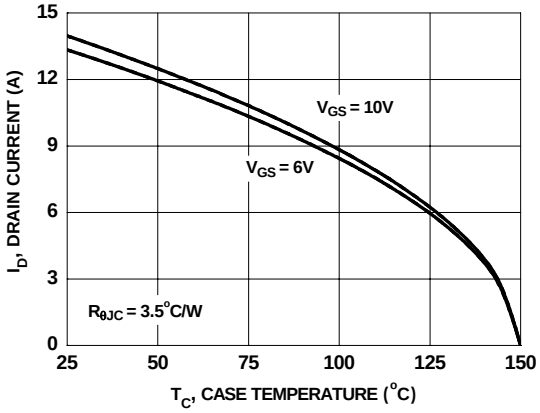


Figure 10. Maximum Continuous Drain Current vs Case Temperature

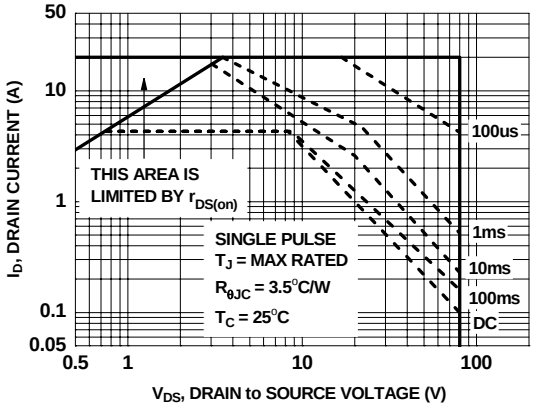


Figure 11. Forward Bias Safe Operating Area

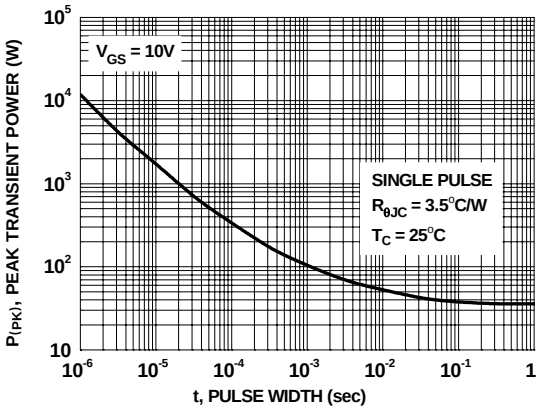


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

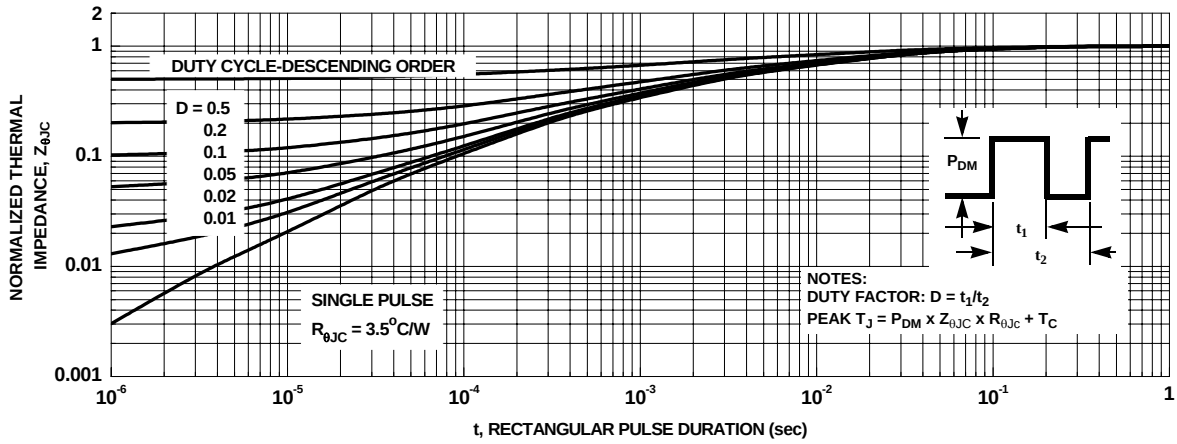


Figure 13. Transient Thermal Response Curve

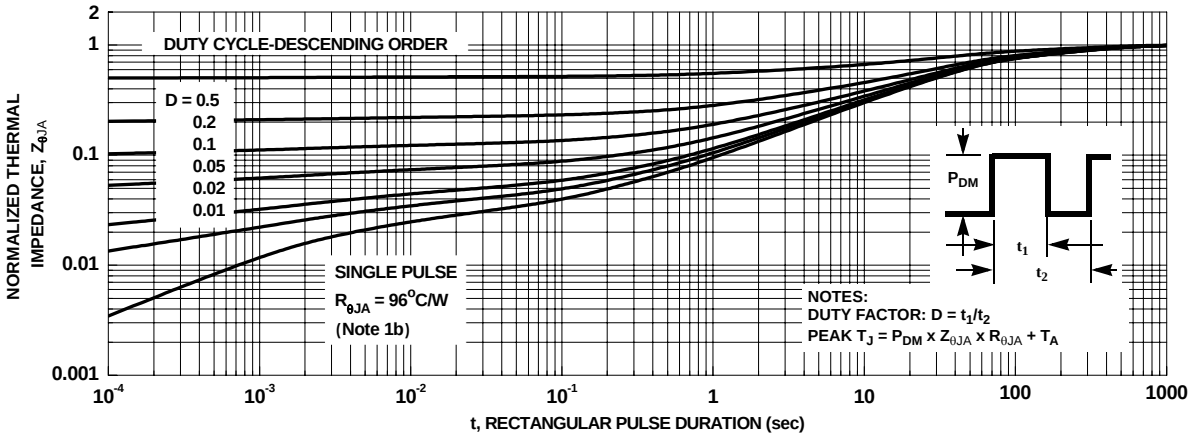


Figure 14. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

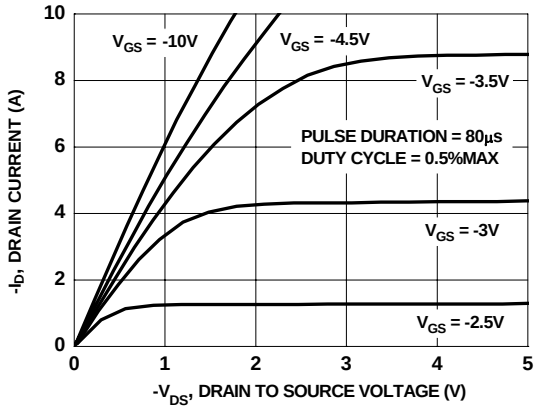


Figure 15. On- Region Characteristics

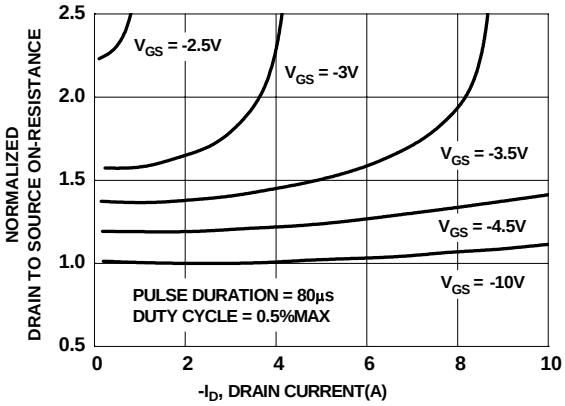


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

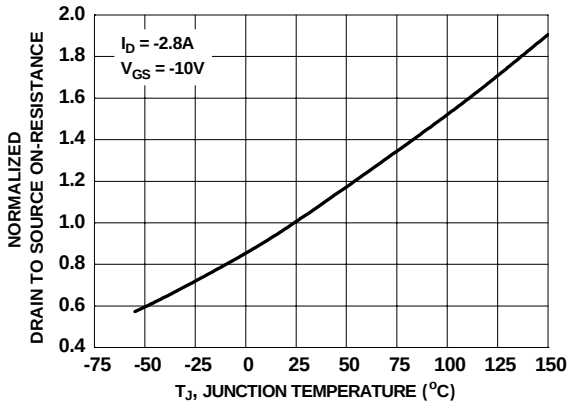


Figure 17. Normalized On-Resistance vs Junction Temperature

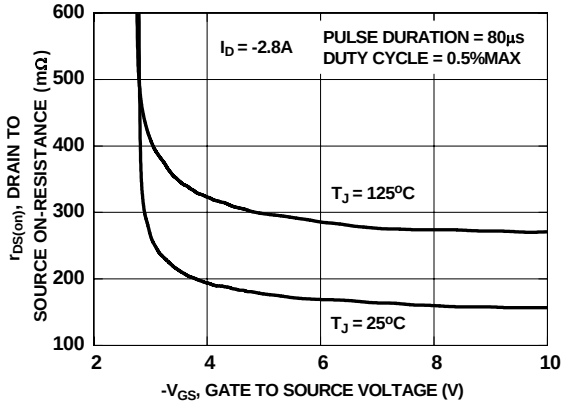


Figure 18. On-Resistance vs Gate to Source Voltage

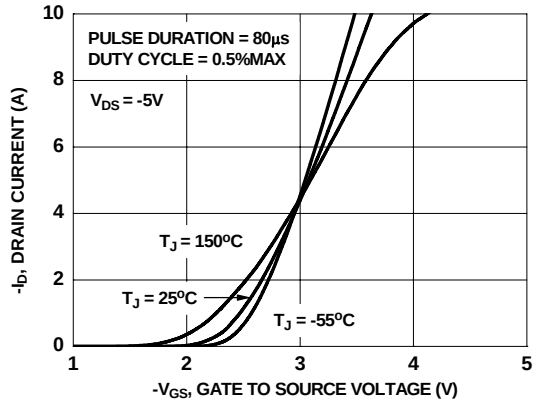


Figure 19. Transfer Characteristics

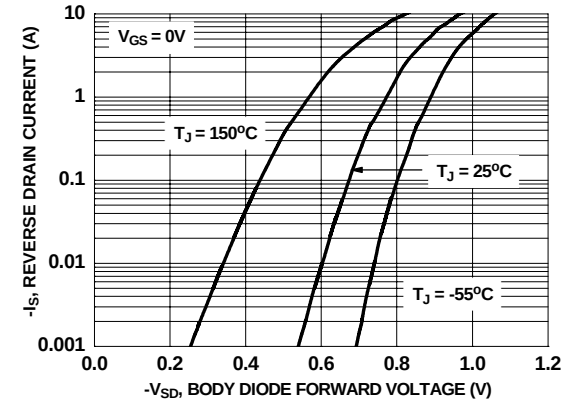


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

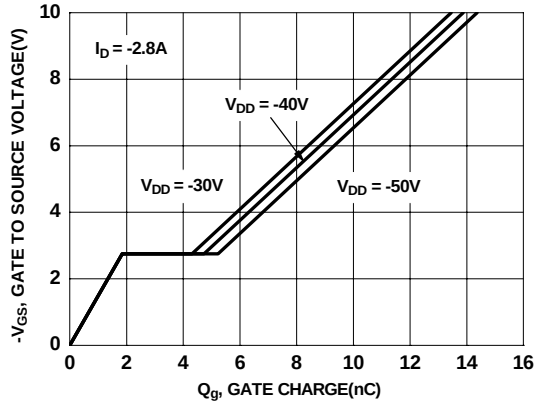


Figure 21. Gate Charge Characteristics

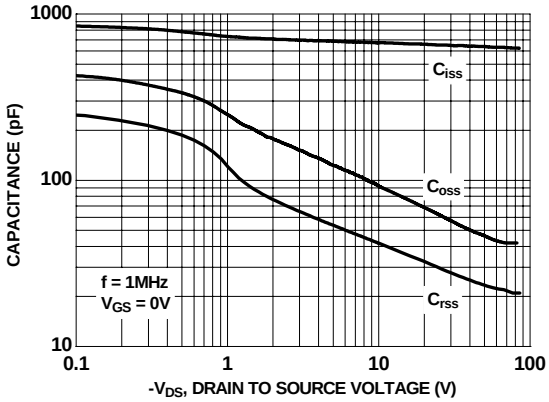


Figure 22. Capacitance vs Drain to Source Voltage

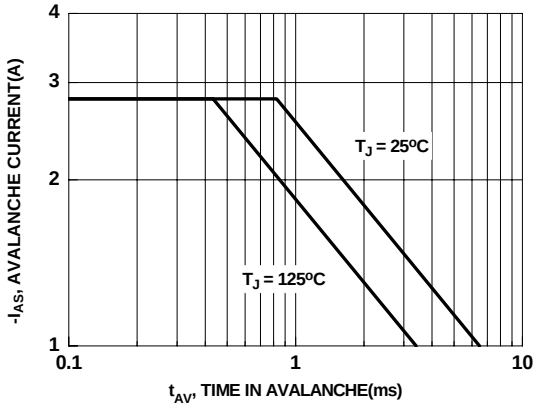


Figure 23. Unclamped Inductive Switching Capability

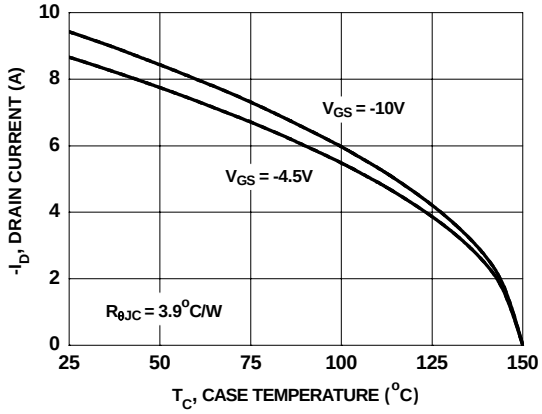


Figure 24. Maximum Continuous Drain Current vs Case Temperature

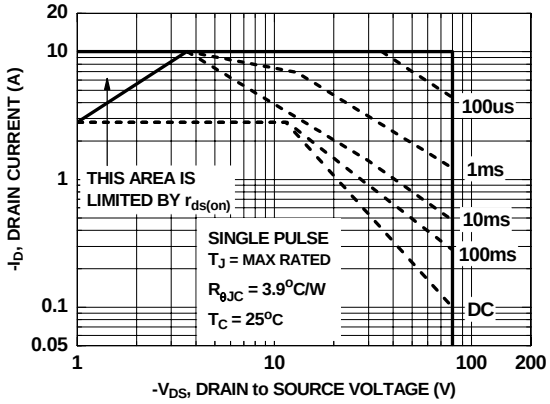


Figure 25. Forward Bias Safe Operating Area

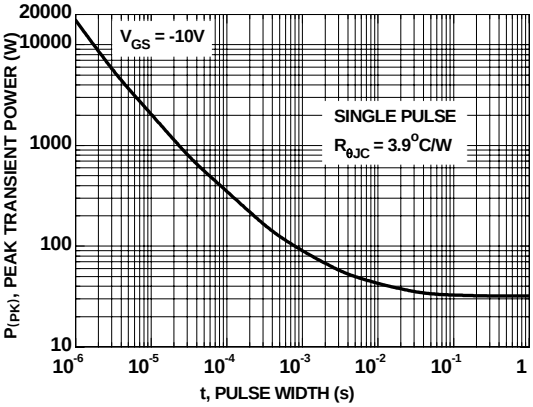


Figure 26. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) T_J = 25°C unless otherwise noted

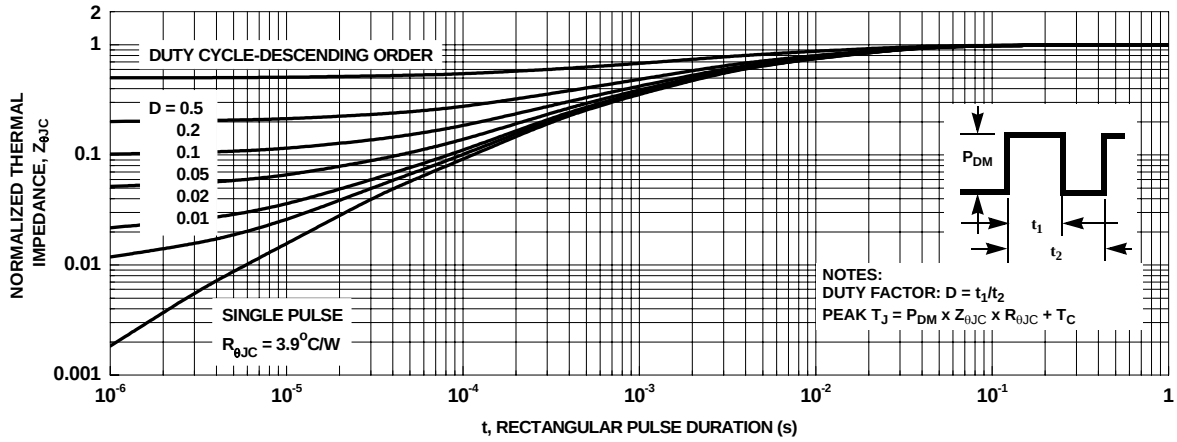


Figure 27. Transient Thermal Response Curve

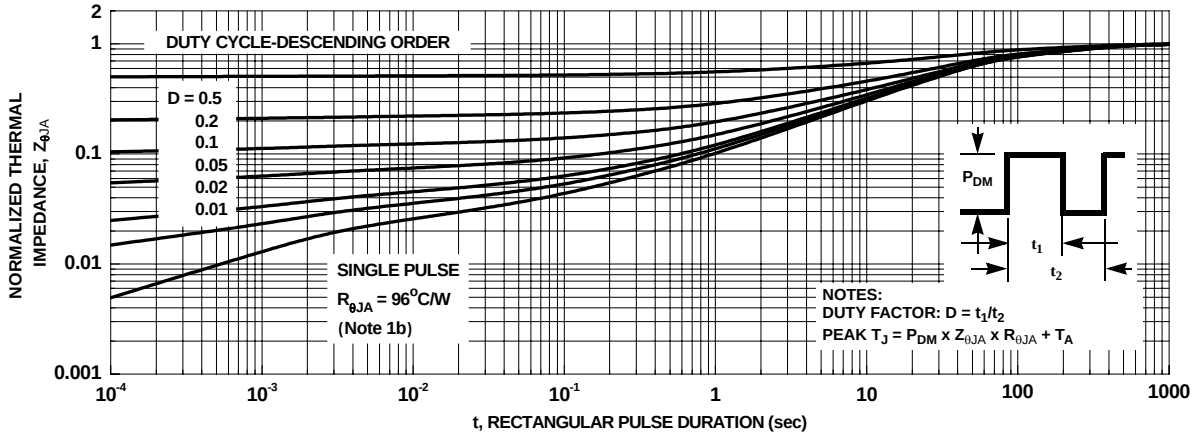


Figure 28. Transient Thermal Response Curve

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidianries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter® *
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world 1mW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SuperMOS™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
µSerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34