

# FDMB3800N

## Dual N-Channel PowerTrench® MOSFET

30V, 4.8A, 40mΩ

### Features

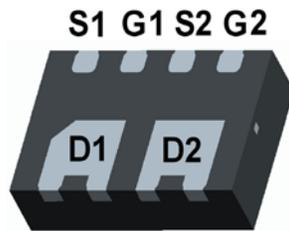
- Max  $r_{DS(on)}$  = 40mΩ at  $V_{GS} = 10V$ ,  $I_D = 4.8A$
- Max  $r_{DS(on)}$  = 51mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 4.3A$
- Fast switching speed
- Low gate Charge
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability.
- RoHS Compliant



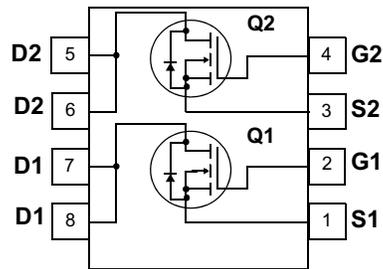
### General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



MicroFET 3X1.9



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	4.8	A
	-Pulsed	9	
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	1.6	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	0.75	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	80	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	165	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
3800	FDMB3800N	MicroFET3X1.9	7"	8mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		24		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$			1 10	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-4		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 4.8\text{A}$		32	40	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 4.3\text{A}$		41	51	
		$V_{GS} = 10\text{V}, I_D = 4.8\text{A}, T_J = 125^\circ\text{C}$		43	61	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 4.8\text{A}$		14		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		350	465	pF
$C_{oss}$	Output Capacitance			90	120	pF
$C_{rss}$	Reverse Transfer Capacitance			40	60	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$		3	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 1\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		8	16	ns
$t_r$	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			21	34	ns
$t_f$	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V to } 5\text{V}$	$V_{DD} = 15\text{V}, I_D = 7.5\text{A}$	4	5.6	nC
$Q_{gs}$	Gate to Source Gate Charge			1.0		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.5		nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain - Source Diode Forward Current			1.25	A	
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1.25\text{A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 4.8\text{A}, di/dt = 100\text{A}/\mu\text{s}$		17		ns
$Q_{rr}$	Reverse Recovery Charge			7		nC

#### Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



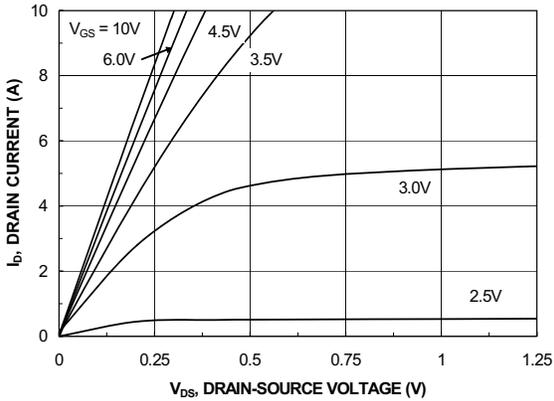
a.  $80^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



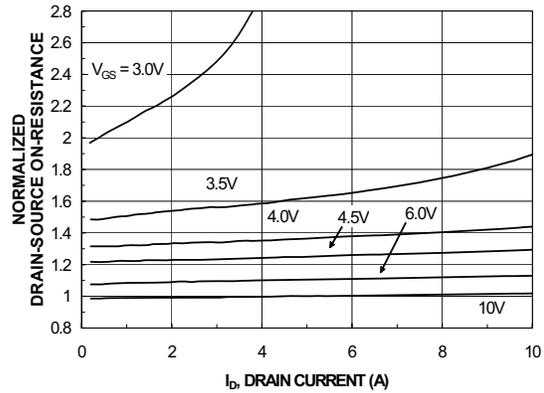
b.  $165^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

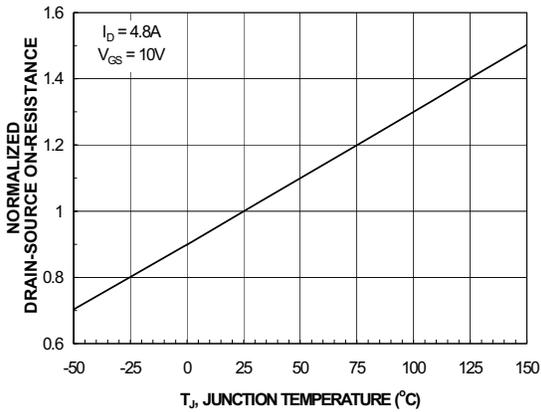
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



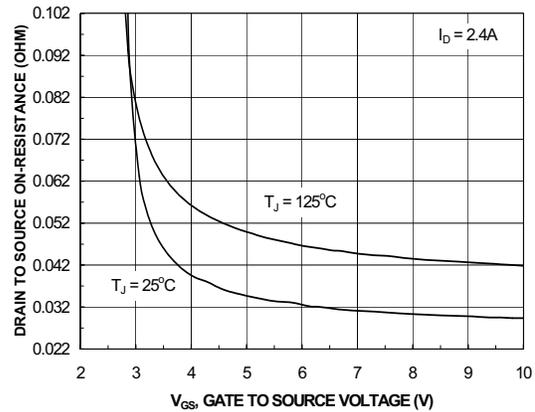
**Figure 1. On Region Characteristics**



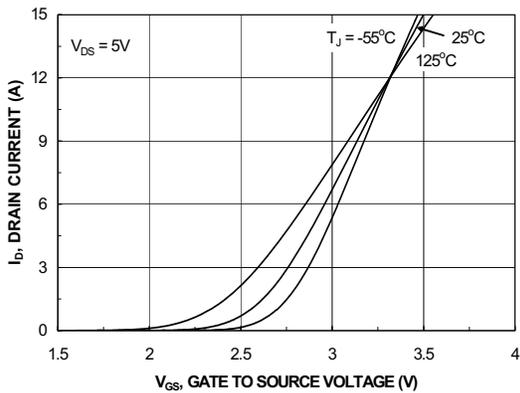
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



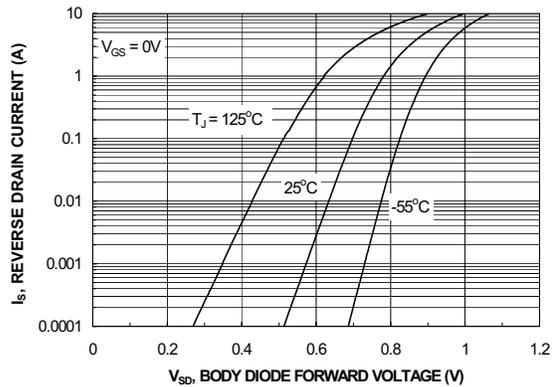
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

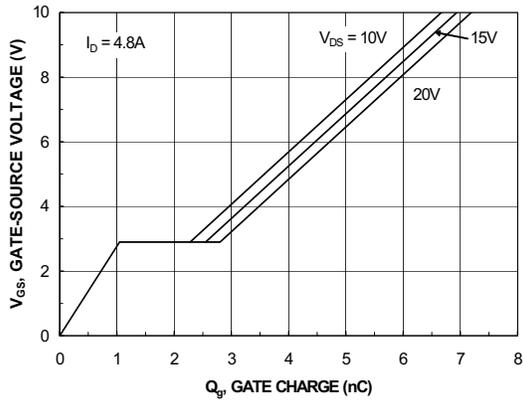


**Figure 5. Transfer Characteristics**

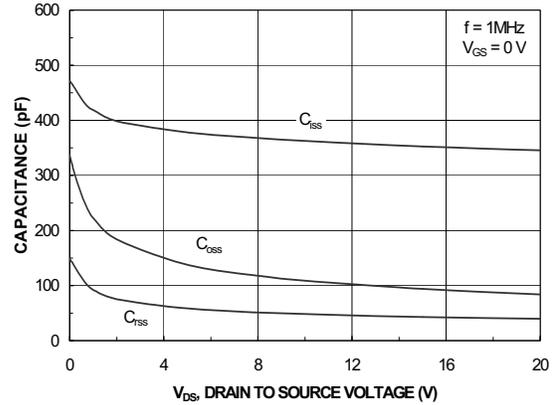


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

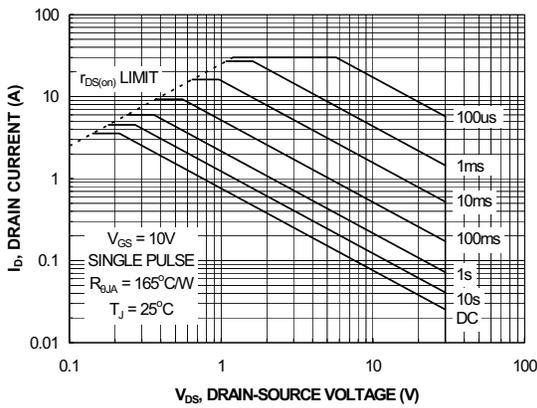
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



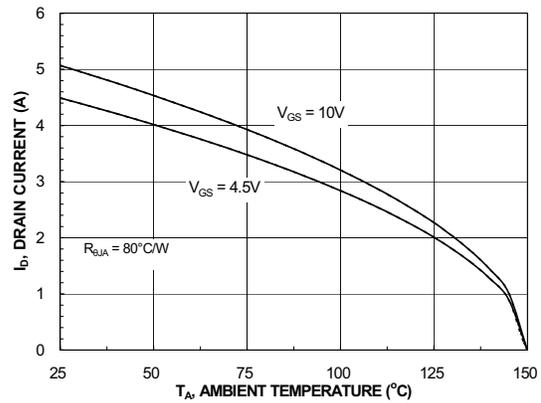
**Figure 7. Gate Charge Characteristics**



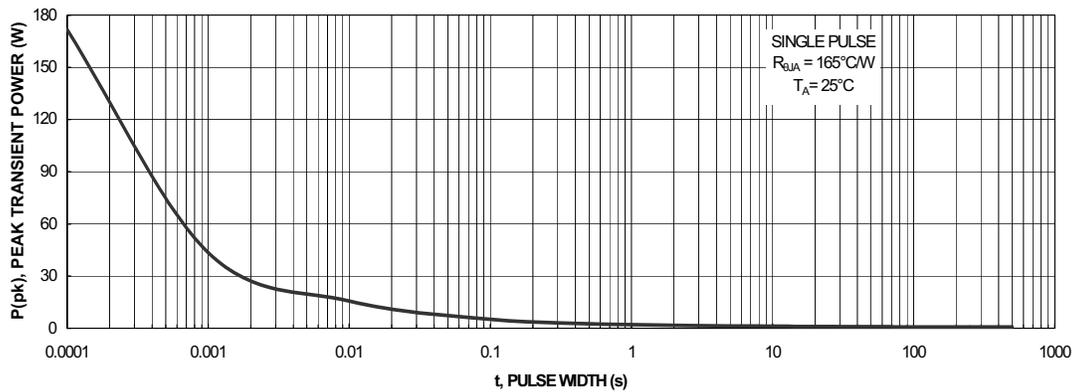
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

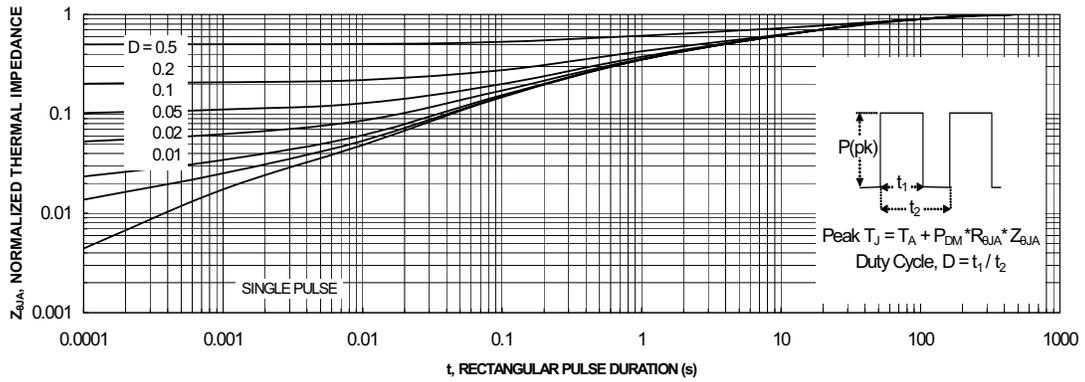


**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**



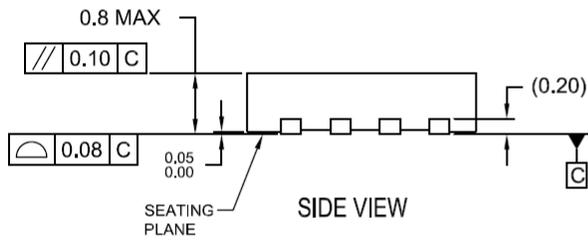
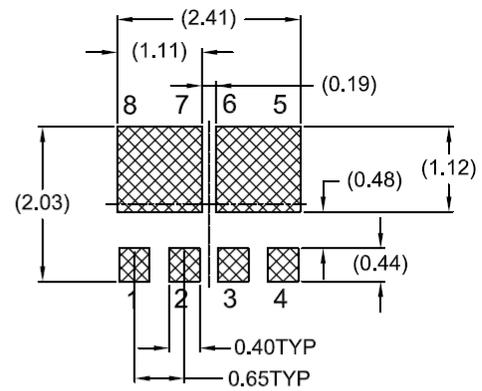
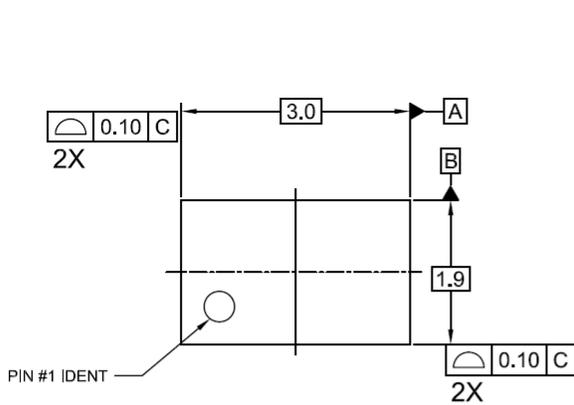
**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



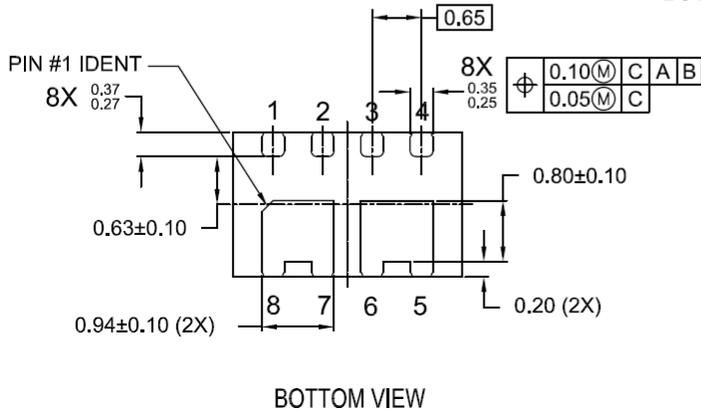
**Figure 12. Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout



**NOTES:**

- Ⓐ DOES NOT FULLY CONFORM TO JEDED REGISTRATION MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILE NAME: MLP08Hrev2





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