FAIRCHILD SEMICONDUCTOR®

April 2013

FDP020N06B_F102

N-Channel PowerTrench® MOSFET

60 V, 313 A, 2 mΩ

Features

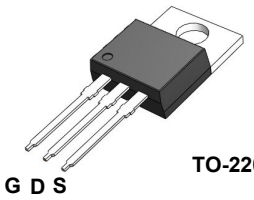
- $R_{DS(on)}$ = 1.65 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 100 A
- Low FOM $R_{DS(on)} * Q_G$
- Low Reverse-Recovery Charge, Q_{rr}= 194 nC
- Soft Reverse-Recovery Body Diode
- Enables High Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

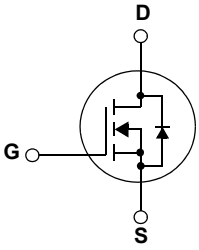
This N-Channel MOSFET is produced using Fairchild Semiconductor®'s advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System



TO-220



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		FDP020N06B_F102	Unit
V_{DSS}	Drain to Source Voltage		60	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	Continuous (T_C = 25°C, Silicon Limited)	313*	A
		Continuous (T_C = 100°C, Silicon Limited)	221*	
		Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	Pulsed (Note 1)	1252	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1859	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	333	W
		Derate above 25°C	2.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP020N06B_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Description	Quantity
FDP020N06B	FDP020N06B_F102	TO-220	F102:Trimmed Leads	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.03	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 48V, T_C = 150°C	-	-	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2.5	3.3	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 100A	-	1.65	2.0	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 100A	-	263	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz	-	16100	20930	pF
C_{oss}	Output Capacitance		-	3840	4992	pF
C_{rss}	Reverse Transfer Capacitance		-	127	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	V_{DS} = 30V, V_{GS} = 0V	-	5897	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 30V, I_D = 100A, V_{GS} = 10V (Note 4)	-	206	268	nC
Q_{gs}	Gate to Source Gate Charge		-	87	-	nC
Q_{gs2}	Gate to Threshold to Plateau		-	36	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	34	-	nC
ESR	Equivalent Series Resistance(G-S)	f = 1MHZ	-	0.9	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30V, I_D = 100A, V_{GS} = 10V,R_{GEN} = 4.7Ω (Note 4)	-	74	158	ns
t_r	Turn-On Rise Time		-	62	134	ns
$t_{d(off)}$	Turn-Off Delay Time		-	112	234	ns
t_f	Turn-Off Fall Time		-	42	94	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	313*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	1252	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 100A	-	-	1.25	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, V_{DD} = 30V, I_{SD} = 100A, dI_F/dt = 100A/μs	-	106	-	ns
Q_{rr}	Reverse Recovery Charge		-	194	-	nC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature
2: Starting T_J = 25°C, L = 3mH, I_{AS} = 35.2A
3: $I_{SD} \le$ 100A, di/dt ≤ 200A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C
4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

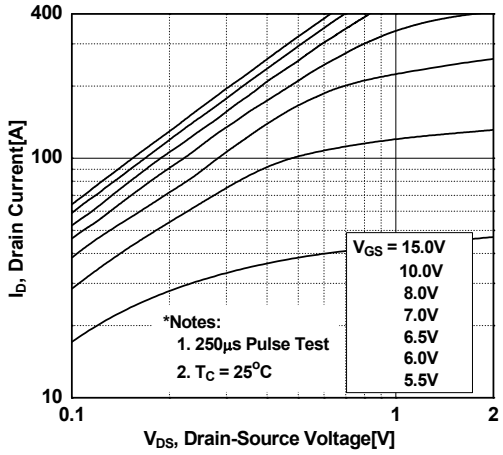


Figure 2. Transfer Characteristics

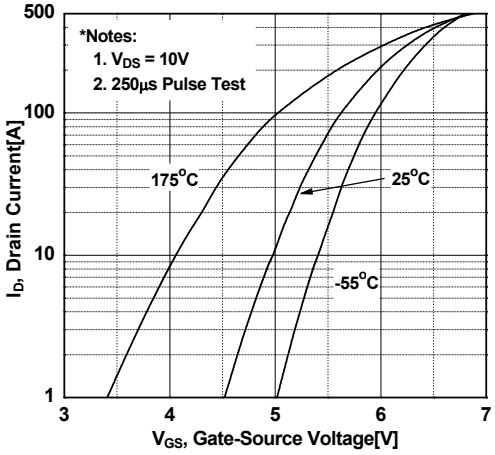


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

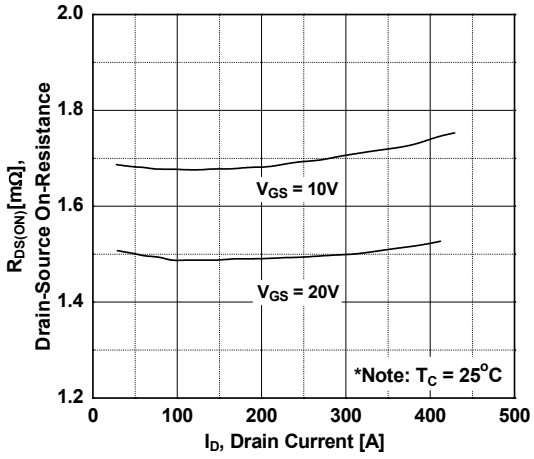


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

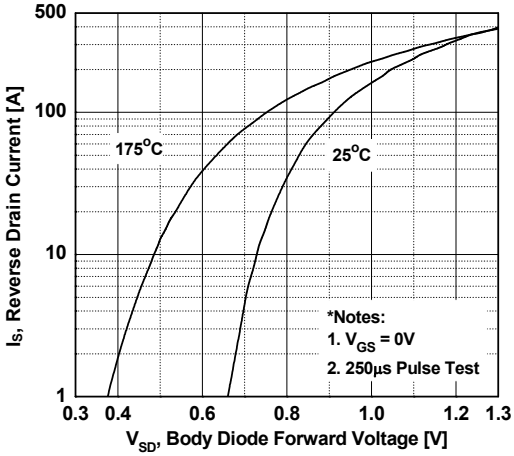


Figure 5. Capacitance Characteristics

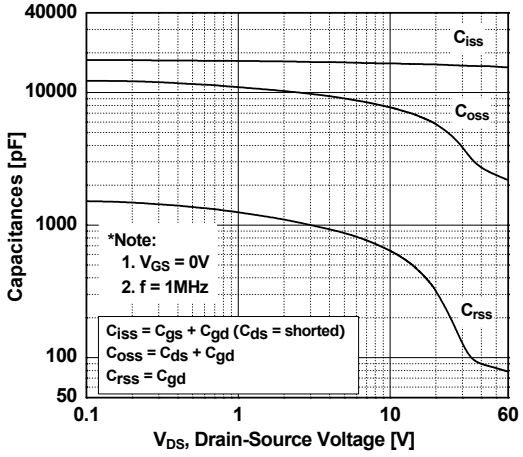
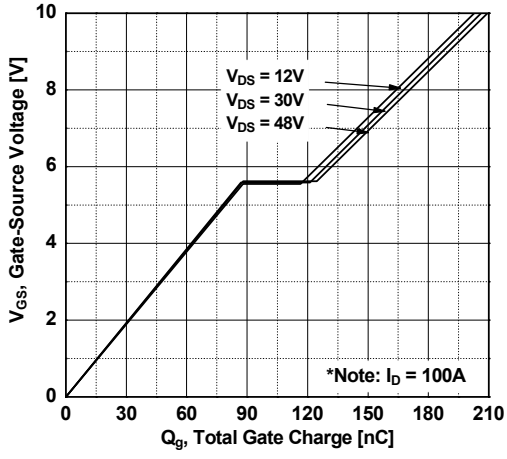


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

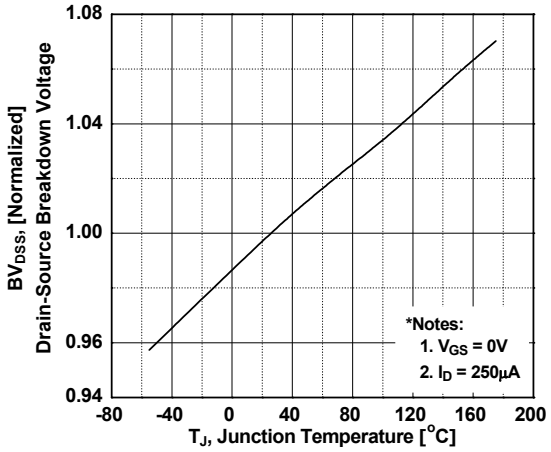


Figure 8. On-Resistance Varition vs. Temperature

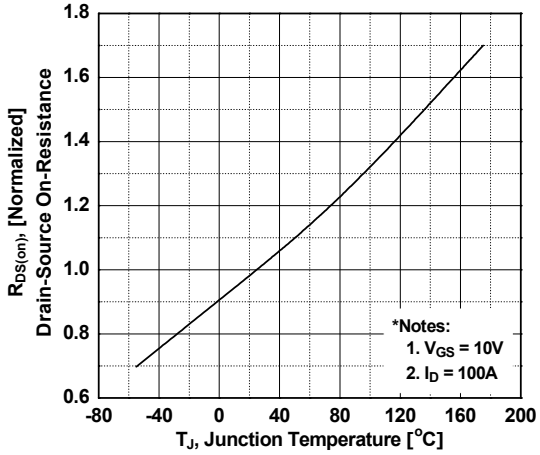


Figure 9. Maximum Safe Operating Area

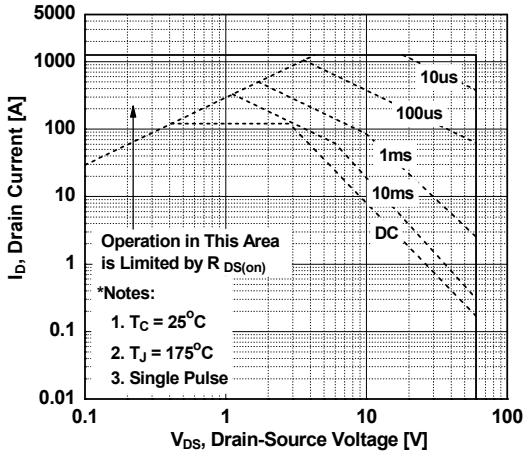


Figure 10. Maximum Drain Current vs. Case Temperature

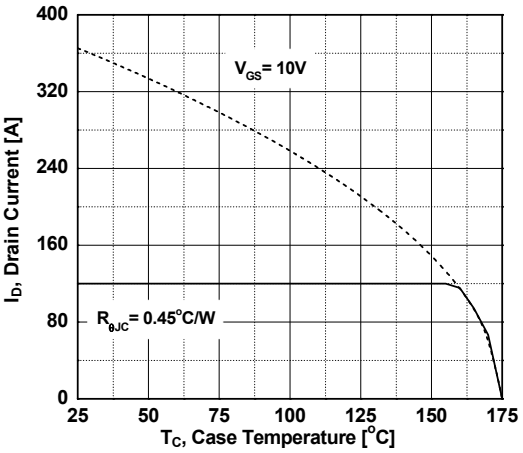


Figure 11. Unclamped Inductive Switching Capability

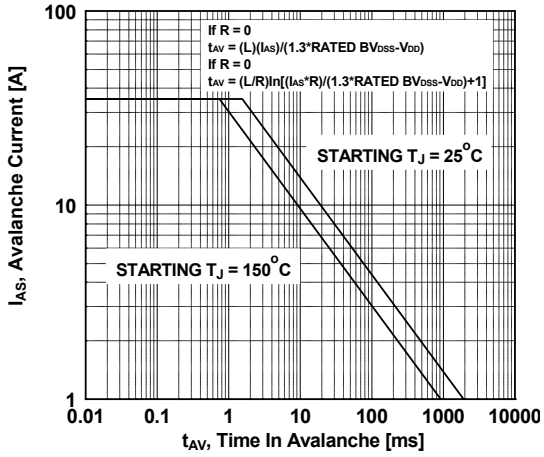
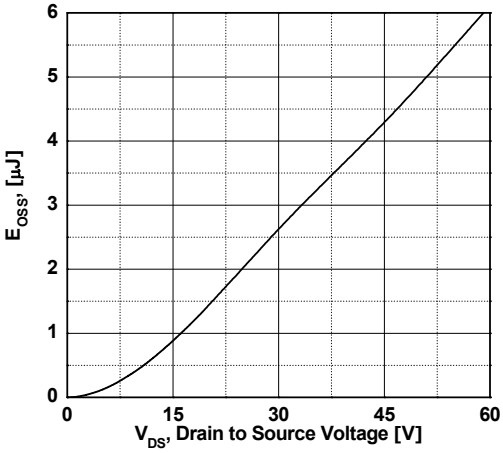
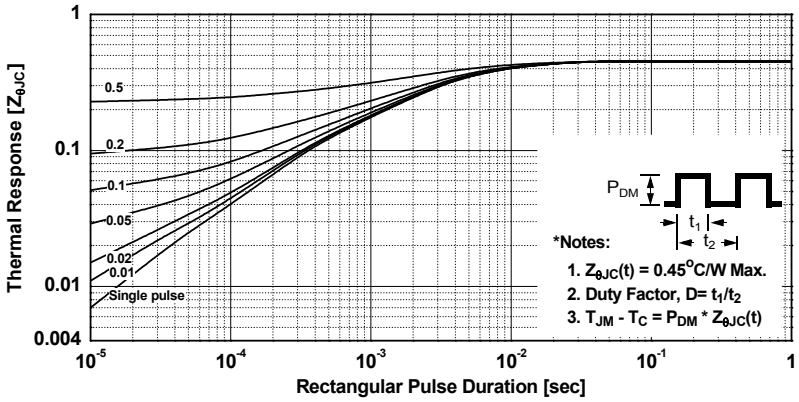


Figure 12. Eoss vs. Drain to Source Voltage

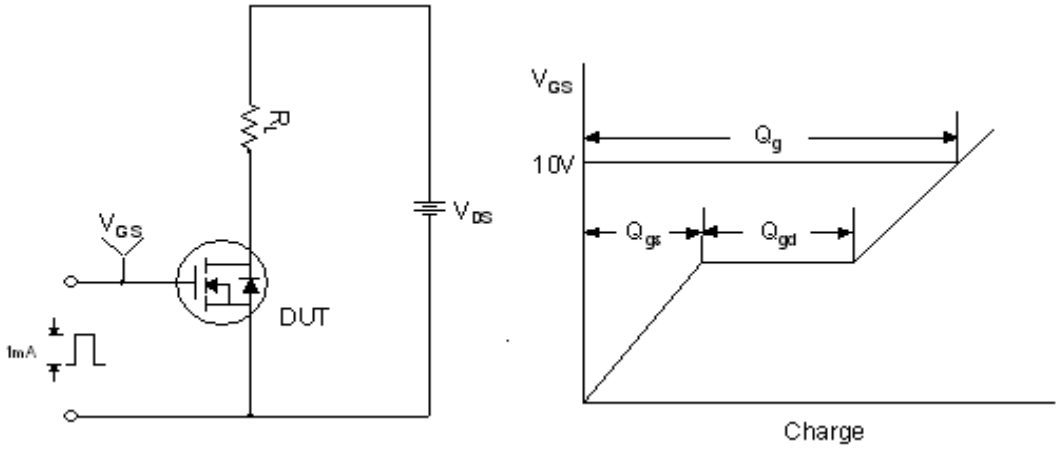


Typical Performance Characteristics (Continued)

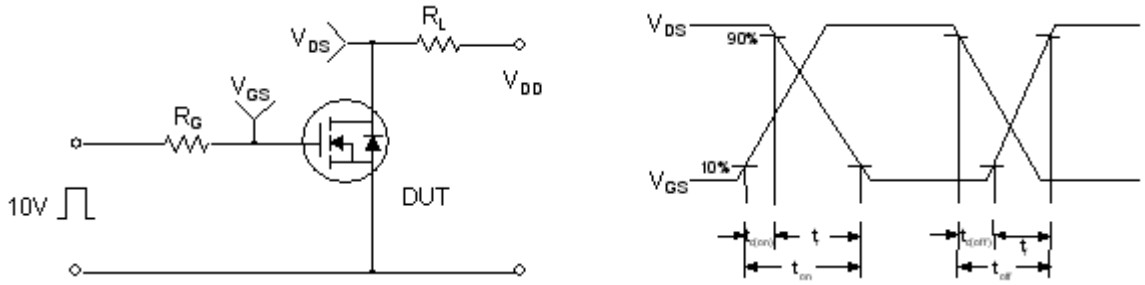
Figure 13. Transient Thermal Response Curve



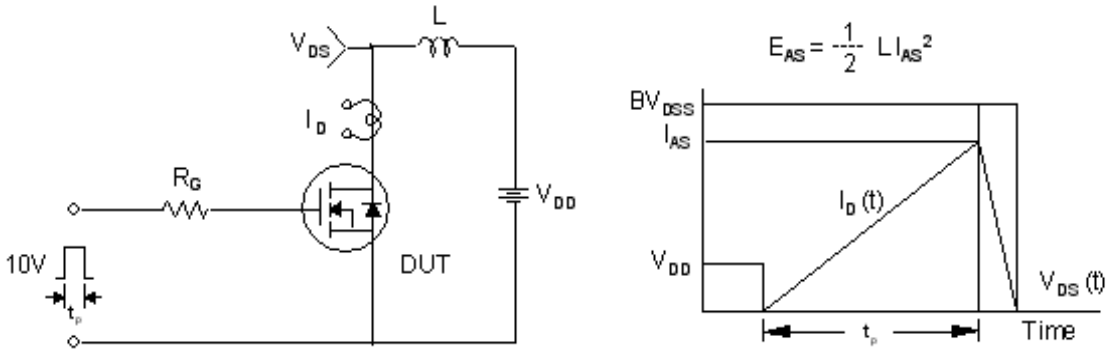
Gate Charge Test Circuit & Waveform



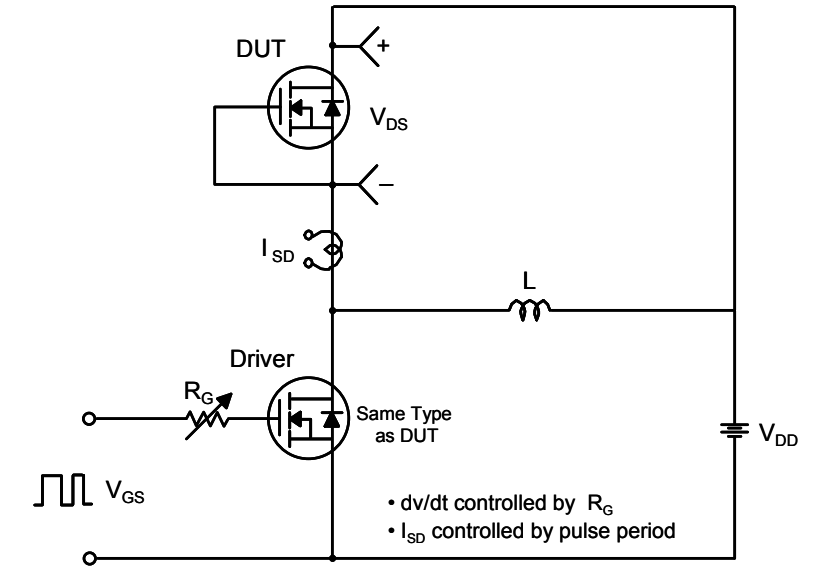
Resistive Switching Test Circuit & Waveforms

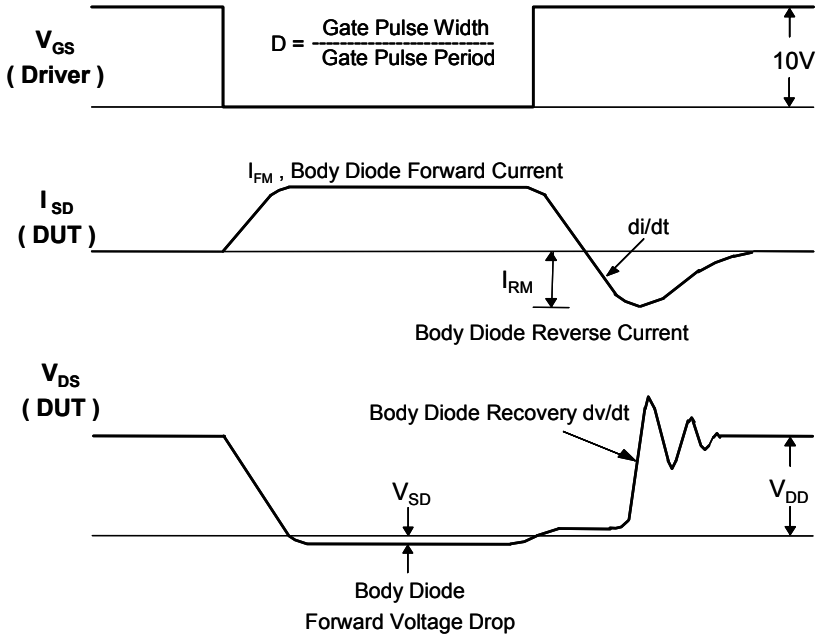


Unclamped Inductive Switching Test Circuit & Waveforms



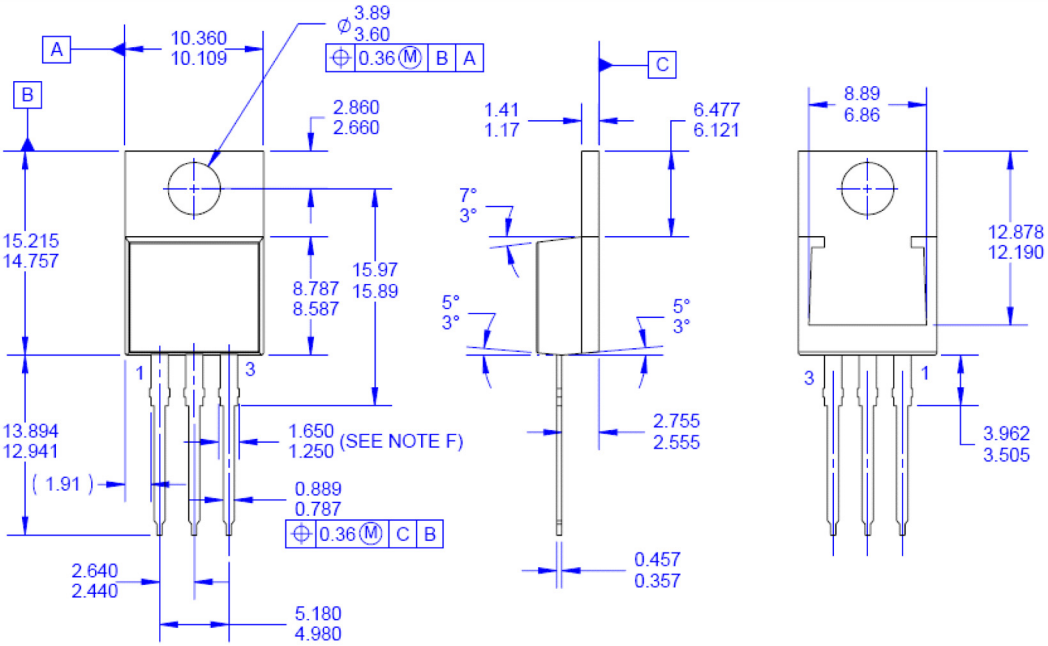
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Physical Dimensions

TO-220T03



NOTES:

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G. DRAWING FILE NAME: TO220T03REV3

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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