

FDP8N50NZU / FDPF8N50NZU N-Channel UniFET™ II Ultra FRFET™ MOSFET 500 V, 6.5 A, 1.2 Ω

Features

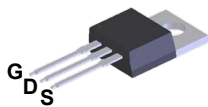
- $R_{DS(on)} = 1.0 \Omega$ (Typ.) @ $V_{GS} = 10 V$, $I_D = 3.25 A$
- Low Gate Charge (Typ. 14 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- Improve dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Application

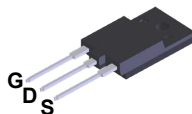
- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

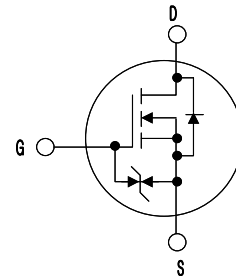
UniFET™ II MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. UniFET II Ultra FRFET™ MOSFET has much superior body diode reverse recovery performance. Its t_{rr} is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET II Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220



TO-220F



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	FDP8N50NZU	FDPF8N50NZU	Unit
V_{DSS}	Drain to Source Voltage	500		V
V_{GSS}	Gate to Source Voltage	± 25		V
I_D	Drain Current	-Continuous ($T_C = 25^\circ C$)	6.5	A
		-Continuous ($T_C = 100^\circ C$)	3.9	
I_{DM}	Drain Current	- Pulsed (Note 1)	26	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	80	mJ
I_{AR}	Avalanche Current	(Note 1)	6.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20	V/ns
P_D	Power Dissipation	($T_C = 25^\circ C$)	130	W
		- Derate above $25^\circ C$	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+150$		$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ C$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP8N50NZU	FDPF8N50NZU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.96	3.1	$^\circ C/W$
$R_{\theta CS}$	Thermal Resistance, Case to Sink, Typ.	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8N50NZU	FDP8N50NZU	TO-220	-	-	50
FDPF8N50NZU	FDPF8N50NZU	TO-220F	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_C = 25^\circ\text{C}$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.5	-	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}$, $V_{GS} = 0\text{V}$ $V_{DS} = 400\text{V}$, $T_C = 125^\circ\text{C}$	-	-	25 250	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 4\text{A}$	-	1.0	1.2	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}$, $I_D = 4\text{A}$	-	6.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	565	735	pF
C_{oss}	Output Capacitance		-	80	105	pF
C_{rss}	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}$, $I_D = 6.5\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	14	18	nC
Q_{gs}	Gate to Source Gate Charge		-	4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	6	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}$, $I_D = 6.5\text{A}$ $R_G = 25\Omega$, $V_{GS} = 10\text{V}$ (Note 4, 5)	-	17	45	ns
t_r	Turn-On Rise Time		-	34	80	ns
$t_{d(off)}$	Turn-Off Delay Time		-	43	95	ns
t_f	Turn-Off Fall Time		-	27	60	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	26	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 6.5A	-	-	1.6	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 6.5A	-	50	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100A/μs	-	0.05	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 3.8\text{mH}$, $I_{AS} = 6.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 6.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

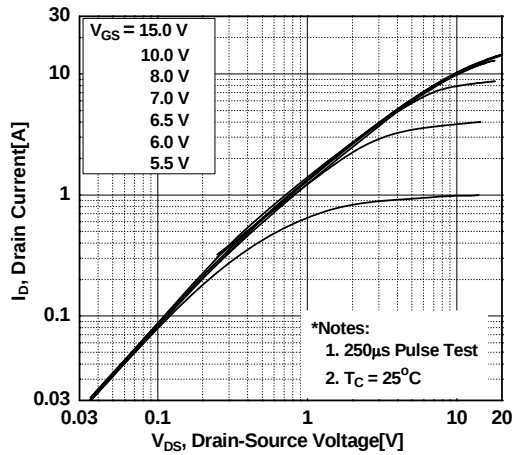


Figure 2. Transfer Characteristics

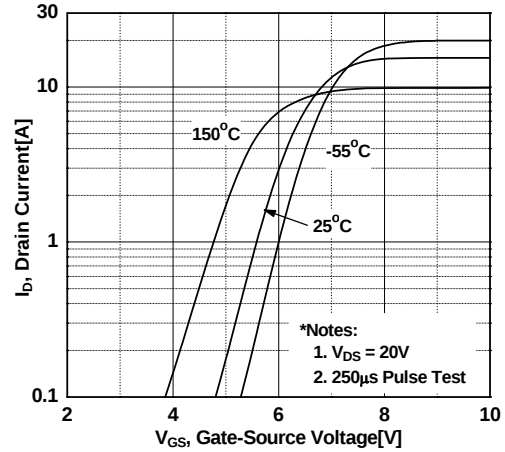


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

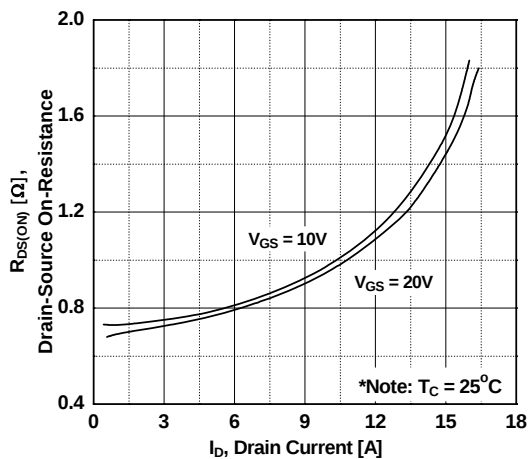


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

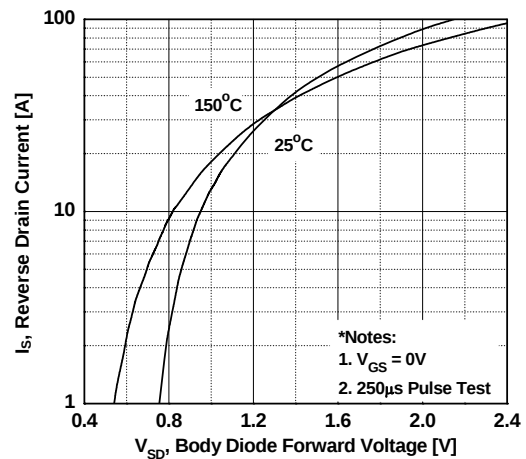


Figure 5. Capacitance Characteristics

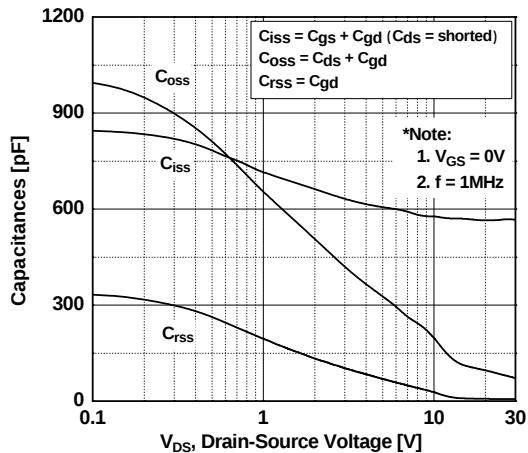
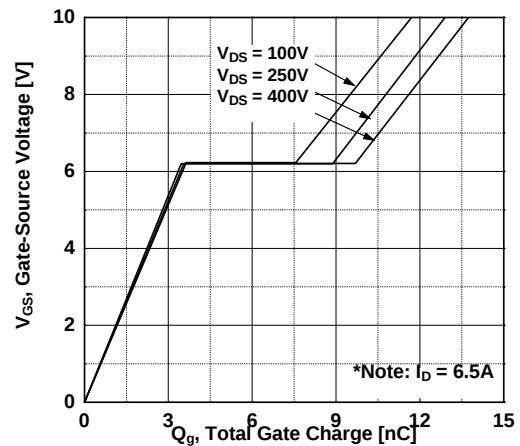


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

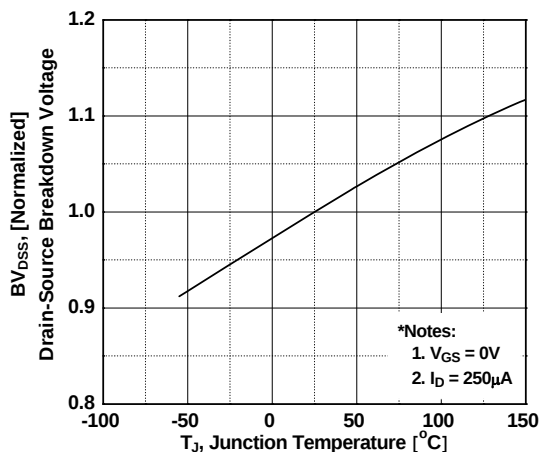


Figure 8. Maximum Safe Operating Area - FDPF8N50NZU

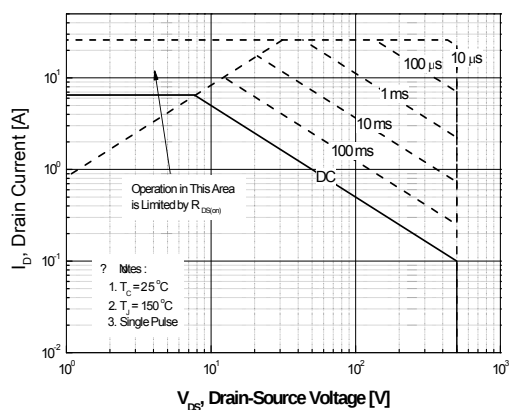


Figure 9. Maximum Drain Current vs. Case Temperature

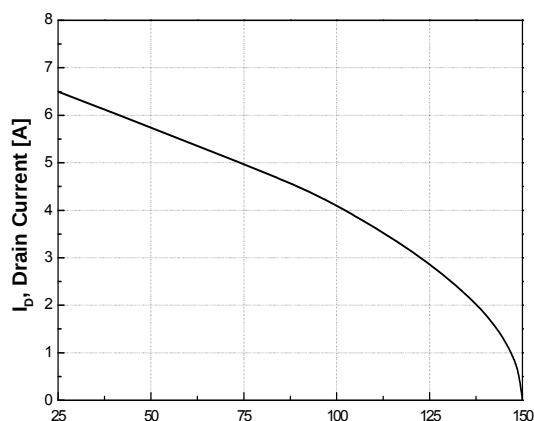
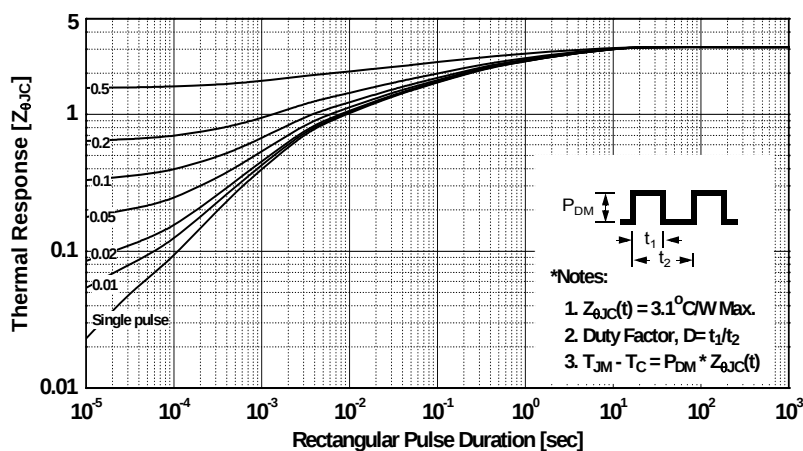
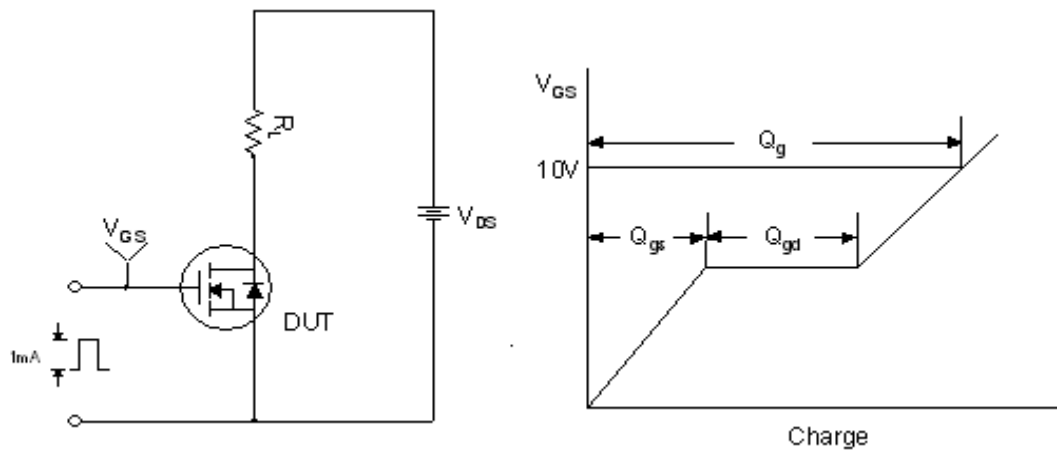


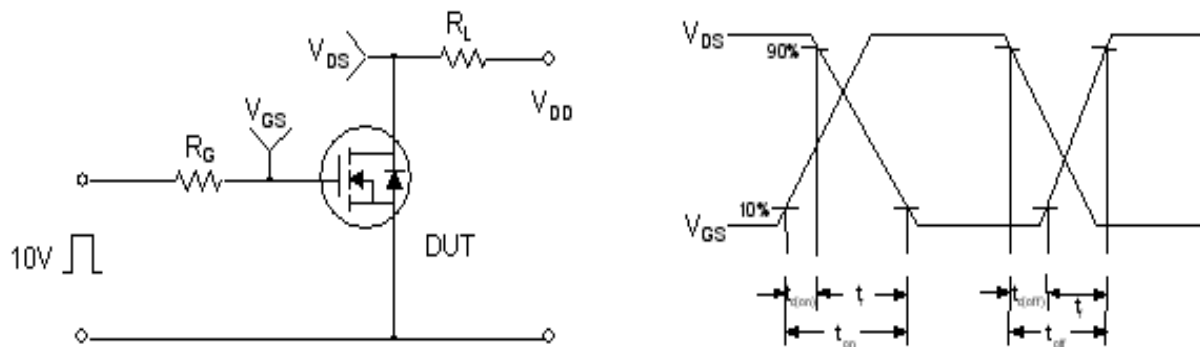
Figure 10. Transient Thermal Response Curve-FDPF8N50NZU



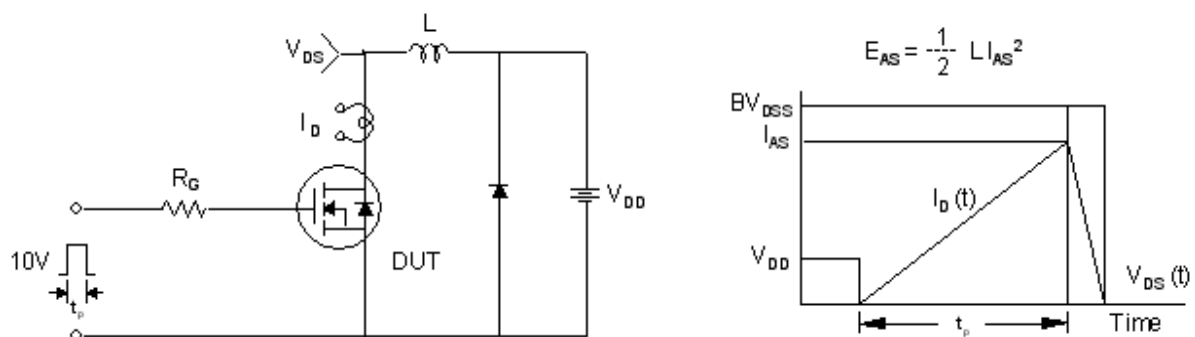
Gate Charge Test Circuit & Waveform



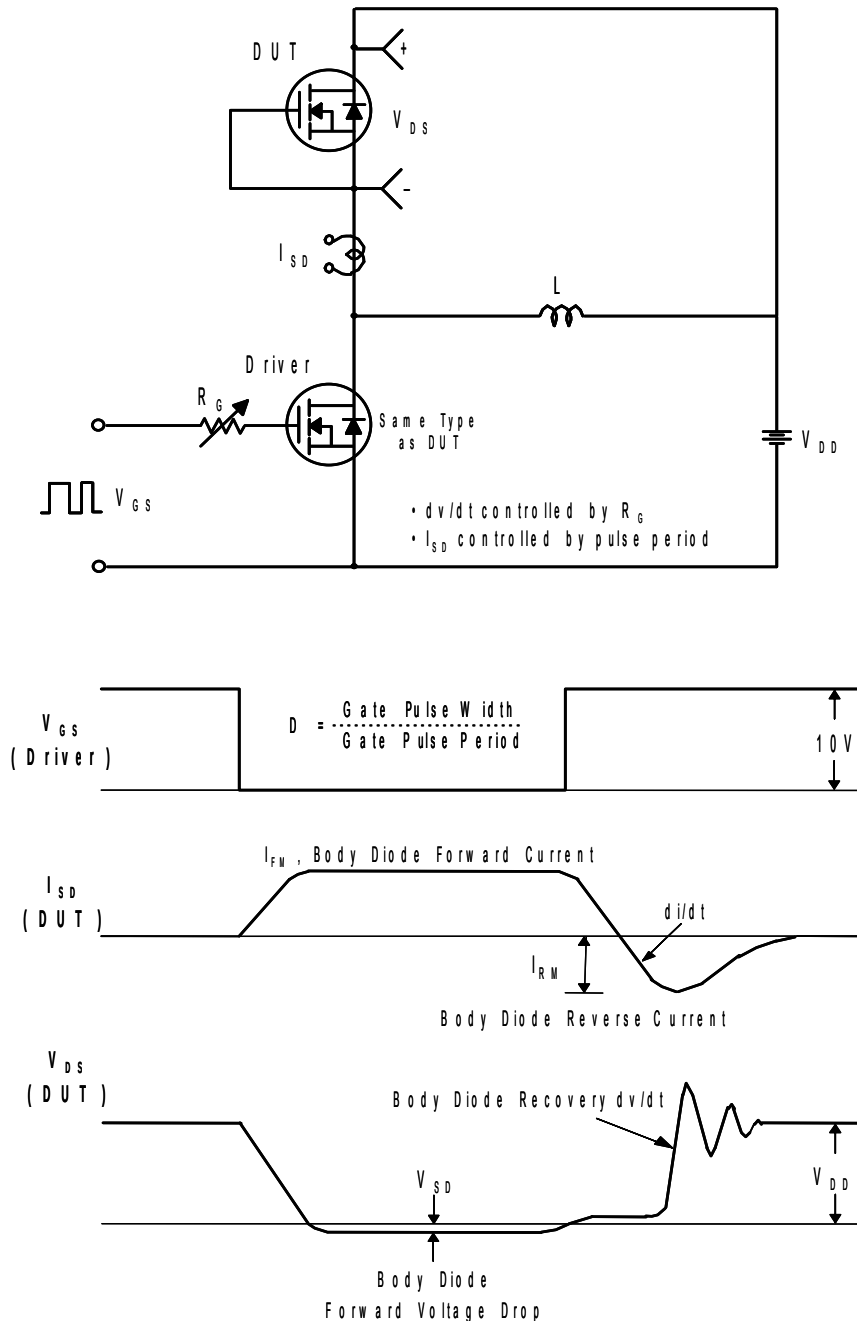
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

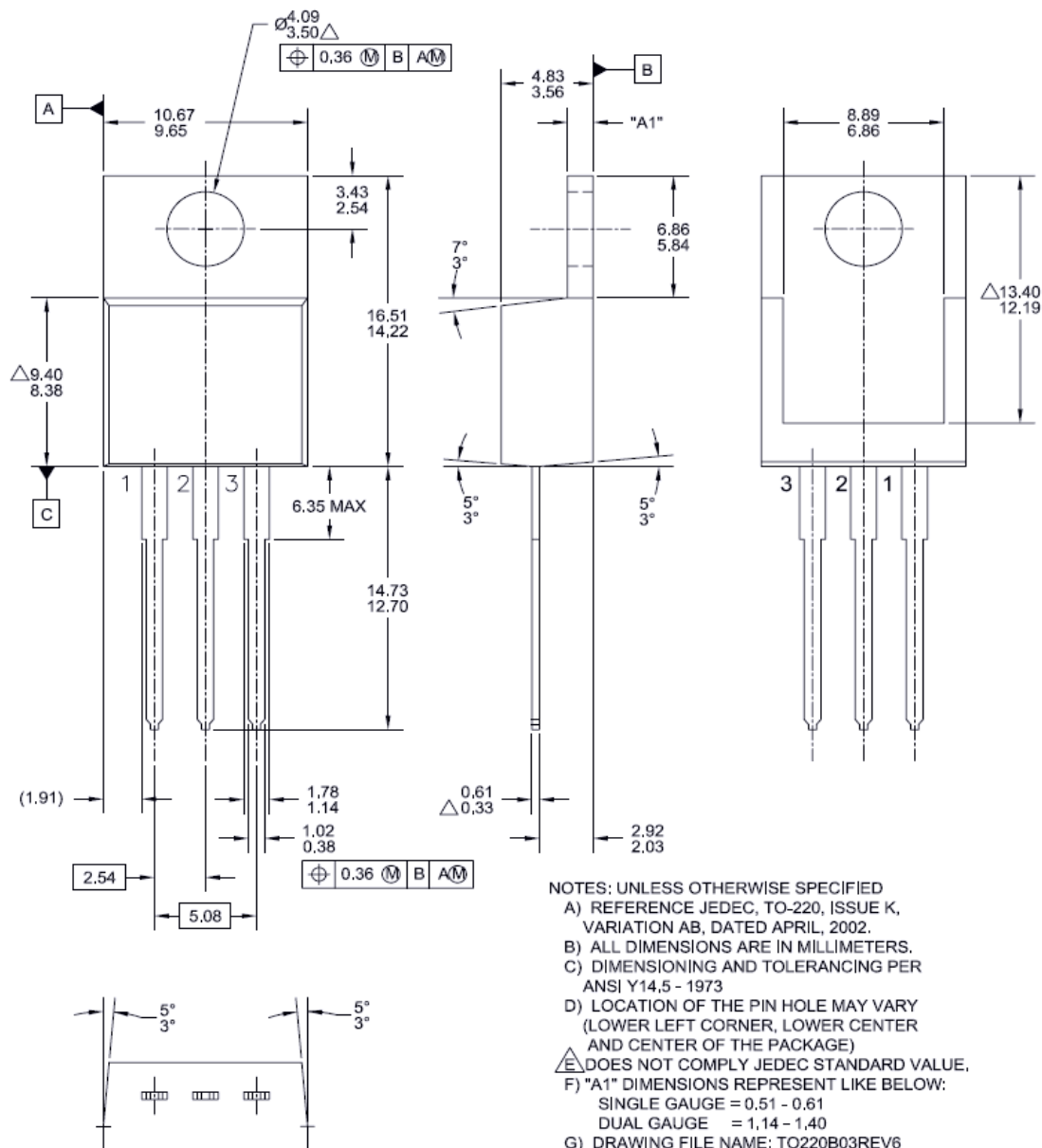


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

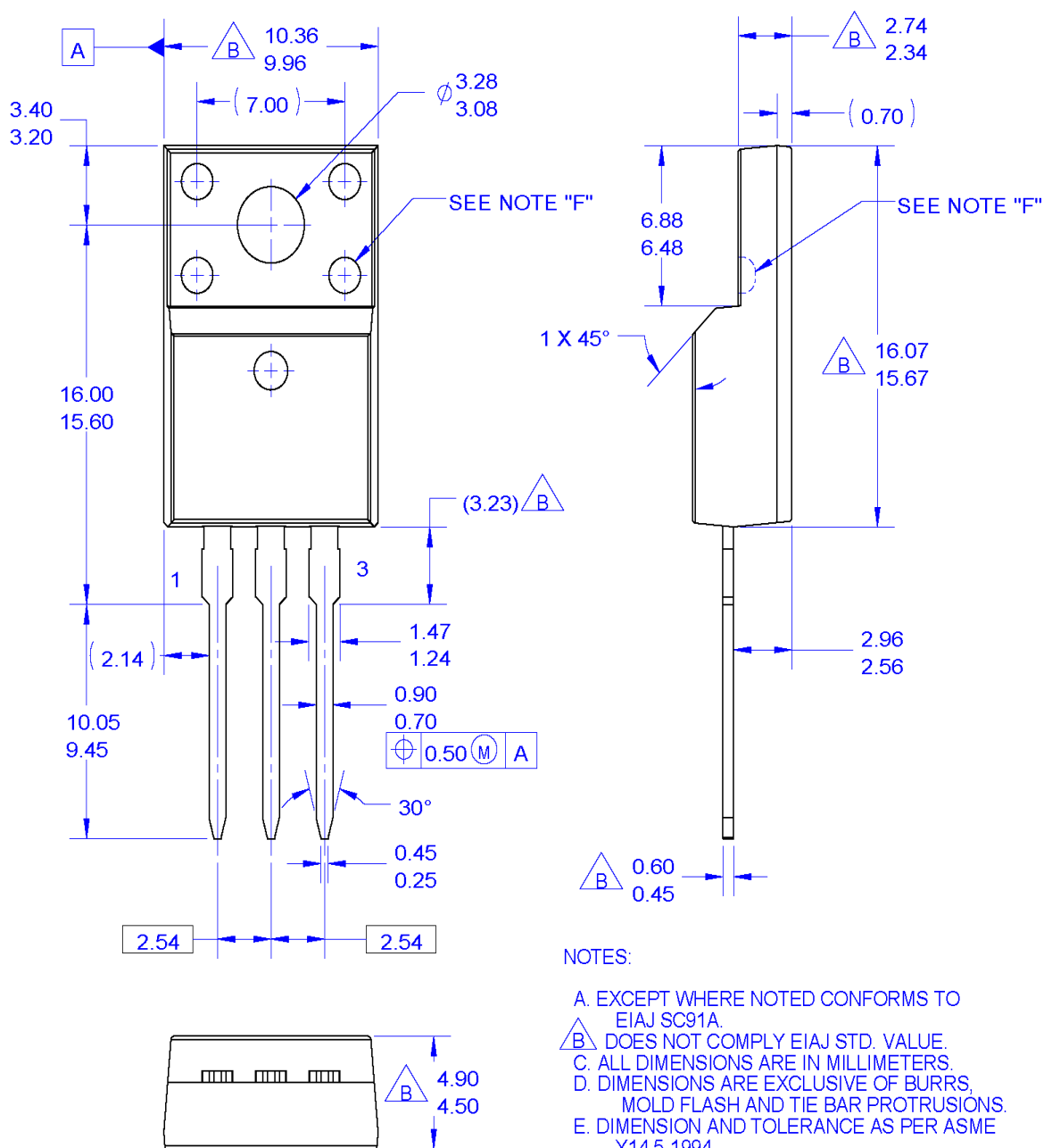
TO-220B03



Dimensions in Millimeters

Mechanical Dimensions

TO-220M03



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.**
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: T0220M03REV3

Dimensions in Millimeters

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. 164