FAIRCHILD SEMICONDUCTOR®

July 2012

FDS6680A

Single N-Channel, Logic Level, PowerTrench® MOSFET

General Description

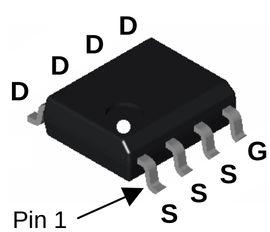
This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced Power Trench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

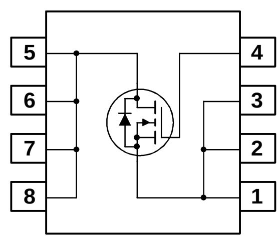
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 12.5 A, 30 V $R_{DS(ON)}$ = 9.5 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 13 mΩ @ V_{GS} = 4.5 V
- Ultra-low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

SO-8





Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	
I_D	Drain Current – Continuous	(Note 1a)	12.5	A
	– Pulsed		50	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Case	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6680A	FDS6680A	13''	12mm	2500 units

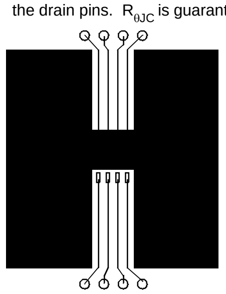
Electrical Characteristics

T_A = 25°C unless otherwise noted

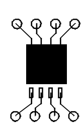
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J=55°C			10	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–4.9		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 12.5 A V_{GS} = 4.5 V, I_D = 10.5 A V_{GS} = 10 V, I_D = 12.5 A, T_J=125°C		7.8 9.9 11.0	9.5 13 15	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	25			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 12.5 A		64		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1620		pF
C_{oss}	Output Capacitance			380		pF
C_{rss}	Reverse Transfer Capacitance			160		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.3		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		10	19	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			27	43	ns
t_f	Turn–Off Fall Time			15	27	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 12.5 A, V_{GS} = 5 V		16	23	nC
Q_{gs}	Gate–Source Charge			5		nC
Q_{gd}	Gate–Drain Charge			5.8		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.73	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 12.5 A, d_{iF}/d_t = 100 A/µs		28		ns
Q_{rr}	Diode Reverse Recovery Charge			18		nC

Notes:

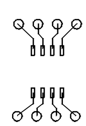
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 105°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

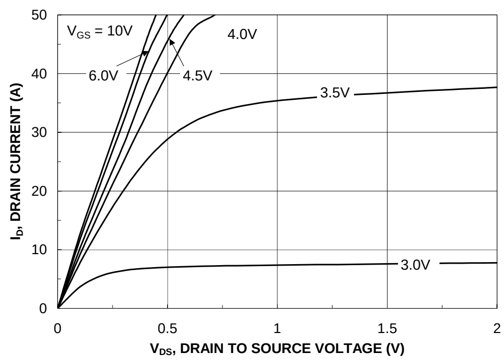


Figure 1. On-Region Characteristics.

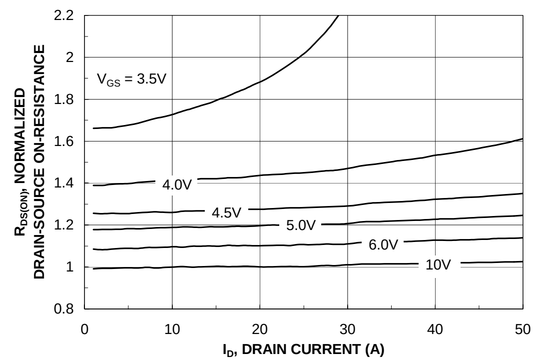


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

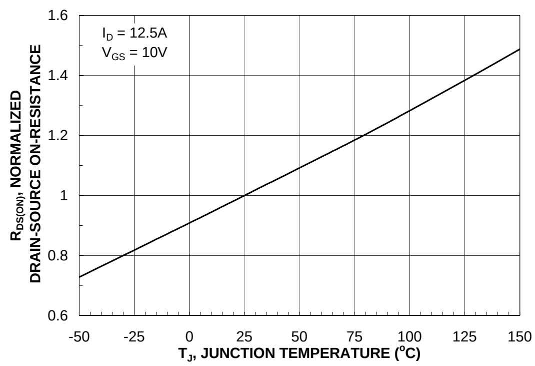


Figure 3. On-Resist ance Variation with Temperature.

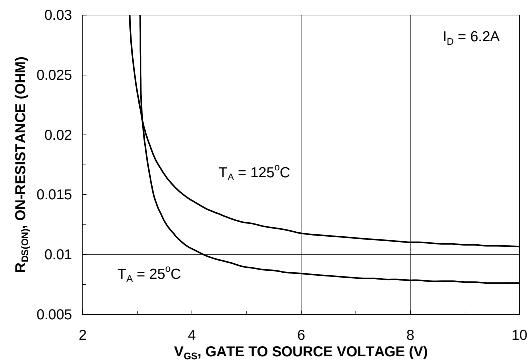


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

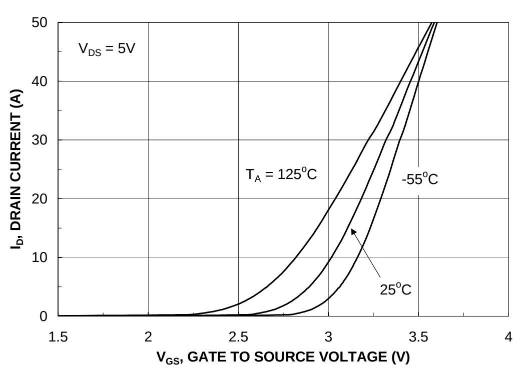


Figure 5. Transfer Characteristics.

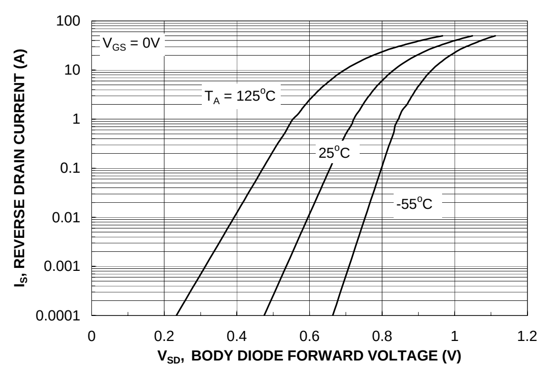


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

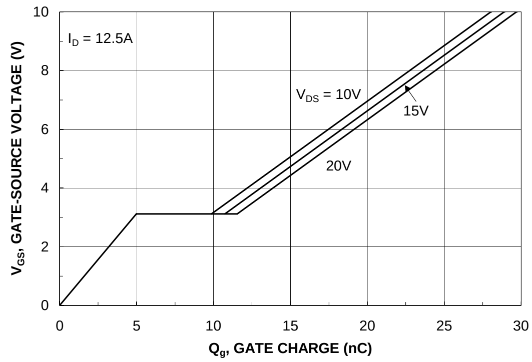


Figure 7. Gate Charge Characteristics.

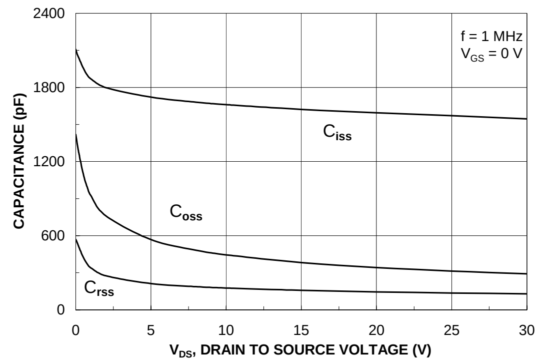


Figure 8. Capacitance Characteristics.

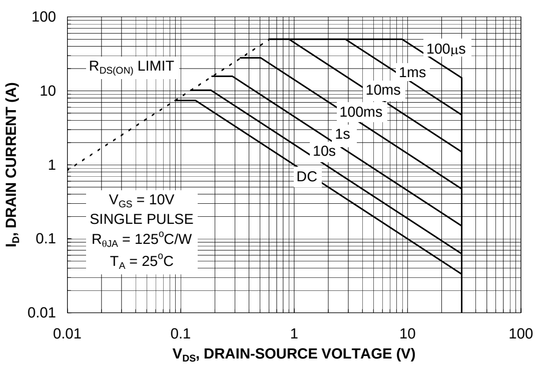


Figure 9. Maximum Safe Operating Area.

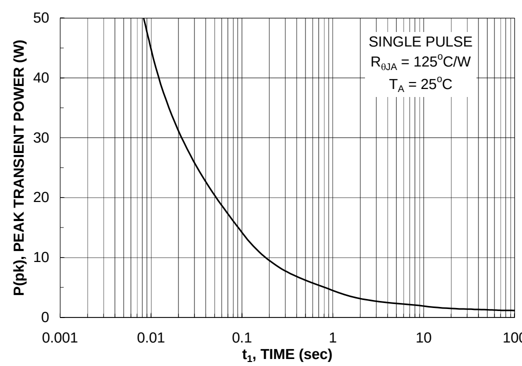


Figure 10. Single Pulse Maximum Power Dissipation.

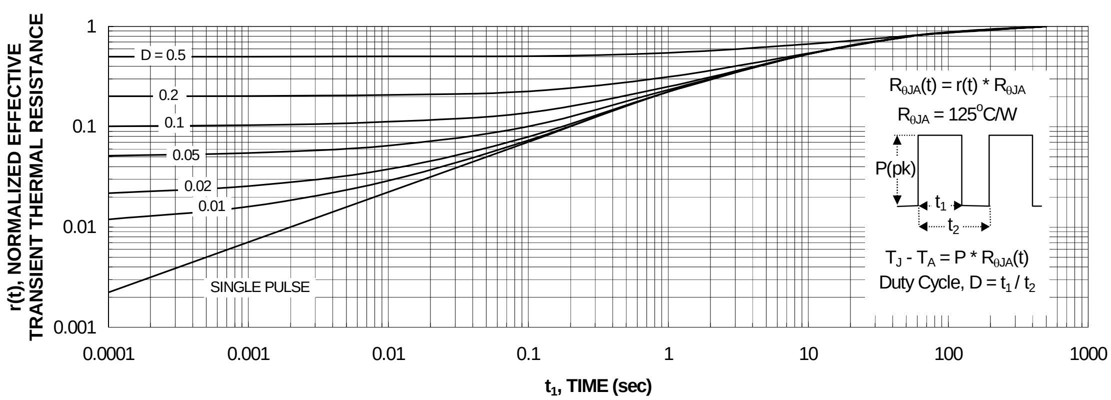


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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