ML610407/ML610408/ML610409

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

ML610407/ML610408/ML610409 is a high performance CMOS 8-bit microcontroller into which peripheral circuits, such as the synchronous serial port, UART, melody driver, RC oscillation type A/D converter, and LCD driver, are incorporated around LAPIS Semiconductor-original 8-bit CPU nX-U8/100. ML610407/ML610408/ML610409 operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.
For industrial use, ML610407P/ML610408P/ML610409P with the extended operating ambient temperature ranging from -40°C to 85°C are available.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@ 32.768 kHz system clock)
    2 μs (@ 500 kHz system clock)
    0.5 μs (@ 2 MHz system clock)

- Internal memory
  - Internal 16KByte maskROM (8K x 16 bits) (including unusable 1KByte TEST area)
  - Internal 1KByte RAM (1024 x 8 bits)

- Interrupt controller
  - 1 non-maskable interrupt source:
    Internal source: 1 (Watchdog Timer)
  - 27 maskable interrupt sources:
    Internal source: 14 (Synchronous serial port 0, Synchronous serial port 1, Timer 0, Timer 1, Timer 2, Timer 3, UART0, Melody 0, RC Oscillation type A/D converter, PWM0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    External source: 13 (P00, P01, P02, P03, P04, P50, P51, P52, P53, P54, P55, P56, P57) *
    *: For P50 to P57, the interrupt sources are ORed into a single interrupt request.

- Time base counter
  - Low-speed time base counter x 1 channel
    Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter x 1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s)

- Timers
  - 8 bits x 4 channels [also available is 16-bit configuration (using Timers 0 and 1, or Timers 2 and 3) x 2 channels]
  - Clock frequency measurement function mode (16-bit configuration using Timers 2 and 3 x 1 channel only)

- Capture
  - Time base capture x 2 channels (4096 Hz to 32 Hz)

- PWM
  - Resolution 16 bits x 1 channel

- Synchronous serial port
  - Master/slave selectable x 2 channels
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 16-bit counter
  - Time division x 2 channels

- General-purpose ports
  - Input-only port: 5 channels (including secondary functions)
  - Output-only port
    ML610407: 12 channels (including secondary functions)
    ML610408: 8 channels (including secondary functions)
    ML610409: 4 channels (including secondary functions)
  - Input/output port: 22 channels (including secondary functions)

- LCD driver
  - Number of segments
    ML610407: Up to 145 dots (select among 29 segments x 5 commons, 30 segments x 4 commons, 31 segments x 3 commons, and 32 segments x 2 commons)
    ML610408: Up to 165 dots (select among 33 segments x 5 commons, 34 segments x 4 commons, 35 segments x 3 commons, and 36 segments x 2 commons)
    ML610409: Up to 185 dots (select among 37 segments x 5 commons, 38 segments x 4 commons, 39 segments x 3 commons, and 40 segments x 2 commons)
  - 1/1 to 1/5 duty
  - 1/2 or 1/3 bias (built-in bias generation circuit)
  - Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected (Cancellation by a mask option is possible)
  - Reset by the watchdog timer (WDT) overflow

•Clock
- Low-speed clock (Operation of this LSI is not guaranteed under a condition with no supply of low-speed crystal oscillation clock)
  Crystal oscillation (32.768 kHz)
- High-speed clock
  Built-in RC oscillation (500 kHz/2 MHz selectable by software)

• Power management
- HALT mode: Suspends the instruction execution by CPU (peripheral circuits are in operating states)
- STOP mode: Stops the low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
- High-speed clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
- Block control function: Completely stops the operation of any function block circuit that is not used (resets registers and stops clock)

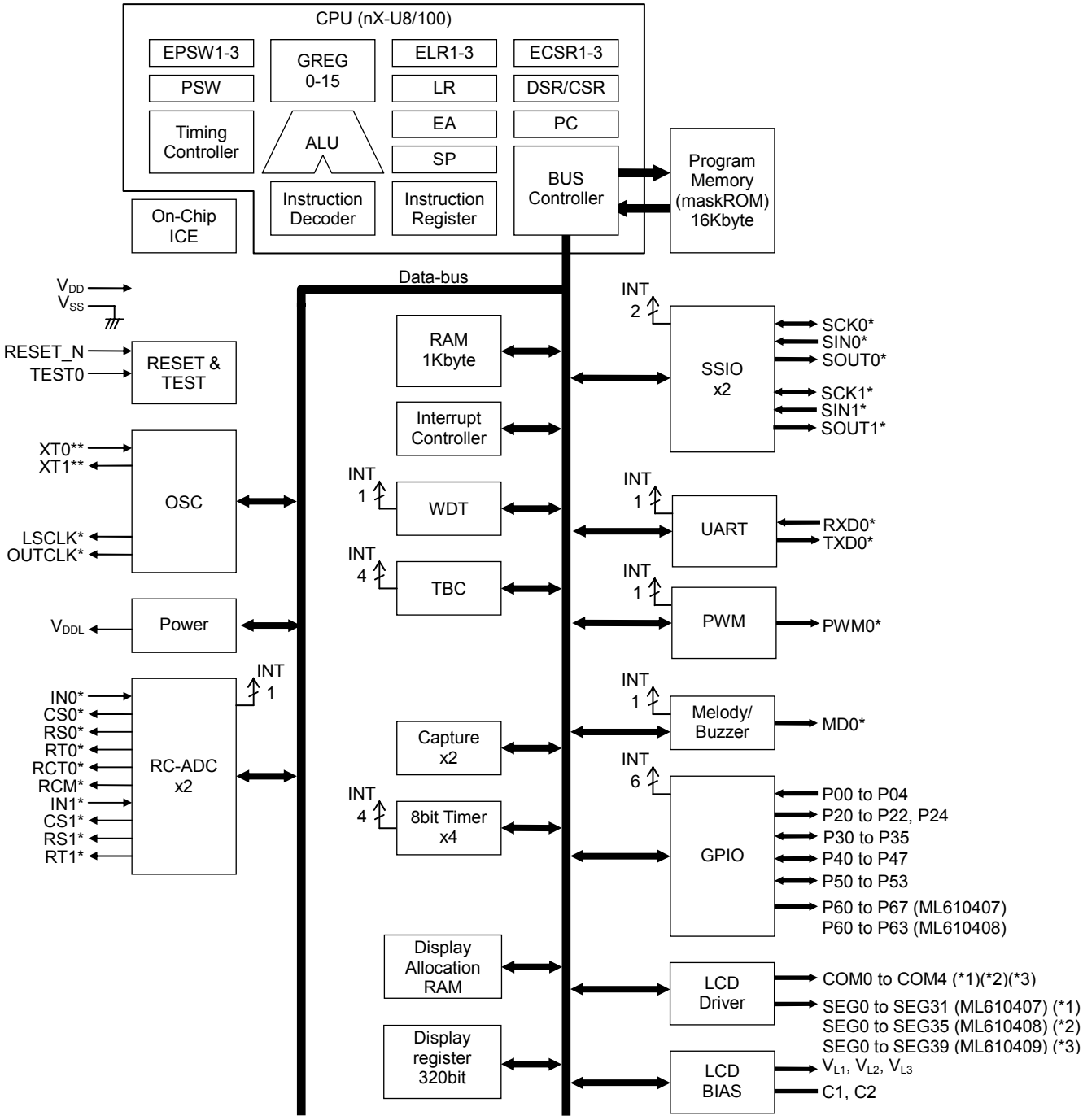
• Shipment
– Chip (Die)
  ML610407-xxxWA
  ML610408-xxxWA
  ML610409-xxxWA
  ML610407P-xxxWA
  ML610408P-xxxWA
  ML610409P-xxxWA
– 100-pin plastic TQFP
  ML610407-xxxTBZ0AAL
  ML610408-xxxTBZ0AAL
  ML610409-xxxTBZ0AAL
  ML610407P-xxxTBZ0AAL
  ML610408P-xxxTBZ0AAL
  ML610409P-xxxTBZ0AAL

xxx: ROM code number (xxx of the blank product is NNN)
P: Wide range temperature version (P version)
WA: Chip (Die)
TBZ0AAL: TQFP

• Guaranteed Operation Range
– Operating temperature: -20°C to +70°C (P version: -40°C to +85°C)
– Operating voltage: V_{DD} = 1.25V to 3.6V

BLOCK DIAGRAM

ML610407/ML610408/ML610409 Block Diagram



* Secondary function or Tertiary function

"*1": Select among 29 segments x 5 commons, 30 segments x 4 commons, 31 segments x 3 commons, and 32 segments x 2 commons with the register

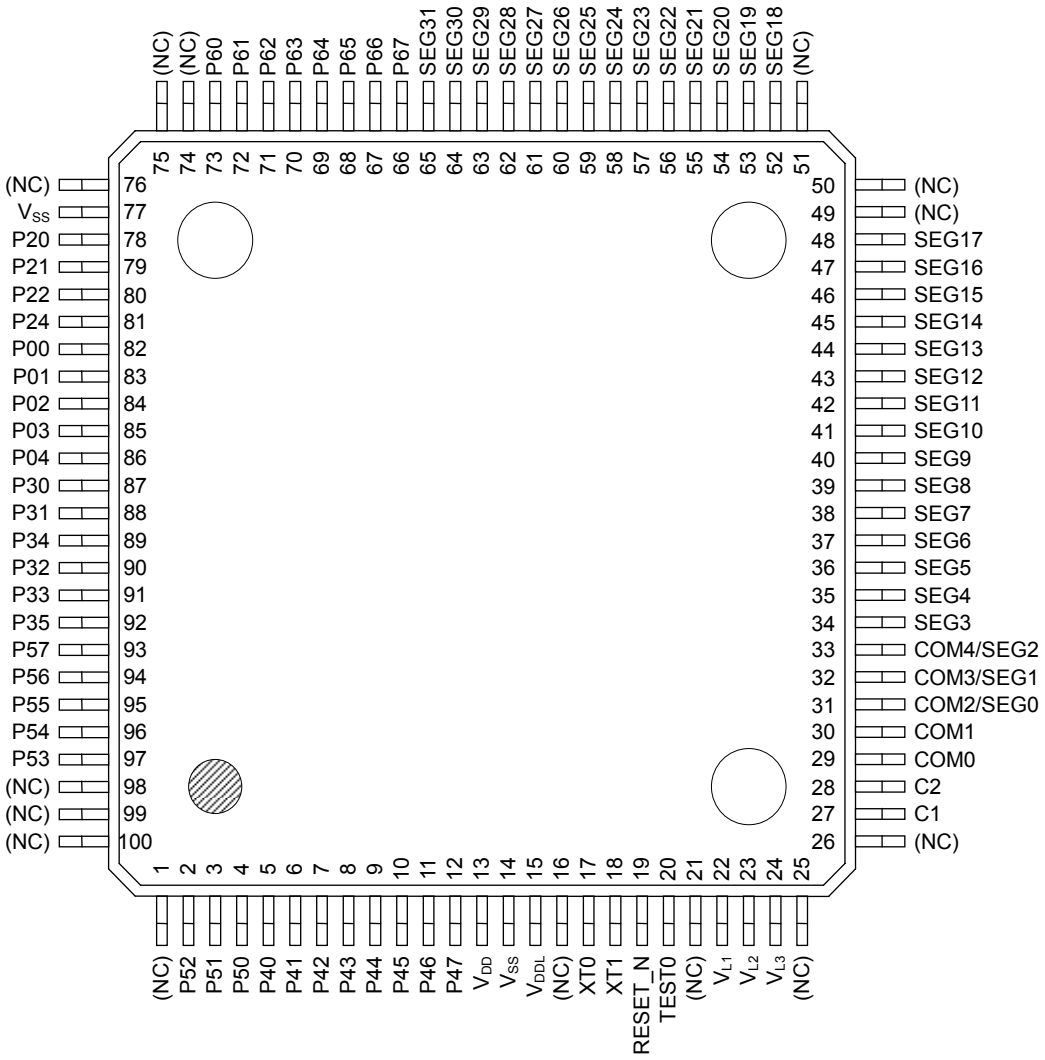
"*2": Select among 33 segments x 5 commons, 34 segments x 4 commons, 35 segments x 3 commons, and 36 segments x 2 commons with the register

"*3": Select among 37 segments x 5 commons, 38 segments x 4 commons, 39 segments x 3 commons, and 40 segments x 2 commons with the register

Figure 1 ML610413P Block Diagram

PACKAGE PIN/CHIP PAD LAYOUT

ML610407 TQFP Package Pin Layout

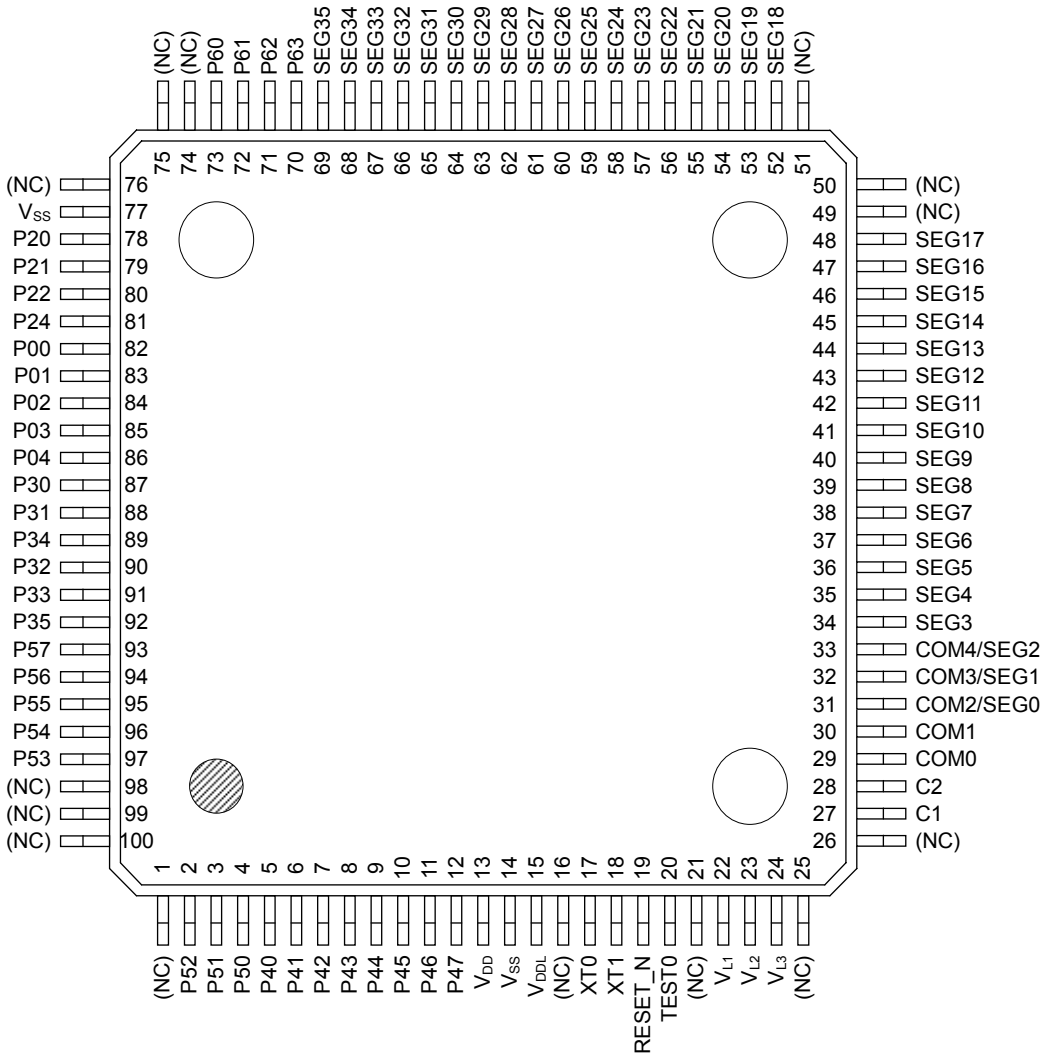


(NC): No Connection

Note:
The assignment of the pads P30 to P35 are not in order.

Figure 2 ML610407 TQFP Package Pin Layout

ML610408 TQFP Package Pin Layout



(NC): No Connection

Note:
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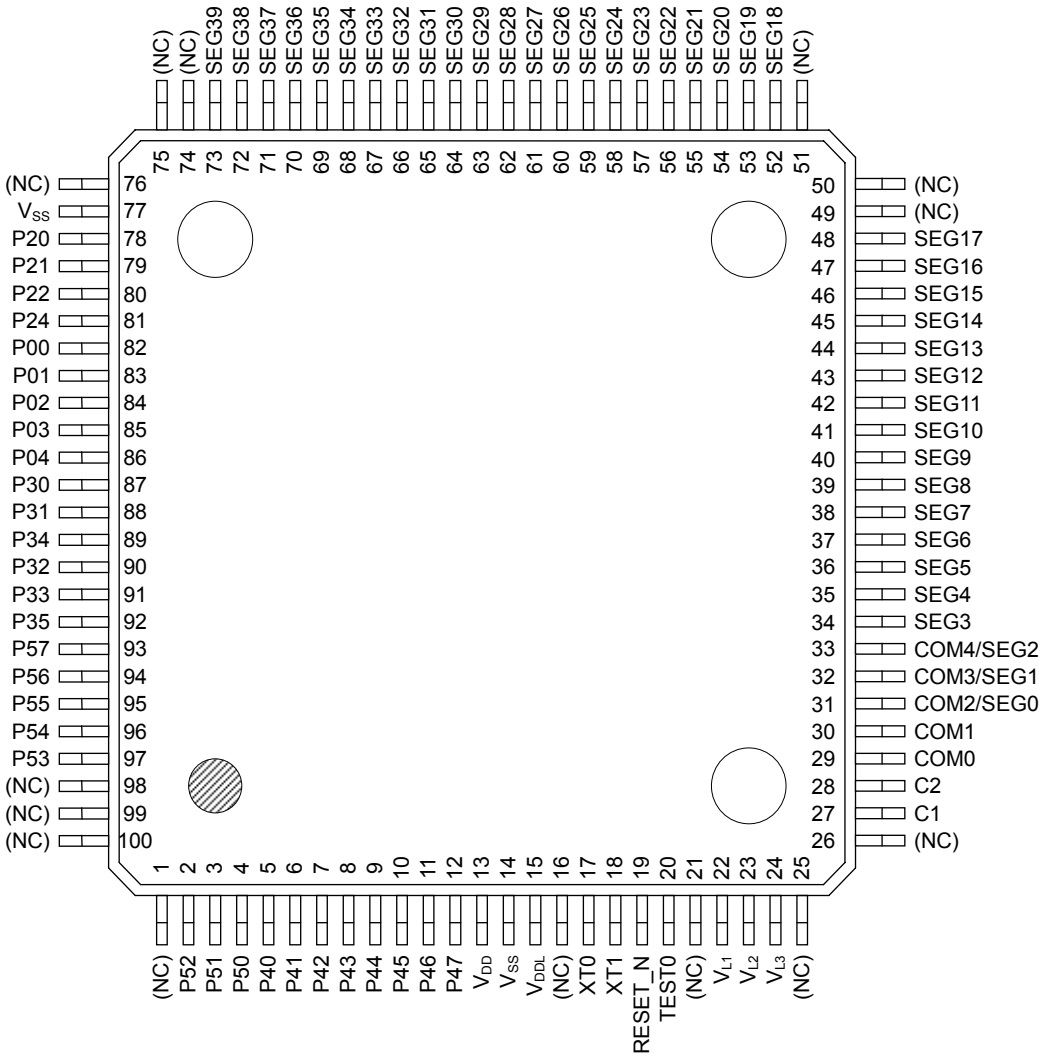
Figure 3 ML610408 TQFP Package Pin Layout

ML610409 TQFP Package Pin Layout

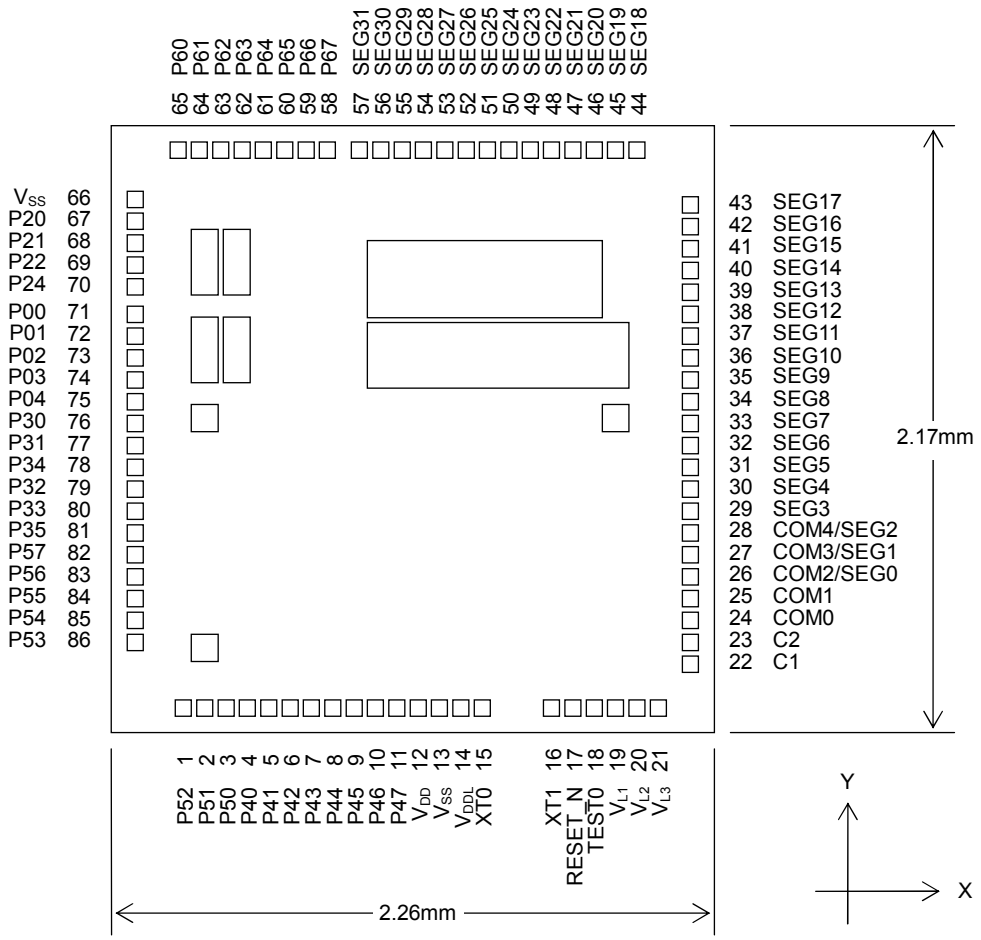


(NC): No Connection

Note:
The assignment of the pads P30 to P35 are not in order.

Figure 4 ML610409 TQFP Package Pin Layout

ML610407 Chip Pad Layout & Dimension

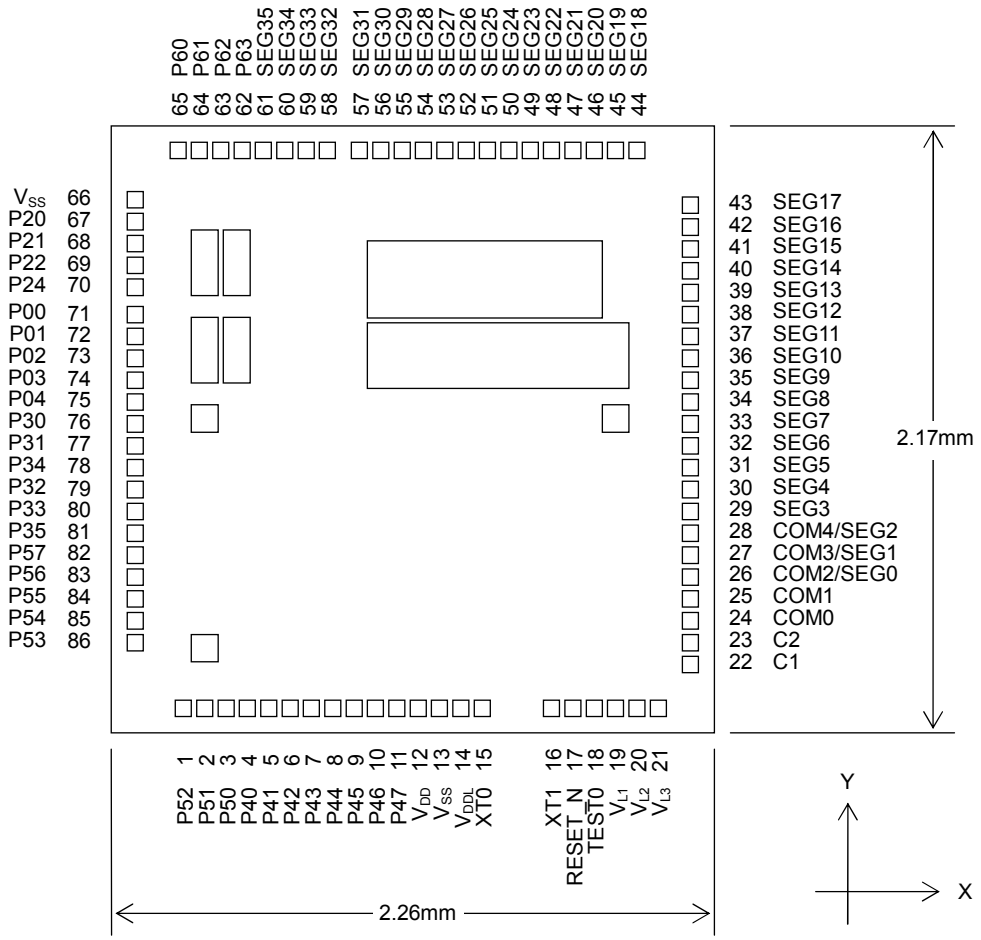


Note:
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.26 mm × 2.17 mm
PAD count: 86 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 5 ML610407 Chip Pin Layout & Dimension

ML610408 Chip Pad Layout & Dimension



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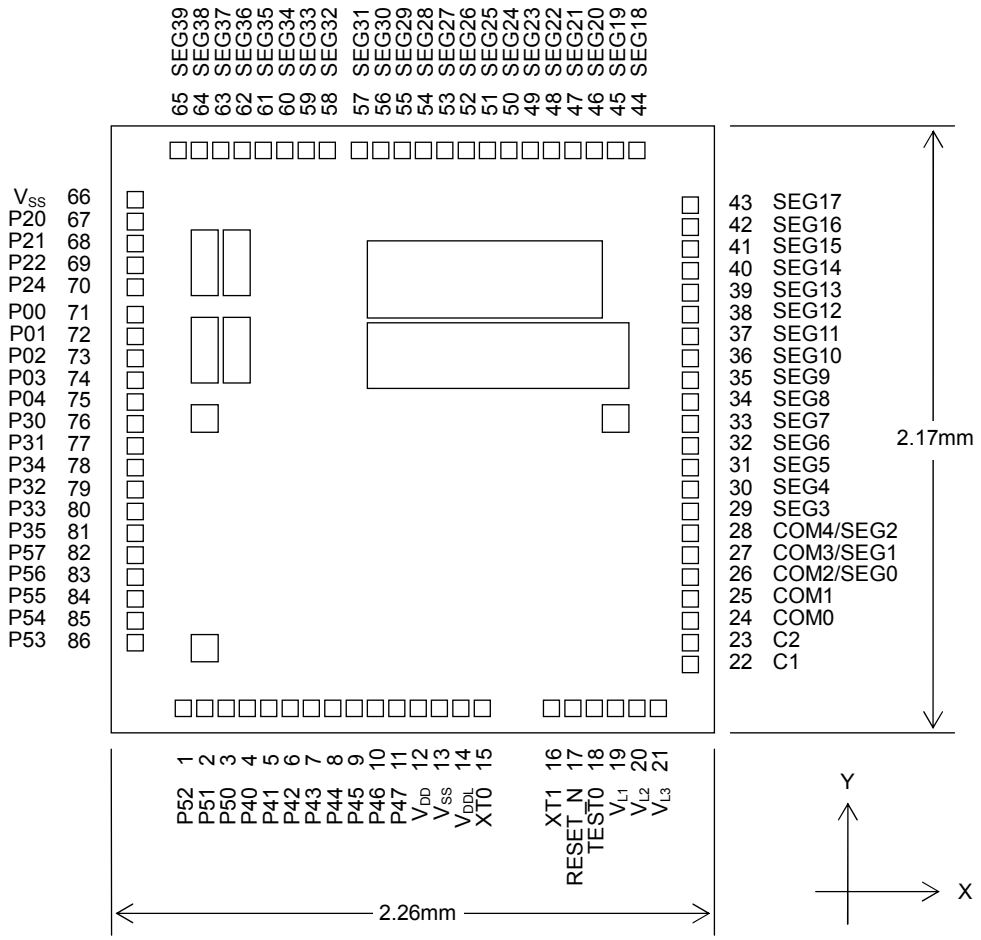
Voltage of the rear side of chip: V_{SS} level.

Figure 6 ML610408 Chip Pin Layout & Dimension

ML610409 Chip Pad Layout & Dimension



Note:
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PAD count: 86 pins
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PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 7 ML610409 Chip Pin Layout & Dimension

PAD COORDINATES

ML610407/ML610408/ML610409 Pad Coordinates

Table 1 ML610407/ML610408/ML610409 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610407/8/9	
		X (µm)	Y (µm)
1	P52	-853	-979
2	P51	-773	-979
3	P50	-693	-979
4	P40	-613	-979
5	P41	-533	-979
6	P42	-453	-979
7	P43	-373	-979
8	P44	-293	-979
9	P45	-213	-979
10	P46	-133	-979
11	P47	-53	-979
12	V_{DD}	27	-979
13	V_{SS}	107	-979
14	V_{DDL}	187	-979
15	XT0	267	-979
16	XT1	427	-979
17	RESET_N	507	-979
18	TEST0	587	-979
19	V_{L1}	667	-979
20	V_{L2}	747	-979
21	V_{L3}	827	-979
22	C1	1024	-845
23	C2	1024	-765
24	COM0	1024	-685
25	COM1	1024	-605
26	COM2/SEG0	1024	-525
27	COM3/SEG1	1024	-445
28	COM4/SEG2	1024	-365
29	SEG3	1024	-285
30	SEG4	1024	-205
31	SEG5	1024	-125
32	SEG6	1024	-45
33	SEG7	1024	35
34	SEG8	1024	115
35	SEG9	1024	195
36	SEG10	1024	275
37	SEG11	1024	355
38	SEG12	1024	435
39	SEG13	1024	515
40	SEG14	1024	595
41	SEG15	1024	675
42	SEG16	1024	755
43	SEG17	1024	835
44	SEG18	840	979
45	SEG19	760	979
46	SEG20	680	979
47	SEG21	600	979

PAD No.	Pad Name	ML610407/8/9	
		X (µm)	Y (µm)
48	SEG22	520	979
49	SEG23	440	979
50	SEG24	360	979
51	SEG25	280	979
52	SEG26	200	979
53	SEG27	120	979
54	SEG28	40	979
55	SEG29	-40	979
56	SEG30	-120	979
57	SEG31	-200	979
58	P67 (*1) SEG32 (*2)(*3)	-295	979
59	P66 (*1) SEG33 (*2)(*3)	-375	979
60	P65 (*1) SEG34 (*2)(*3)	-455	979
61	P64 (*1) SEG35 (*2)(*3)	-535	979
62	P63 (*1)(*2) SEG36 (*3)	-615	979
63	P62 (*1)(*2) SEG37 (*3)	-695	979
64	P61 (*1)(*2) SEG38 (*3)	-775	979
65	P60 (*1)(*2) SEG39 (*3)	-855	979
66	V_{SS}	-1024	842
67	P20	-1024	762
68	P21	-1024	682
69	P22	-1024	602
70	P24	-1024	522
71	P00	-1024	422
72	P01	-1024	342
73	P02	-1024	262
74	P03	-1024	182
75	P04	-1024	102
76	P30	-1024	22
77	P31	-1024	-58
78	P34	-1024	-138
79	P32	-1024	-218
80	P33	-1024	-298
81	P35	-1024	-378
82	P57	-1024	-458
83	P56	-1024	-538
84	P55	-1024	-618
85	P54	-1024	-698
86	P53	-1024	-778

(*1) Pad for ML610407 . (*2) Pad for ML610408. (*3) Pad for ML610409.

PIN LIST

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
14,77	13,66	Vss	—	Negative power supply pin	—	—	—	—
13	12	V_{DD}	—	Positive power supply pin	—	—	—	—
15	14	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—
22	19	V_{L1}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*2)	—	—	—	—
23	20	V_{L2}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*2)	—	—	—	—
24	21	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
27	22	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—
28	23	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—
20	18	TEST0	I/O	Test pin	—	—	—	—
19	17	RESET_N	I	Reset input pin	—	—	—	—
17	15	XT0	I	Low-speed clock oscillation pin	—	—	—	—
18	16	XT1	O	Low-speed clock oscillation pin	—	—	—	—
82	71	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—	—
83	72	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—	—
84	73	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 received data	—	—	—	—
85	74	P03/EXI3	I	Input port, External interrupt	—	—	—	—
86	75	P04/EXI4/ T02P0CK	I	Input port, Timer 0/Timer 2/PWM0 external clock input External interrupt	—	—	—	—
78	67	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
79	68	P21/LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
80	69	P22/LED2	O	Output port	Secondary	MD0	O	Melody 0 output
81	70	P24/LED4	O	Output port	Secondary	PWM0	O	PWM0 output
87	76	P30	I/O	Input/output port	Secondary	IN0	I	RC type ADC0 oscillation input pin
88	77	P31	I/O	Input/output port	Secondary	CS0	O	RC type ADC0 reference capacitor connection pin
89	78	P34	I/O	Input/output port	Secondary	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
90	79	P32	I/O	Input/output port	Secondary	RS0	O	RC type ADC0 reference resistor connection pin
91	80	P33	I/O	Input/output port	Secondary	RT0	O	RC type ADC0 measurement resistor sensor connection pin
92	81	P35	I/O	Input/output port	Secondary	RCM	O	RC type ADC oscillation monitor

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
5	4	P40	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SIN0	I	SSIO0 data input
6	5	P41	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
7	6	P42	I/O	Input/output port	Secondary	RXD0	I	UART data input
					Tertiary	SOUT0	O	SSIO0 data output
8	7	P43	I/O	Input/output port	Secondary	TXD0	O	UART data output
					Tertiary	PWM0	O	PWM0 output
9	8	P44/ T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	Secondary	IN1	I	RC type ADC1 oscillation input pin
					Tertiary	SIN0	I	SSIO0 data input
10	9	P45/T13CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	Secondary	CS1	O	RC type ADC1 reference capacitor connection pin
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
11	10	P46	I/O	Input/output port	Secondary	RS1	O	RC type ADC1 reference resistor connection pin
					Tertiary	SOUT0	O	SSIO0 data output
12	11	P47	I/O	Input/output port	Secondary	RT1	O	RC type ADC1 measurement resistor sensor connection pin
4	3	P50/EXI8	I/O	Input/output port, External interrupt	Secondary	MD0	O	Melody 0 output
					Tertiary	SIN1	I	SSIO1 data input
3	2	P51/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
2	1	P52/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
97	86	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—	—
96	85	P54/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SIN1	I	SSIO1 data input
95	84	P55/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
94	83	P56/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
93	82	P57/EXI8	I/O	Input/output port, External interrupt	—	—	—	—

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
29	24	COM0	O	LCD common pin	—	—	—	—
30	25	COM1	O	LCD common pin	—	—	—	—
31	26	COM2/ SEG0	O	LCD common/segment pin	—	—	—	—
32	27	COM3/ SEG1	O	LCD common/segment pin	—	—	—	—
33	28	COM4/ SEG2	O	LCD common/segment pin	—	—	—	—
34	29	SEG3	O	LCD segment pin	—	—	—	—
35	30	SEG4	O	LCD segment pin	—	—	—	—
36	31	SEG5	O	LCD segment pin	—	—	—	—
37	32	SEG6	O	LCD segment pin	—	—	—	—
38	33	SEG7	O	LCD segment pin	—	—	—	—
39	34	SEG8	O	LCD segment pin	—	—	—	—
40	35	SEG9	O	LCD segment pin	—	—	—	—
41	36	SEG10	O	LCD segment pin	—	—	—	—
42	37	SEG11	O	LCD segment pin	—	—	—	—
43	38	SEG12	O	LCD segment pin	—	—	—	—
44	39	SEG13	O	LCD segment pin	—	—	—	—
45	40	SEG14	O	LCD segment pin	—	—	—	—
46	41	SEG15	O	LCD segment pin	—	—	—	—
47	42	SEG16	O	LCD segment pin	—	—	—	—
48	43	SEG17	O	LCD segment pin	—	—	—	—
52	44	SEG18	O	LCD segment pin	—	—	—	—
53	45	SEG19	O	LCD segment pin	—	—	—	—
54	46	SEG20	O	LCD segment pin	—	—	—	—
55	47	SEG21	O	LCD segment pin	—	—	—	—
56	48	SEG22	O	LCD segment pin	—	—	—	—
57	49	SEG23	O	LCD segment pin	—	—	—	—
58	50	SEG24	O	LCD segment pin	—	—	—	—
59	51	SEG25	O	LCD segment pin	—	—	—	—
60	52	SEG26	O	LCD segment pin	—	—	—	—
61	53	SEG27	O	LCD segment pin	—	—	—	—
62	54	SEG28	O	LCD segment pin	—	—	—	—
63	55	SEG29	O	LCD segment pin	—	—	—	—
64	56	SEG30	O	LCD segment pin	—	—	—	—
65	57	SEG31	O	LCD segment pin	—	—	—	—
66	58	P67(*2)	O	Output port	—	—	—	—
		SEG32(*3)	O	LCD segment pin	—	—	—	—
67	59	P66(*2)	O	Output port	—	—	—	—
		SEG33(*3)	O	LCD segment pin	—	—	—	—
68	60	P65(*2)	O	Output port	—	—	—	—
		SEG34(*3)	O	LCD segment pin	—	—	—	—
69	61	P64(*2)	O	Output port	—	—	—	—
		SEG35(*3)	O	LCD segment pin	—	—	—	—
70	62	P63(*4)	O	Output port	—	—	—	—
		SEG36(*5)	O	LCD segment pin	—	—	—	—
71	63	P62(*4)	O	Output port	—	—	—	—
		SEG37(*5)	O	LCD segment pin	—	—	—	—
72	64	P61(*4)	O	Output port	—	—	—	—
		SEG38(*5)	O	LCD segment pin	—	—	—	—
73	65	P60(*4)	O	Output port	—	—	—	—
		SEG39(*5)	O	LCD segment pin	—	—	—	—

(*1) Internally generated, or connect to either positive power supply pin (V_{DD}) or power supply pin for internal logic (V_{DDL}). For details, see "ML610407/ML610408/ML610409 User's Manual Chapter 22 LCD Drivers."
(*2) Pin for ML610407/ML610408
(*3) Pin for ML610409
(*4) Pin for ML610407
(*5) Pin for ML610408/ML610409

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal resonator is connected to this pin. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS}. (see appendix C measuring circuit 1)	—	—
XT1	O		—	—
LSCLK	O	Low-speed clock output. Assigned to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P04	I	General-purpose input port.	Primary	Positive
General-purpose output port				
P20 to P22, P24	O	General-purpose output port. This cannot be used as the general output port when used as the secondary function.	Primary	Positive
General-purpose input/output port				
P30 to P35	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P40 to P47	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary or tertiary function.	Primary	Positive
P50 to P57	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P60 to P63	O	General-purpose output port. Incorporated only into ML610407/8, and not into ML610409.	Primary	Positive
P64 to P67	O	General-purpose output port. Incorporated only into ML610407, and not into ML610408/ ML610409.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Assigned to the tertiary function of the P51 pin and P54 pin.	Tertiary	—
SIN1	I	Synchronous serial data input pin. Assigned to the tertiary function of the P50 pin and P54 pin.	Tertiary	Positive
SOUT1	O	Synchronous serial data output pin. Assigned to the tertiary function of the P52 pin and P56 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the secondary function of the P24 and tertiary function of the P43 pin.	Secondary Tertiary	Positive
T0P02CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P04 pin and P44 pin.	Primary	—
External interrupt				
EXI0-4	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00 to P04 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. Assigned to the primary function of the P50 to P57 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T0P02CK	I	External clock input pin used for both Timer 0 and Timer 2. This pin is used as the primary function of the P04 pin and P44 pin.	Primary	—
T13CK	I	External clock input pin used for both Timer 1 and Timer 3. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 and P50 pins.	Secondary	Positive/ negative
LED drive				
LED0 to LED2, LED4	O	N-channel open drain output pins to drive LED. This pin is used as the primary function of the P20 to P22 and P24 pins.	Primary	Positive /negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Assigned to the tertiary function of the P51 pin and P54 pin.	Tertiary	—
SIN1	I	Synchronous serial data input pin. Assigned to the tertiary function of the P50 pin and P54 pin.	Tertiary	Positive
SOUT1	O	Synchronous serial data output pin. Assigned to the tertiary function of the P52 pin and P56 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the secondary function of the P24 and tertiary function of the P43 pin.	Secondary Tertiary	Positive
T0P02CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P04 pin and P44 pin.	Primary	—
External interrupt				
EXI0-4	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00 to P04 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. Assigned to the primary function of the P50 to P57 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T0P02CK	I	External clock input pin used for both Timer 0 and Timer 2. This pin is used as the primary function of the P04 pin and P44 pin.	Primary	—
T13CK	I	External clock input pin used for both Timer 1 and Timer 3. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 and P50 pins.	Secondary	Positive/ negative
LED drive				
LED0 to LED2, LED4	O	N-channel open drain output pins to drive LED. This pin is used as the primary function of the P20 to P22 and P24 pins.	Primary	Positive /negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0 to COM4	O	Common output pins. COM2, COM3, and COM4 can be switched to SEG0, SEG1, and SEG2, respectively, through the register setting. To change the setting, switch between COM4 and SEG2 for one pin and switch between COM3, COM4 and SEG1, SEG2 for two pins.	—	—
SEG0 to SEG23	O	Segment output pin. The SEG0, SEG1, and SEG2 pins are for switching the register setting with the COM2, COM3, and COM4.	—	—
SEG24 to SEG27	O	Segment output pin. Incorporated into ML610408/ML610409, not into ML610407.	—	—
SEG28 to SEG31	O	Segment output pin. Incorporated into ML610409, not into ML610407/ML610408.		
LCD driver power supply				
V_{L1}	—	Power supply pin for LCD bias (internally generated) or power supply connection pin. Depending on LCD Bias setting and V_{DD} voltage level, V_{DD} or V_{DDL} or capacitor is connected. For details of the connection method, see Chapter 22, "LCD Drivers".	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitor C_{12} (see Appendix C measuring circuit 1) is connected between C1 and C2.	—	—
C2	—		—	—

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Test				
TEST0	I/O	Pin for testing. A pull-down resistor is internally connected.	—	Positive
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors C_{L0} and C_{L1} (see Appendix C measuring circuit 1) are connected between this pin and V_{SS}.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin handling
VL1	Open
VL2	Open
VL3	Open
C1, C2	Open
RESET_N	Open
TEST0	VSS
P00 to P04	VDD or VSS
P20 to P22, P24	Open
P30 to P35	Open
P40 to P47	Open
P50 to P57	Open
P60 to P67	Open
COM0 to COM4	Open
SEG0 to SEG39	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS}= 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	-0.3 to +4.6	V
Power supply voltage 2	V_{DDL}	Ta=25°C	-0.3 to +3.6	V
Power supply voltage 3	V_{L1}	Ta=25°C	-0.3 to +2.0	V
Power supply voltage 4	V_{L2}	Ta=25°C	-0.3 to +4.0	V
Power supply voltage 5	V_{L3}	Ta=25°C	-0.3 to +6.0	V
Input voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	-0.3 to V_{DD}+0.3	V
output current 1	I_{OUT1}	Port 3 to 6, Ta=25°C	-12 to +11	mA
Output current 2	I_{OUT2}	Port 2, Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{STG}	—	-55 to +150	°C

Recommended Operating conditions

(V_{SS}= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	without P version	-20 to +70	°C
		P version	-40 to +85	
Operating voltage	V_{DD}	f_{OP}=30k to 625kHz	1.25 to 3.6	V
		f_{OP}=30k to 2.5MHz	1.8 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD}=1.25 to 3.6V	30k to 625k	Hz
		V_{DD}=1.8 to 3.6V	30k to 2.5M	
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitance	C_{DL}	—	3 to 18	pF
	C_{GL}	—	3 to 18	
V_{DD} pin external capacitance	C_V	—	1.0±30% to 2.2±30%*1	µF
V_{DDL} pin external capacitance	C_L	—	0.47±30% to 2.2±30%*2	µF
$V_{L1, 2, or 3}$ pin external capacitance	$C_{a,b,c}$	—	0.1±30%	µF
Pin-to-pin (C1 to C2) external capacitance	C_{12}	—	0.47±30%	µF

*1: Please select as C_V is larger than C_L or same as C_L.
*2: When the load of VDD is small and the power rise time is too short, it may happen that the power-on reset is not generated. In this case please select C_L with larger capacitance

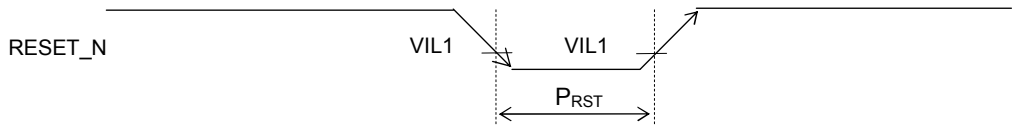
DC Characteristics (1/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

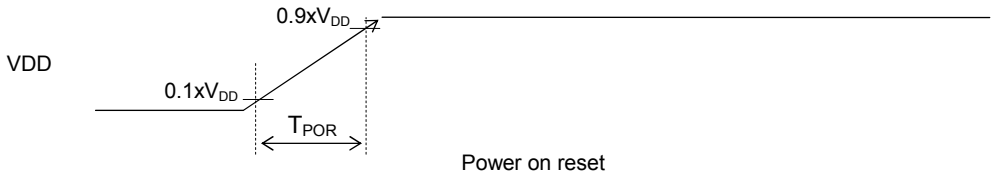
Parameter	Symbol	Condition		Rating			Unit	Measurement circuit
				Min.	Typ.	Max.		
500kHz/2MHz RC oscillation frequency	f_{RC}	V_{DD}=1.25 to 3.6V	Ta=25°C	Typ. -10%	500	Typ. +10%	kHz	1
			*3	Typ. -25%	500	Typ. +25%	kHz	
		V_{DD}=1.8 to 3.6V	Ta=25°C	Typ. -10%	2.0	Typ. +10%	MHz	
			*3	Typ. -25%	2.0	Typ. +25%	MHz	
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.6	2	s	
500kHz/2MHz RC oscillation start time	T_{RC}	—		—	—	3	µs	
Low-speed oscillation stop detect time*1	T_{STOP}	—		12	16.4	41	ms	
Reset pulse width	P_{RST}	—		200	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset generated power rise time	T_{POR}	—		—	—	10	ms	

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.
*2: 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=12pF).
*3: Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)

RESET



RESET_N pin reset



Power on reset

DC Characteristics (2/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
V_{DDL} voltage	V_{DDL}	fop=30k to 625kHz	1.1	1.2	1.3	V	1
		fop=30k to 2.5MHz	1.35	1.5	1.65		
V_{DDL} temperature deviation *1	ΔV_{DDL}	V_{DD}=3.0V	—	-1	—	mV/°C	
V_{DDL} voltage dependency *1	ΔV_{DDL}	—	—	5	20	mV/V	

*1: The maximum V_{DDL} voltage becomes the V_{DD} voltage level when the V_{DDL} voltage determined by the temperature and voltage deviations mathematically exceeds the V_{DD} voltage.

DC Characteristics (3/5)

(VDD=3.0V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measurement circuit
				Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/High-speed oscillation: stopped.	Ta=25°C	—	0.4	0.8	μA	1
			*5	—	—	6.5		
Supply current 2	IDD2	CPU: In HALT state. (LTBC, WDT: Operating)*3*4. High-speed 500kHz/2MHz oscillation: Stopped. LCD/BIAS circuits: Operating *6	Ta=25°C	—	0.9	1.8	μA	
			*5	—	—	7.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz/2MHz oscillation: Stopped, LCD/BIAS circuits: Operating *2	Ta=25°C	—	4.0	7.5	μA	
			*5	—	—	11.0		
Supply current 4-1	IDD4-1	CPU: In 500kHz RC operating state. LCD/BIAS circuits: Operating.*2	Ta=25°C	—	60	80	μA	
			*5	—	—	90		
Supply current 4-2	IDD4-2	CPU: In 2MHz RC operating state. LCD/BIAS circuits: Operating.*2	Ta=25°C	—	240	300	μA	
			*5	—	—	320		

*1: When the CPU operating rate is 100% (no HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : 32.768KHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)
*4 : Significant bits of BLKCON0 to BLKCON4 registers are all "1" except DLCD bit on BLKCON4.
*5 : Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)
*6: LCD stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC Characteristics (4/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20 to P22, P24 (N-channel open drain output mode is not selected)) (P30 to P35) (P40 to P47) (P50 to P57) (P60 to P63) *1 *2 (P64 to P67) *1	VOH1	IOH1=-0.5mA, V_{DD}=1.8 to 3.6V	V_{DD} -0.5	—	—	V	2
		IOH1=-0.03mA, V_{DD}=1.25 to 3.6V	V_{DD} -0.3	—	—		
	VOL1	IOL1=+0.5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
		IOL1=+0.1mA, V_{DD}=1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20 to P22, P24 (N-channel open drain output mode is selected))	VOL2	IOL2=+5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0 to 4) (SEG0 to 31) *1 (SEG0 to 35) *2 (SEG0 to 39) *3	VOH3	IOH3=-0.05mA, VL1=1.2V	V_{L3} -0.2	—	—		
	VOML3	IOML3=+0.05mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOML3S	IOML3S=-0.05mA, VL1=1.2V	V_{L2} -0.2	—	—		
	VOLM3	IOLM3=+0.05mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOLM3S	IOLM3S=-0.05mA, VL1=1.2V	V_{L1} -0.2	—	—		
	VOL3	IOL3=+0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20 to P22,P24) (P30 to P35) (P40 to P47) (P50 to P57) (P60 to P63) *1 *2 (P60 to P67) *1	IOOH	VOH=V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL=V_{SS} (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	2	300	600		
	IIL2	VIL2=V_{SS}	-1	—	—		
Input current 3 (P00 to P04) (P30 to P35) (P40 to P47) (P50 to P57)	IIH3	VIH3=V_{DD}, V_{DD}=1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3=V_{DD}, V_{DD}=1.25 to 3.6V (when pulled-down)	0.01	30	200		
	IIL3	VIL3=V_{SS}, V_{DD}=1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3=V_{SS}, V_{DD}=1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3=V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3=V_{SS} (in high-impedance state)	-1	—	—		

*1: Characteristics for ML610407.
*2: Characteristics for ML610408.
*3: Characteristics for ML610409.

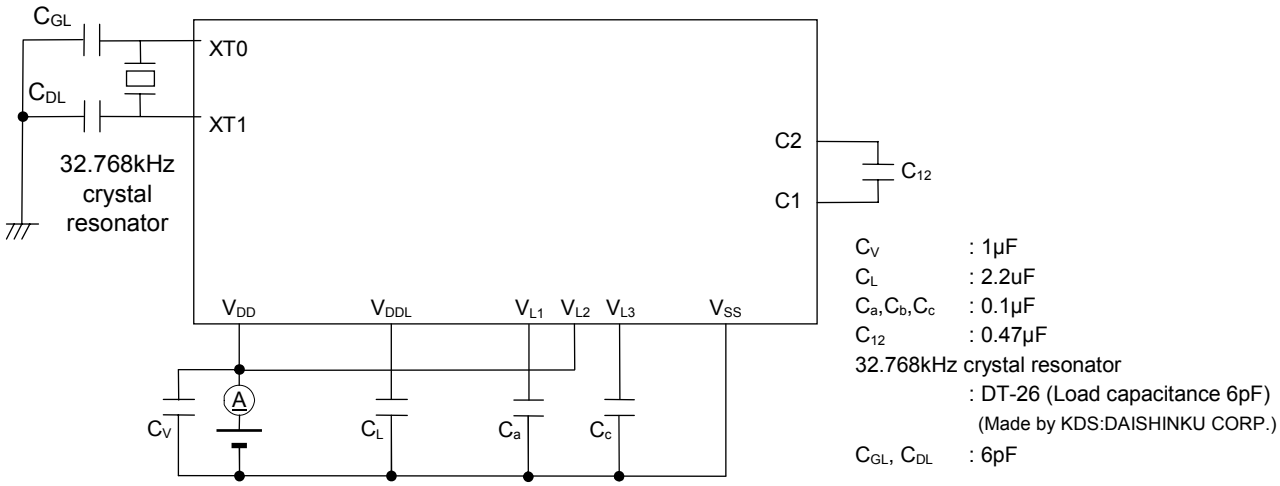
DC Characteristics (5/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0, TEST1_N) (P00 to P04) (P30 to P35) (P40 to P47) (P50 to P57)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD}=1.8 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD}=1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00 to P04) (P30 to P35) (P40 to P47) (P50 to P57)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	5	pF	—

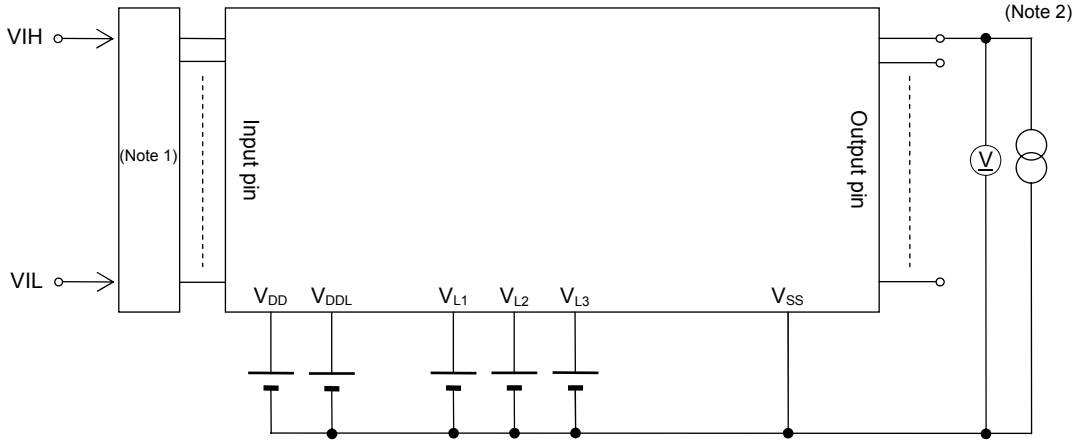
Measuring Circuits

Measuring Circuit 1



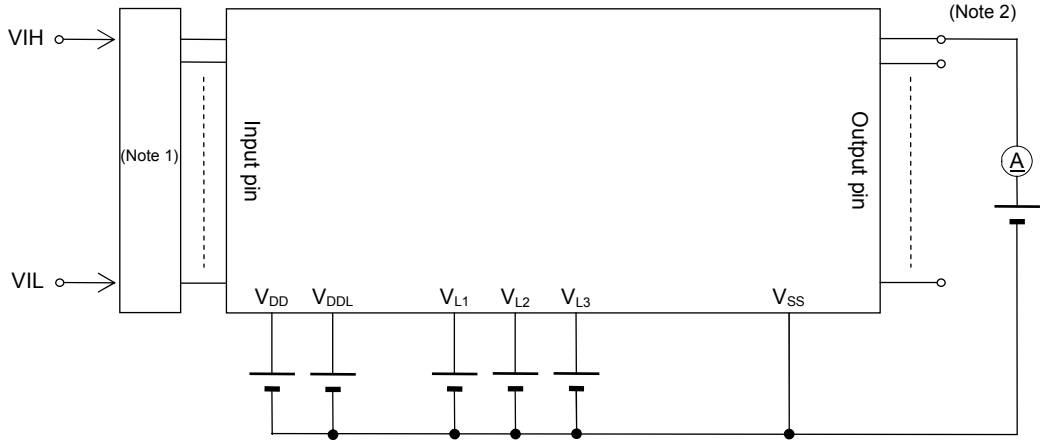
C_V : 1µF
C_L : 2.2uF
C_a,C_b,C_c : 0.1µF
C_{12} : 0.47µF
32.768kHz crystal resonator
: DT-26 (Load capacitance 6pF)
(Made by KDS:DAISHINKU CORP.)
C_{GL}, C_{DL} : 6pF

Measuring Circuit 2



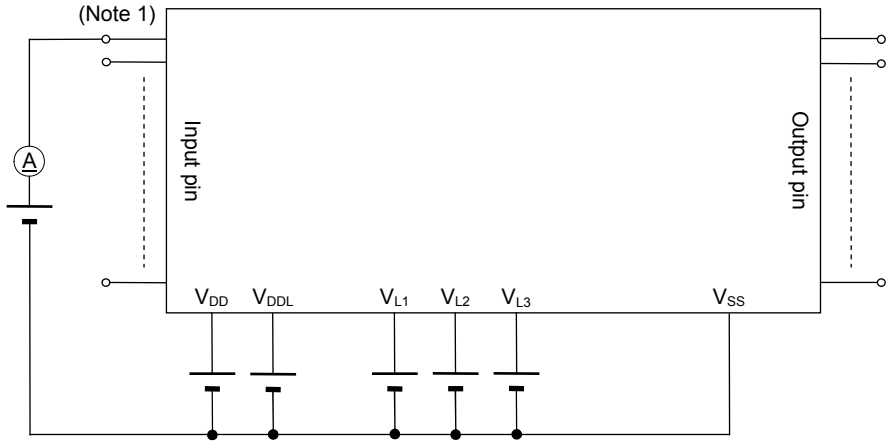
(Note 1) Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin

Measuring Circuit 3



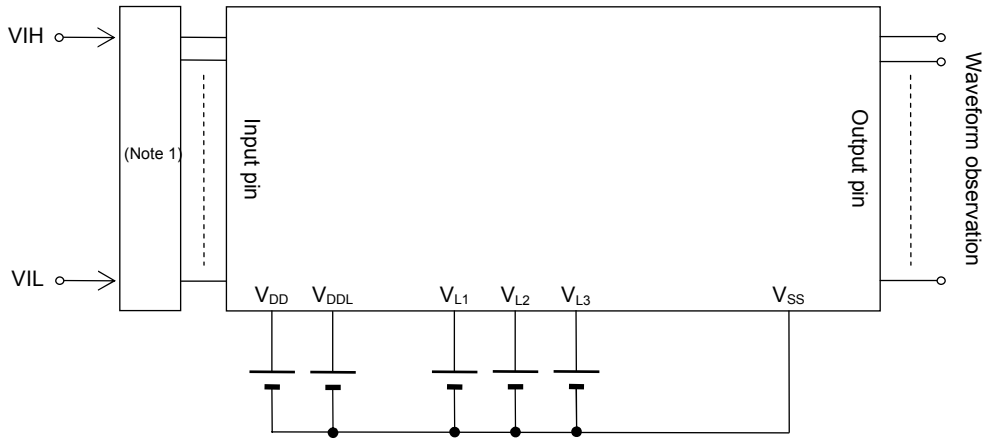
(Note 1) Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin

Measuring Circuit 4



(Note 1) Repeats for the specified input pin

Measuring Circuit 5

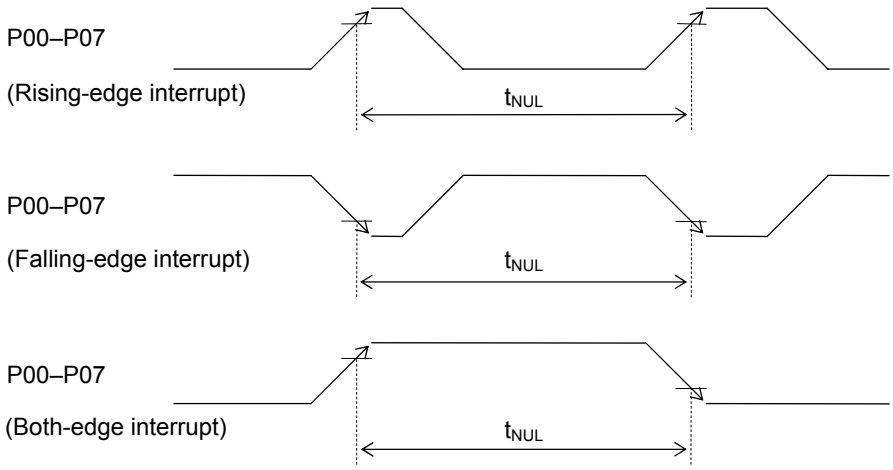


(Note 1) Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

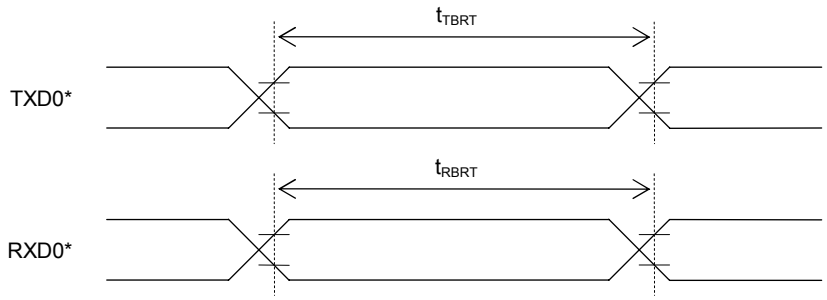


AC Characteristics (UART)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] -3%	BRT*[1]	BRT*[1] +3%	s

*[1]: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



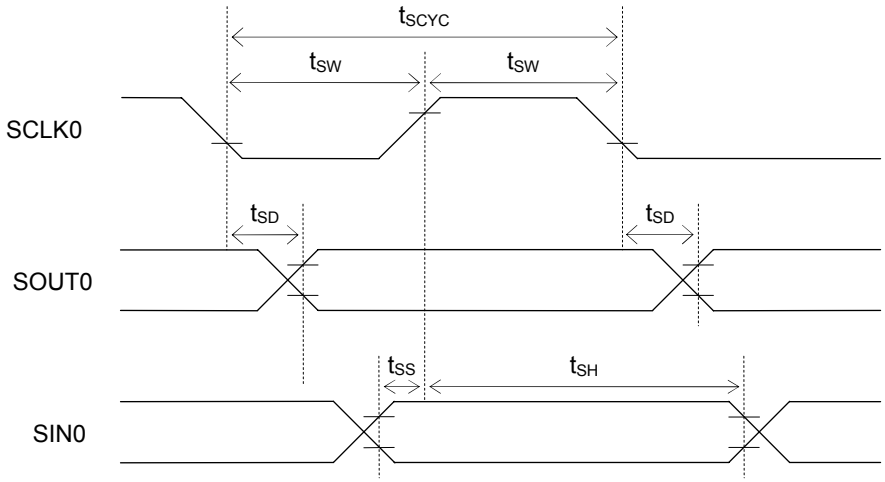
*: Indicates the secondary function of the port.

AC Characteristics (Synchronous Serial Port)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	In the 500kHz oscillation mode*2	10	—	—	µs
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	1	—	—	µs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*1	—	s
SCLK input pulse width (slave mode)	t_{SW}	In the 500kHz oscillation mode*2	4	—	—	µs
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	0.4	—	—	µs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	In the 500kHz oscillation mode*2 Output load 10pF	—	—	500	ns
		In the 2MHz oscillation mode*3 Output load 10pF	—	—	240	
SOUT output delay time (master mode)	t_{SD}	In the 500kHz oscillation mode*2 Output load 10pF	—	—	500	ns
		In the 2MHz oscillation mode*3 Output load 10pF, V_{DD}=1.8 to 3.6V	—	—	240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	In the 500kHz oscillation mode*2	500	—	—	ns
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	240	—	—	
SIN input hold time	t_{SH}	In the 500kHz oscillation mode*2	300	—	—	ns
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	80	—	—	

*1: Clock cycle selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)
*2: When 500kHz oscillation is selected with RCM of the frequency control register 0 (FCON0)
*3: When 2MHz oscillation is selected with RCM of the frequency control register 0 (FCON0)



*: Indicates the secondary function of the port

AC Characteristics (RC Oscillation A/D Converter)

Condition for V_{DD}=1.8 to 3.6V

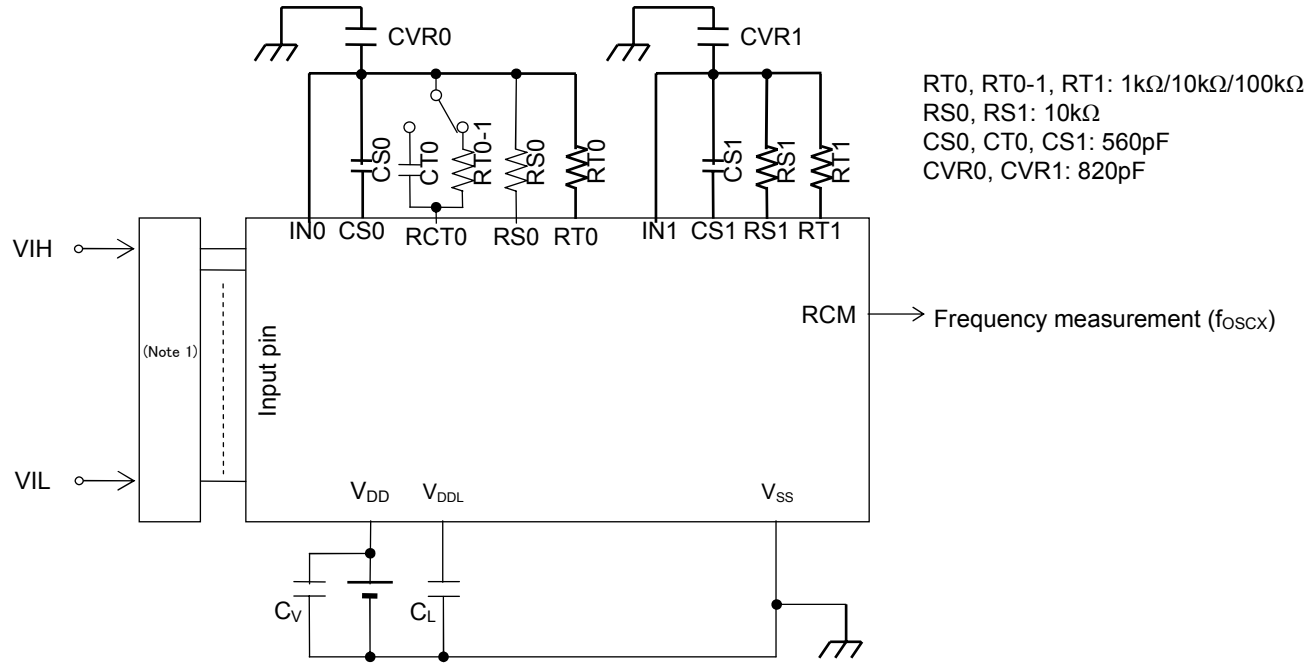
(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=1kΩ	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10kΩ	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100kΩ	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1=1kΩ	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.981	1	1.019	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.099	0.101	0.104	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCX}(\text{RT0-CS0 oscillation})}{f_{OSCX}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCX}(\text{RT0-1-CS0 oscillation})}{f_{OSCX}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCX}(\text{RT1-CS1 oscillation})}{f_{OSCX}(\text{RS1-CS1 oscillation})}$$

(x = 1, 2, 3)



*1: Input logic circuit to determine the specified measuring conditions.

Condition for V_{DD}=1.25 to 3.6V

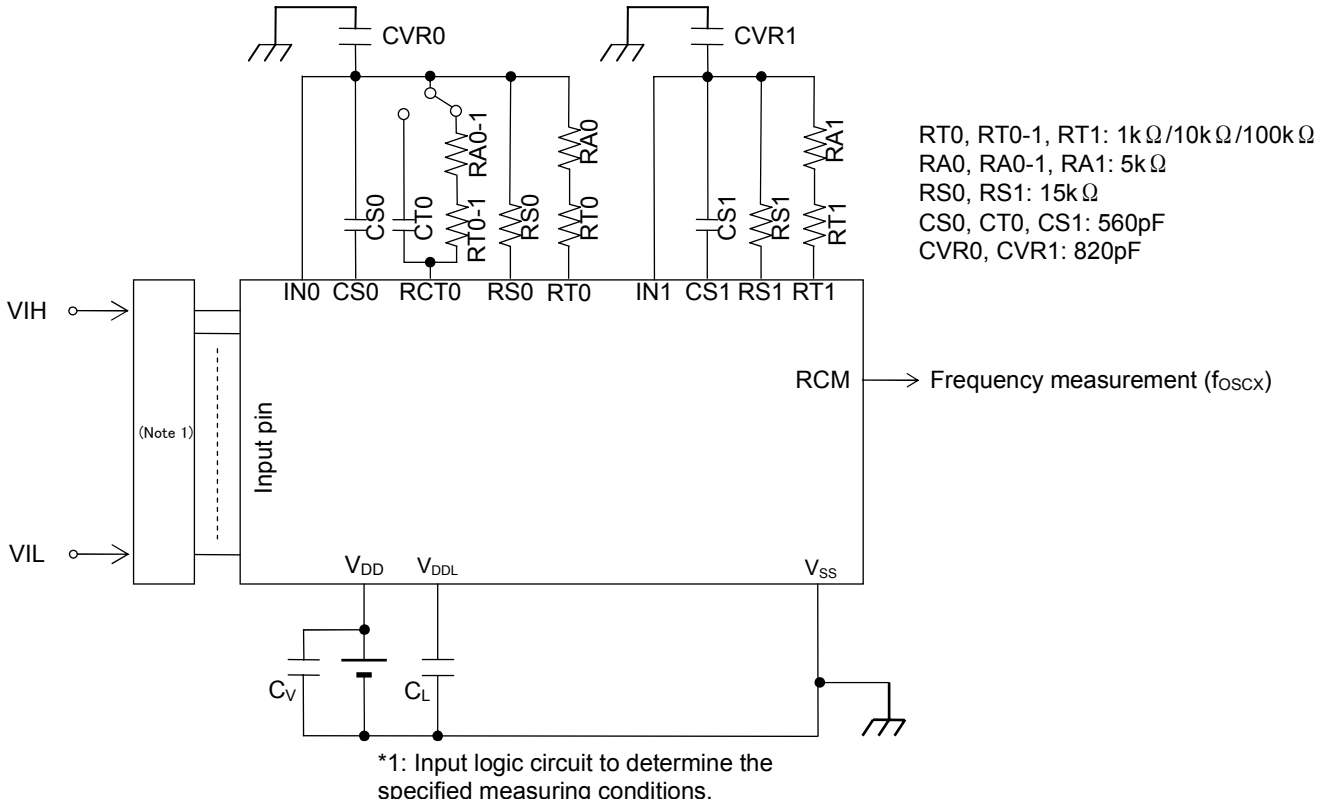
(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 1.5V	f_{OSC1}	Resistor for oscillation=6kΩ	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 1.5V	Kf1	RT0, RT0-1, RT1=1kΩ	2.139	2.381	2.632	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.973	1	1.028	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.142	0.147	0.152	—
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=6kΩ	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1=1kΩ	2.227	2.432	2.626	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.982	1	1.018	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.141	0.145	0.149	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(\text{RT0-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCx}(\text{RT0-1-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCx}(\text{RT1-CS1 oscillation})}{f_{OSCx}(\text{RS1-CS1 oscillation})}$$

(x = 1, 2, 3)



*1: Input logic circuit to determine the specified measuring conditions.

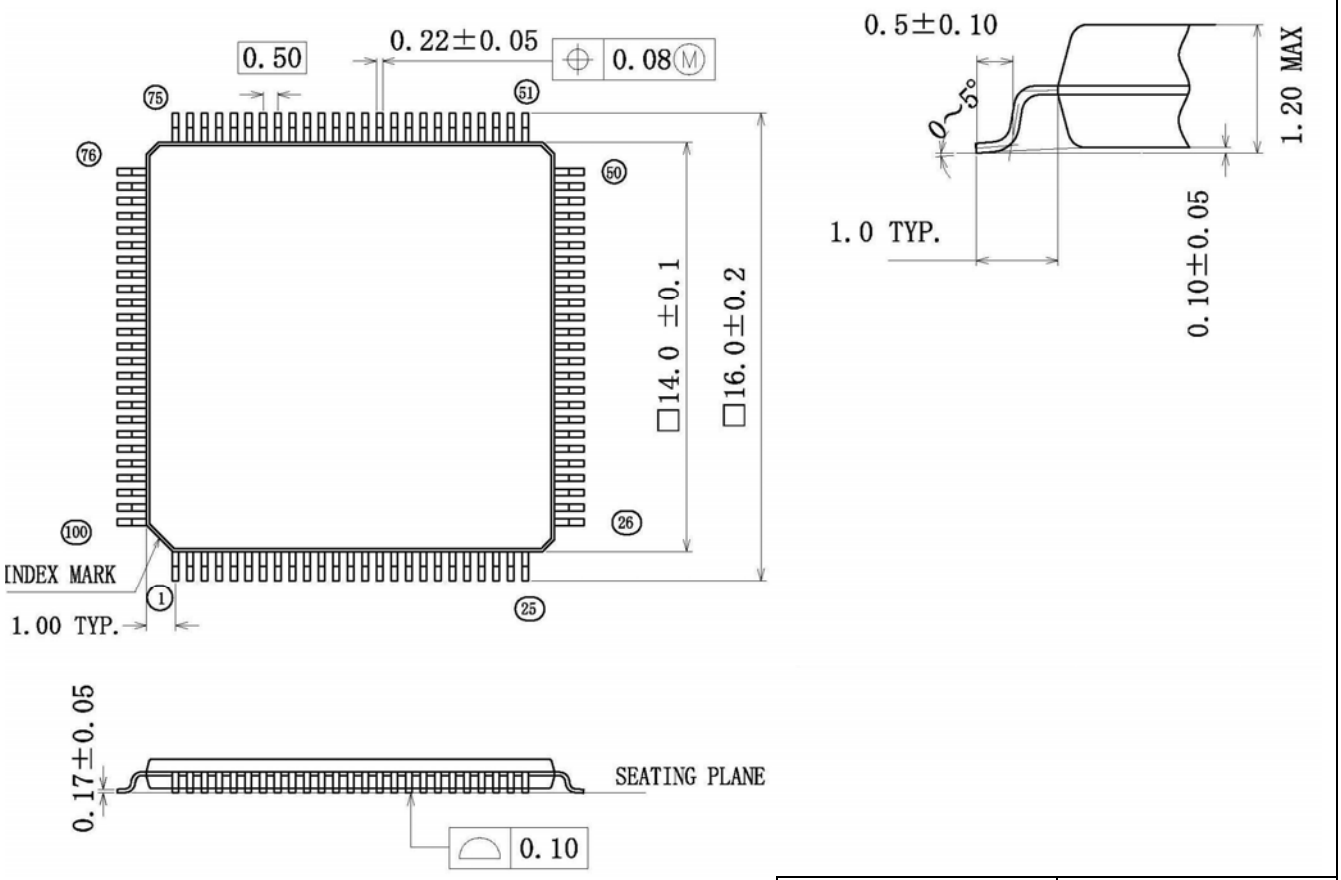
Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wiring between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have V_{SS}(GND) trace next to the signal.
- Please make wiring to components (capacitor, resistor, and so on) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

PACKAGE DIMENSIONS

(Unit: mm)

P-TQFP100-1414-0.50-TK



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn / 2Bi
Solder thickness	More than 5μm
Package weight (g)	-
Rev. No./Last Revised	3/ Nov.11,2012

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVESION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610409-01	Mar.7,2011	–	–	Formally edition 1
FEDL610409-02	Mar.30,2011	23	23	The supply current was changed.
FEDL610409-03	Mar.30,2011	23	23	Correct the supply current.
FEDL610409-04	Mar.27,2012	21,26	21,26	The value of capacitor CL was changed to 2.2uF.
FEDL610409-05	Jul.18,2012	20	20	The termination of the TEST0 was changed from OPEN to VSS.
		21	21	The notes about C_V, C_L were added.
		3, 34	3, 34	The package dimension was changed.

NOTES

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