FAIRCHILD SEMICONDUCTOR®

October 2013

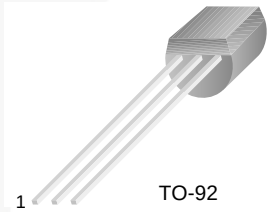
FJN4303R
PNP Epitaxial Silicon Transistor

Features

- Switching Circuit, Inverter, Interface Circuit, Driver Circuit
- Built-in Bias Resistor (R_1 = 22 kΩ, R_2 = 22 kΩ)
- Complement to FJN3303R

Application

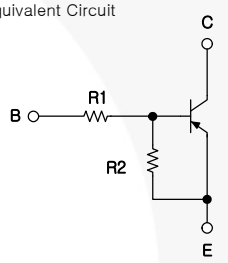
- Switching Application (Integrated Bias Resistor)



TO-92

1. Emitter 2. Collector 3. Base

Equivalent Circuit



Ordering Information

Part Number	Top Mark	Package	Packing Method
FJN4303RTA	R4303	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	-50	V
V_{CEO}	Collector-Emitter Voltage	-50	V
V_{EBO}	Emitter-Base Voltage	-10	V
I_C	Collector Current	-100	mA
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 to 150	°C

Thermal Characteristics[1]

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	300	mW
	Derate Above T_A = 25°C	2.4	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	416	°C/W

Note:

1. PCB Board Size: FR-4 76 x 114 x 0.6T mm^3(3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted**.**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = -10 μA, I_E = 0	-50			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = -100 μA, I_B = 0	-50			V
I_{CBO}	Collector Cut-Off Current	V_{CB} = -40 V, I_E = 0			-0.1	μA
h_{FE}	DC Current Gain	V_{CE} = -5 V, I_C = -5 mA	56			
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = -10 mA, I_B = -0.5 mA			-0.3	V
f_T	Current Gain Bandwidth Product	V_{CE} = -10 V, I_C = -5 mA		200		MHz
C_{ob}	Output Capacitance	V_{CB} = -10 V, I_E = 0, f = 1.0 MHz		5.5		pF
$V_{I(off)}$	Input Off Voltage	V_{CE} = -5 V, I_C = -100 μA			-0.5	V
$V_{I(on)}$	Input On Voltage	V_{CE} = -0.3 V, I_C = -5 mA	-3.0			V
R_1	Input Resistor		15	22	29	kΩ
R_1/R_2	Resistor Ratio		0.9	1.0	1.1	

Typical Performance Characteristics

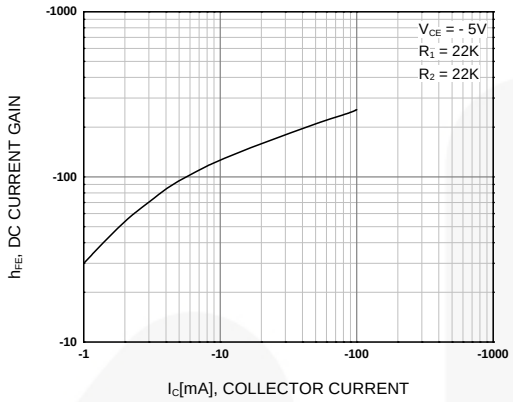


Figure 1. DC Current Gain

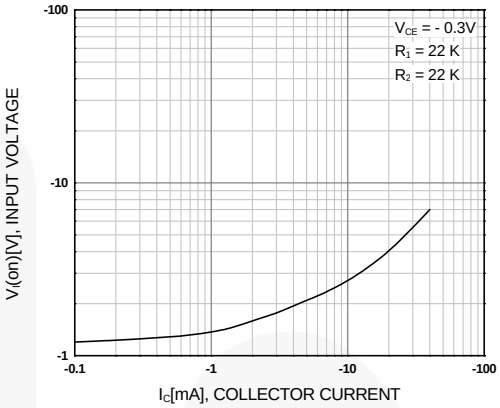


Figure 2. Input On Voltage

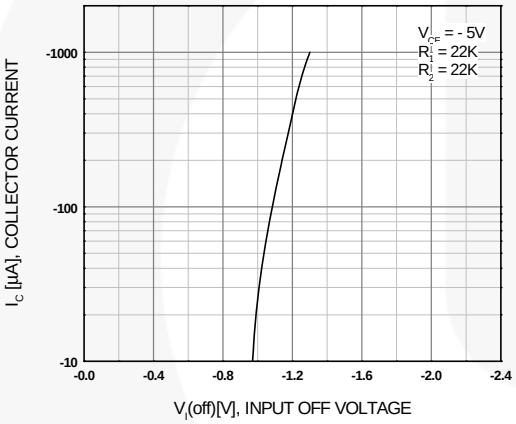


Figure 3. Input Off Voltage

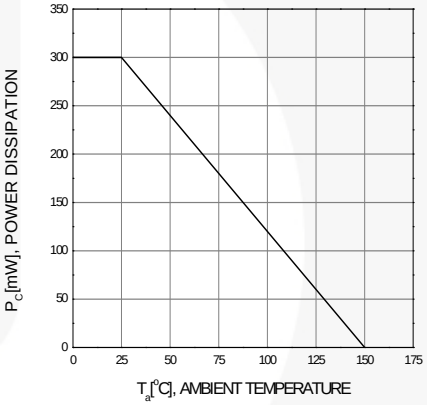
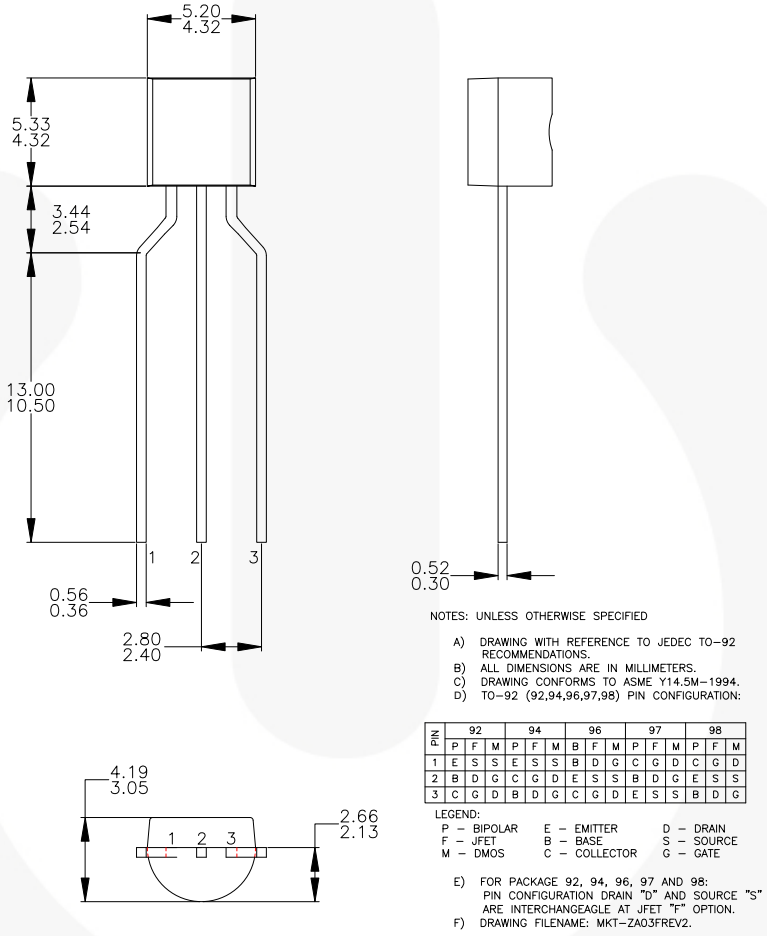


Figure 4. Power Derating

Physical Dimensions

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03FREV2.

Figure 5. 3-LEAD, TO-92, MOLDED 0.200 IN LINE SPACING LD FORM (J61Z OPTION) (ACTIVE)

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