FAIRCHILD SEMICONDUCTOR®

LIMITED DATASHEET

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September 2012

FPF3040
IntelliMAX™ 20 V-Rated Dual Input Single Output Power-Source-Selector Switch

Features

- Dual-Input, Single-Output Load Switch
- Input Supply Operating Range:
  - 4~10.5 V at V_{IN}
  - 4~6.5 V at V_{BUS}
- Typical R_{ON}:
  - 95 mΩ at V_{IN}=5 V
  - 70 mΩ at V_{BUS}=5 V
- Bi-Directional Switch for V_{IN} and V_{BUS}
- Slew Rate Controlled:
  - 50 µs at V_{IN} for < 4.7 µF C_{OUT}
  - 90 µs at V_{BUS} for < 4.7 µF C_{OUT}
- Maximum I_{SW}: 2 A Per Channel
- Break-Before-Make Transition
- Under-Voltage Lockout (UVLO)
- Over-Voltage Lockout (OVLO)
- Thermal Shutdown
- Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements
- ESD Protected:
  - Human Body Model: >3 kV
  - Charged Device Model: >1.5 kV
  - IEC 61000-4-2 Air Discharge: >15 kV
  - IEC61000-4-2 Contact Discharge: >8 kV

Applications

- Input Power Selection Block Supporting USB and Wireless Charging
- Smartphone / Tablet PC

Description

The FPF3040 is a 20 V-rated Dual-Input Single-Output (DISO) load switch consisting of two channels of slew-rate-controlled, low-on-resistance, N-channel MOSFET switches with protection features. The slew-rate-controlled turn-on characteristic prevents inrush current and the resulting excessive voltage droop on the input power rails. The input voltage range operates from 4 V to 6.5 V at V_{BUS} and from 4 V to 10.5 V at V_{IN} to align with the needs of low-voltage portable device power rails.

V_{IN} and V_{BUS} have the over-voltage protection functionality of typical 12 V and 7.5 V, respectively, to avoid unwanted damage to system.

V_{IN} and V_{BUS} bi-directional switching allows reverse current from V_{OUT} to V_{IN} or V_{BUS} for On-The-Go, (OTG) Mode. The switching is controlled by logic input EN and V_{IN_SEL} is capable of interfacing directly with low-voltage control signal General-Purpose Input / Output (GPIO).

FPF3040 is available in 1.8 mm x 2.0 mm Wafer-Level Chip-Scale Package (WLCSP), 16-bump, 0.4 mm pitch.

Ordering Information

Part Number	Top Mark	Channel	Typical R_{ON} per Channel at $5V_{IN}$	Rise Time (t_R)	Package
FPF3040UCX	QY	DISO	95 mΩ for V_{IN}	50 µs for V_{IN}	1.8 mm x 2.0 mm Wafer-Level Chip-Scale Package (WLCSP), 16-Bump, 0.4 mm Pitch
			70 mΩ for V_{BUS}	90 µs for V_{BUS}	

Application Diagram

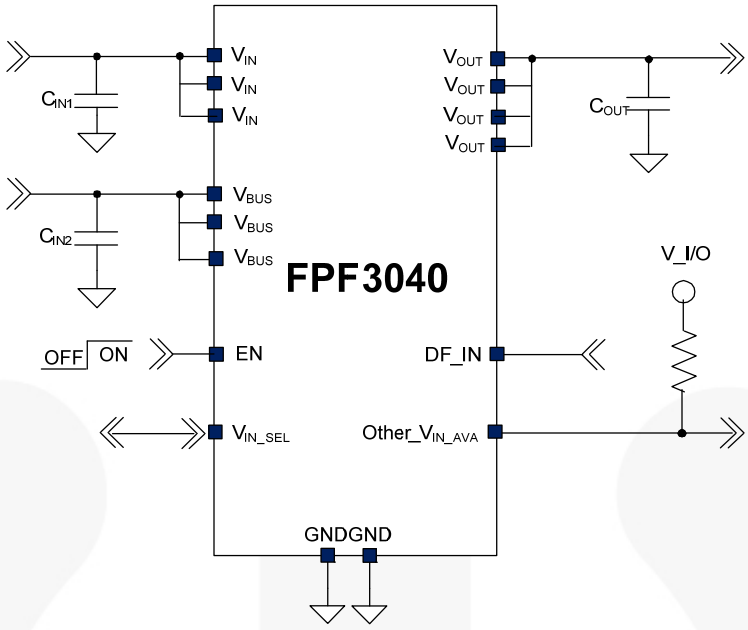


Figure 1. Typical Application

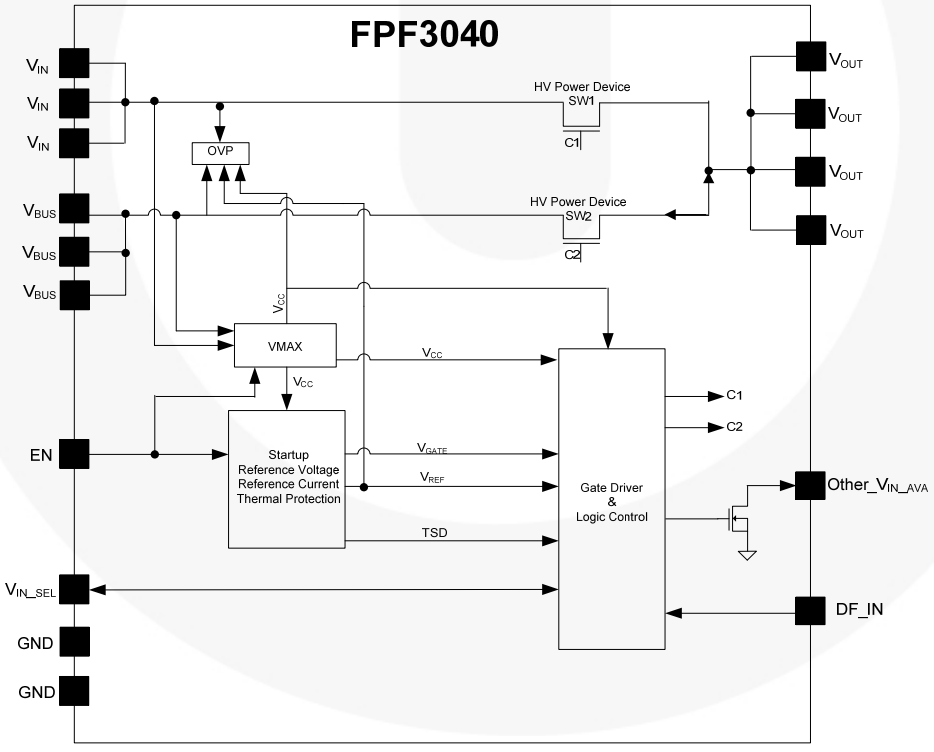
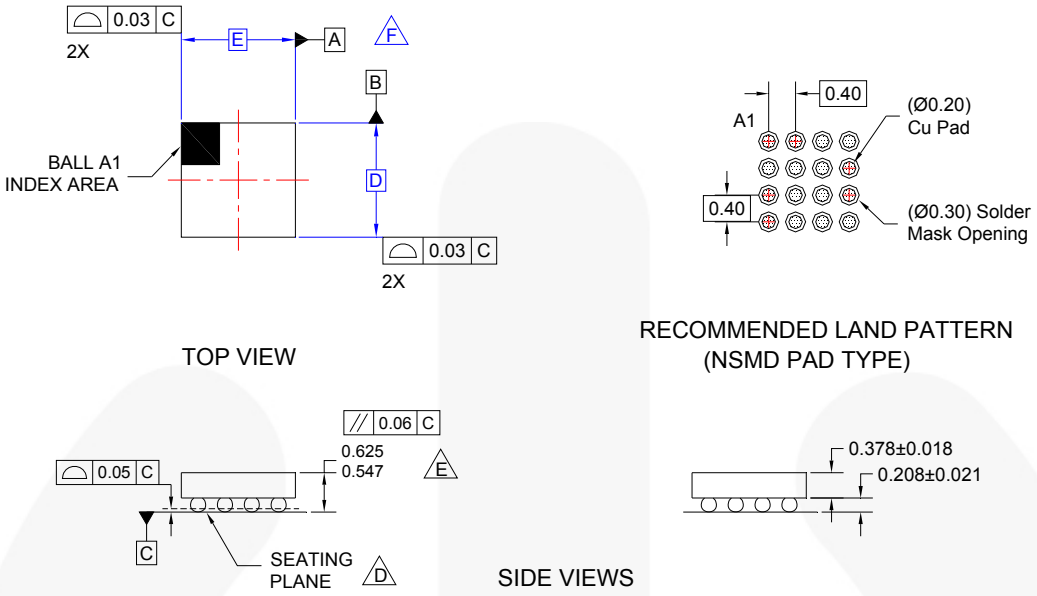


Figure 2. Functional Block Diagram

Package Description



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC016AArev2.

Figure 31.1.8 mm x 2.0 mm Wafer-Level Chip-Scale Package (WLCSP), 16-Bump, 0.4 mm Pitch

Product	D	E	X	Y
FPF3040UCX	1.96 mm ±0.03 mm	1.76 mm ±0.03 mm	0.28 mm	0.38 mm

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Rev. I62