

FSA641 — 2:1 MIPI Switch, Featuring 2-Data and 1-Data Lane Configuration

Features

| | |
|-------------------------|--|
| Switch Type | 2:1 |
| Signal Types | MIPI, DPHY |
| V _{CC} | 2.65 to 4.3 V |
| Input Signals | 0 to V _{CC} |
| R _{ON} | 7 Ω Typical HS MIPI 10 Ω Typical LS MIPI |
| ΔR _{ON} | 0.75 Ω Typical HS & LS MIPI |
| I _{CC} | 1 μA Maximum |
| O _{IRR} | -50 dB Typical |
| X _{TALK} | -40 dB Typical |
| Bandwidth | 1 GHz Typical |
| Channel-to-Channel Skew | 15 ps Typical |
| C _{ON} | 8 pF Typical |
| Package | 20-Lead UMLP 3.0x3.0x 0.55 mm, 0.4 mm Pitch |
| Ordering Information | FSA641UMX |

Applications

- Cellular Phones, Smartphones
- Displays

Typical Application

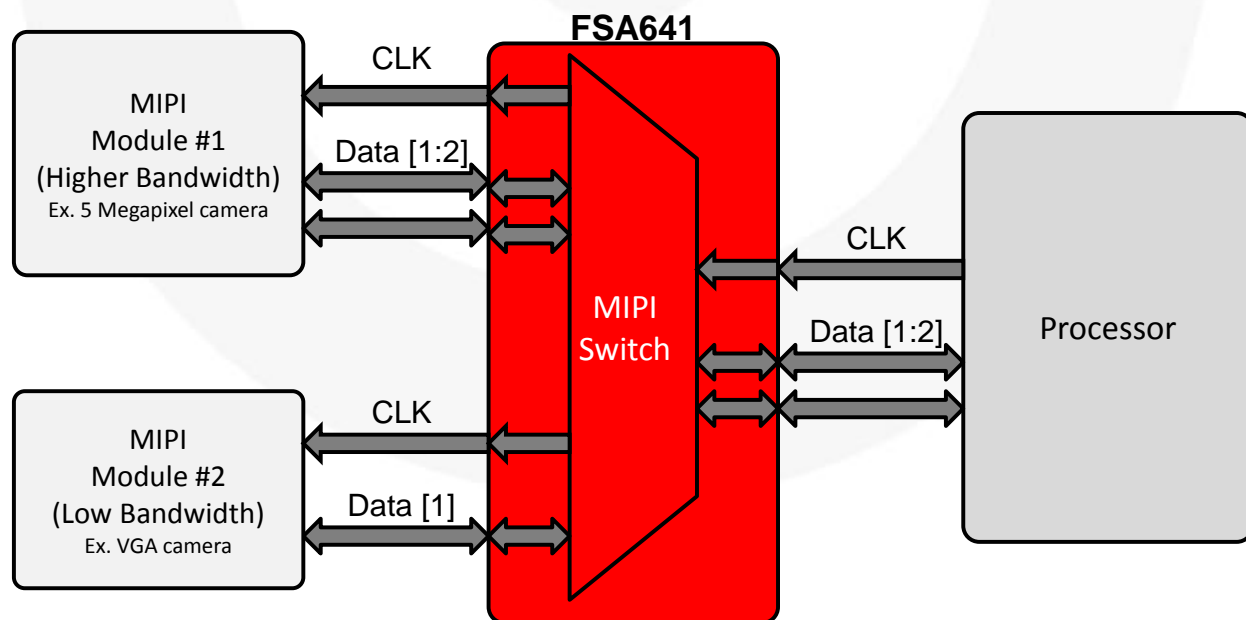


Figure 1. Mobile Phone Example

Description

The FSA641 is a 2:1 MIPI switch made for 2-data lane and 1-data lane modules. This part is configured as a single-pole, double-throw switch (SPDT) and is optimized for switching between two high-speed or low-power MIPI sources. The FSA641 has specially been designed for the MIPI specification and allows connection to either a CSI or DSI module. The FSA641 features an extremely low on capacitance (C_{ON}) of 8 pF. The wide bandwidth (1 GHz) results in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk minimizes interference.

Related Resources

- For samples and questions, please contact: Analog.Switch@fairchildsemi.com.
- FSA641 Demonstration Board

Pin Configuration

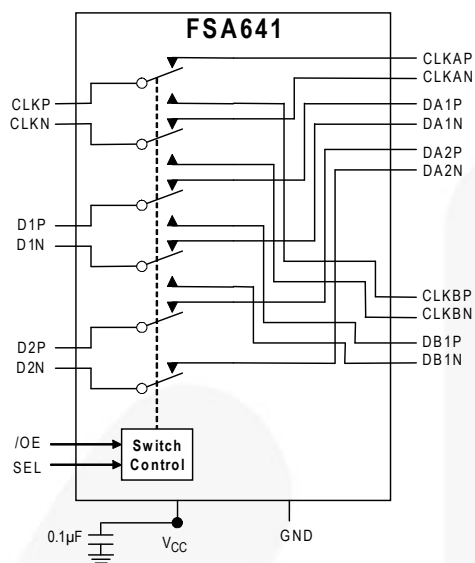


Figure 2. Functional Block Diagram

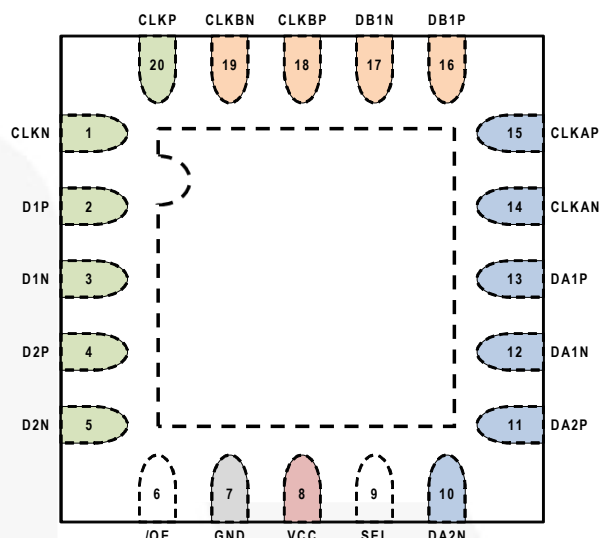


Figure 3. Pin Assignments (Top Through View)

Pin Descriptions

| Pin # | Pin Name | Type | Description |
|--------|----------|--------|--|
| 20 | CLKP | I/O | Common positive clock path |
| 1 | CLKN | I/O | Common negative clock path |
| 2 | D1P | I/O | Common positive data 1 path |
| 3 | D1N | I/O | Common negative data 1 path |
| 4 | D2P | I/O | Common positive data 2 path |
| 5 | D2N | I/O | Common negative data 2 path |
| 15 | CLKAP | I/O | A-port positive clock path |
| 14 | CLKAN | I/O | A-port negative clock path |
| 13 | DA1P | I/O | A-port positive data 1 path |
| 12 | DA1N | I/O | A-port negative data 1 path |
| 11 | DA2P | I/O | A-port positive data 2 path |
| 10 | DA2N | I/O | A-port negative data 2 path |
| 18 | CLKBP | I/O | B-port positive clock path |
| 19 | CLKBN | I/O | B-port negative clock path |
| 16 | DB1P | I/O | B-port positive data 1 path |
| 17 | DB1N | I/O | B-port negative data 1 path |
| 6 | /OE | Input | Output Enable (Active Low) |
| 7 | GND | Ground | Ground |
| 8 | VCC | Supply | Power; 0.1 µF decoupling capacitor to ground recommended |
| 9 | SEL | Input | A-port or B-port Select pin |
| Paddle | n/a | NC | Not Connected |

Truth Table

| SEL | /OE | Function |
|------------|------|----------------------------|
| Don't Care | HIGH | Disconnect |
| LOW | LOW | D1, D2, CLK=DA1, DA2, CLKA |
| HIGH | LOW | D1, CLK=DB1, CLKB; D2 OPEN |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------|--|--------------|----------------|------|
| V_{CC} | Supply Voltage | -0.50 | +5.25 | V |
| V_{CNTRL} | DC Input Voltage (SEL, /OE) ⁽¹⁾ | -0.5 | V_{CC} | V |
| V_{SW} | DC Switch I/O Voltage ⁽¹⁾ | -0.5 | $V_{CC} + 0.3$ | V |
| I_{IK} | DC Input Diode Current | -50 | | mA |
| I_{OUT} | DC Output Current | | 50 | mA |
| T_{STG} | Storage Temperature | -65 | +150 | °C |
| ESD | Human Body Model, JEDEC: JESD22-A114 | All Pins | 6.5 | kV |
| | | I/O to GND | 8.0 | |
| | | Power to GND | 16.0 | |
| | Charged Device Model, JEDEC: JESD22-C101 | | 2.0 | |

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------|---|------|----------|------|
| V_{CC} | Supply Voltage | 2.65 | 4.30 | V |
| V_{CNTRL} | Control Input Voltage (SEL, /OE) ⁽²⁾ | 0 | V_{CC} | V |
| V_{SW} | Switch I/O Voltage | -0.5 | V_{CC} | V |
| T_A | Operating Temperature | -40 | +85 | °C |

Note:

2. The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are $T_A=25^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | V_{CC} (V) | $T_A=-40$ to $+85^{\circ}\text{C}$ | | | Units |
|-----------|---|---|----------------|------------------------------------|------|------|---------------|
| | | | | Min. | Typ. | Max. | |
| V_{IK} | Clamp Diode Voltage | $I_{IN}=-18$ mA | 2.775 | | | -1.2 | V |
| I_{IN} | Control Input Leakage | $V_{SW}=0$ to 4.3 V | 4.3 | -1 | | 1 | μA |
| V_{IH} | Input Voltage High | $V_{IN}=0$ to V_{CC} | 2.650 to 2.775 | 1.3 | | | V |
| | | | 4.3 | 1.7 | | | |
| V_{IL} | Input Voltage Low | $V_{IN}=0$ to V_{CC} | 2.650 to 2.775 | | | 0.5 | V |
| I_{OZ} | Off-State Leakage | A, B=0+0.3 V to $V_{CC}-0.3$ | 4.3 | -2 | | 2 | μA |
| I_{CC} | Quiescent Supply Current | $V_{CNTRL}=0$ or V_{CC} , $I_{OUT}=0$ | 4.3 | | | 1.0 | μA |
| I_{CCT} | Increase in I_{CC} Current Per Control Voltage and V_{CC} | $V_{CNTRL}=1.8$ V | 2.775 | | | 1.5 | μA |

DC Electrical Characteristics, Low-Speed Mode

All typical values are $T_A=25^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | V_{CC} (V) | $T_A=-40$ to $+85^{\circ}\text{C}$ | | | Units |
|-----------------|--|--|--------------|------------------------------------|------|------|----------|
| | | | | Min. | Typ. | Max. | |
| R_{ON} | LS Switch On Resistance ⁽³⁾ | $V_{SW}=1.2$ V, $I_{ON}=-10$ mA, Figure 4 | 2.65 | | 10 | 14 | Ω |
| ΔR_{ON} | LS Delta R_{ON} ⁽⁴⁾ | $V_{SW}=1.2$ V, $I_{ON}=-10$ mA (Intra-pair) | 2.65 | | 0.75 | | Ω |

Notes:

- Measured by the voltage drop between A/B and CLK/Dn pins at the indicated current through the switch.
- Guaranteed by characterization.

DC Electrical Characteristics, High-Speed Mode

All typical values are $T_A=25^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | V_{CC} (V) | $T_A=-40$ to $+85^{\circ}\text{C}$ | | | Units |
|-----------------|--|--|--------------|------------------------------------|------|------|----------|
| | | | | Min. | Typ. | Max. | |
| R_{ON} | HS Switch On Resistance ⁽⁵⁾ | $V_{SW}=0.4$ V, $I_{ON}=-10$ mA, Figure 4 | 2.65 | | 7.0 | 9.5 | Ω |
| ΔR_{ON} | HS Delta R_{ON} ⁽⁶⁾ | $V_{SW}=0.4$ V, $I_{ON}=-10$ mA (Intra-pair) | 2.65 | | 0.75 | | Ω |

Notes:

- Measured by the voltage drop between A, B, and Dn pins at the indicated current through the switch.
- Guaranteed by characterization.

AC Electrical Characteristics

All values are at $R_L=50\ \Omega$ and $R_S=50\ \Omega$ and all typical values are $V_{CC}=2.775\text{ V}$ at $T_A=25^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | $V_{CC}\text{ (V)}$ | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | | | Units |
|-----------|---|---|---------------------|--|------|------|-------|
| | | | | Min. | Typ. | Max. | |
| O_{IRR} | Off Isolation ⁽⁷⁾ | $f=100\text{ MHz}$, $R_T=50\ \Omega$ Figure 14 | 2.775 | | -50 | | dB |
| Xtalk | Non-Adjacent Channel Crosstalk ⁽⁷⁾ | $f=100\text{ MHz}$, $R_T=50\ \Omega$ Figure 15 | 2.775 | | -40 | | dB |
| BW | -3db Bandwidth ⁽⁷⁾ | $C_L=0\text{ pF}$, $R_T=50\ \Omega$ Figure 13 | 2.775 | | 1.0 | | GHz |
| t_{ON} | Turn-On Time SEL, /OE to Output | $C_L=5\text{ pF}$, $V_{SW}=1.2\text{ V}$ Figure 6, Figure 7 | 2.650 to 2.775 | | 20 | 37 | ns |
| t_{OFF} | Turn-Off Time SEL, /OE to Output | $C_L=5\text{ pF}$, $V_{SW}=1.2\text{ V}$ Figure 6, Figure 7 | 2.650 to 2.775 | | 15 | 27 | ns |
| t_{PD} | Propagation Delay ⁽⁷⁾ | $C_L=5\text{ pF}$ Figure 6, Figure 8 | 2.775 | | 0.25 | | ns |
| t_{BBM} | Break-Before-Make Time | $C_L=5\text{ pF}$, $V_{SW1}=V_{SW2}=1.2\text{ V}$ Figure 12 | 2.650 to 2.775 | 7 | 9 | 12 | ns |

Note:

7. Guaranteed by characterization.

AC Electrical Characteristics, High-Speed

All typical values are $V_{CC}=2.775\text{ V}$ at $T_A=25^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | | | Units |
|-----------------------------|--|---|--|------|------|-------|
| | | | Min. | Typ. | Max. | |
| $t_{SK(\text{Part_Part})}$ | Channel-to-Channel Skew Across Multiple Parts ^(8,9) | TDR-Based Method ($V_{SW}=0.2V_{PP}$, $C_L = C_{ON}$) | | 40 | 80 | ps |
| $t_{SK(\text{Chl_Chl})}$ | Channel-to-Channel Skew Within a Single Part ⁽⁸⁾ | TDR-Based Method ($V_{SW}=0.2V_{PP}$, $C_L = C_{ON}$) | | 15 | 30 | ps |
| $t_{SK(\text{Pulse})}$ | Skew of Opposite Transitions in the Same Differential Channel ⁽⁸⁾ | TDR-Based Method ($V_{SW}=0.2V_{PP}$, $C_L = C_{ON}$) | | 10 | 20 | ps |

Notes:

8. Guaranteed by characterization.

9. Assumes the same V_{CC} and temperature for all devices.

Capacitance

| Symbol | Parameter | Conditions | $T_A=-40^\circ\text{C to }+85^\circ\text{C}$ | | | Units |
|-----------|---|--|--|------|------|-------|
| | | | Min. | Typ. | Max. | |
| C_{IN} | Control Pin Input Capacitance ⁽¹⁰⁾ | $V_{CC}=0\text{ V}$ | | 1.5 | | pF |
| C_{ON} | Dn/CLK- On Capacitance ⁽¹⁰⁾ | $V_{CC}=2.775\text{ V}$, /OE=0V, $f=1\text{ MHz}$ Figure 11 | | 8.0 | | |
| C_{OFF} | Dn/CLK Off Capacitance ⁽⁹⁾ | $V_{CC}=2.775\text{ V}$, /OE=2.775 V, $f=1\text{ MHz}$ Figure 10 | | 2.5 | | |

Note:

10. Guaranteed by characterization.

Test Diagrams

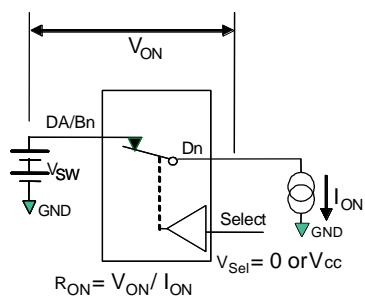
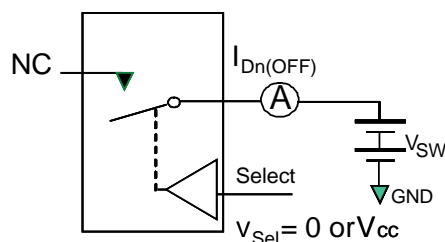


Figure 4. On Resistance



**Each switch port is tested separately

Figure 5. Off Leakage

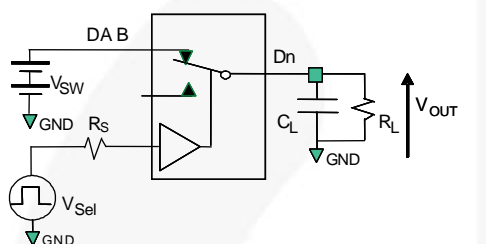


Figure 6. AC Test Circuit Load

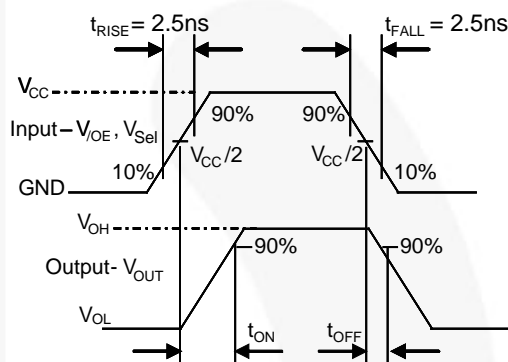


Figure 7. Turn-On / Turn-Off Waveforms

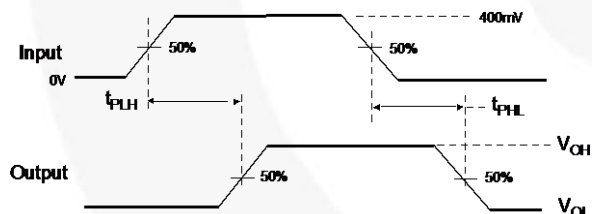


Figure 8. Propagation Delay ($t_{RTF} = 500 \text{ ps}$)

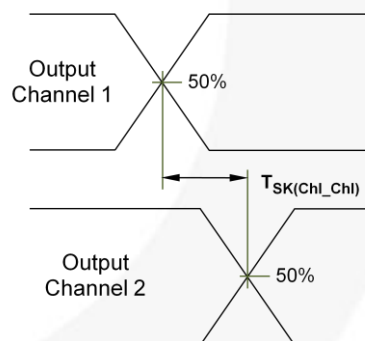


Figure 9. Channel-to-Channel Skew

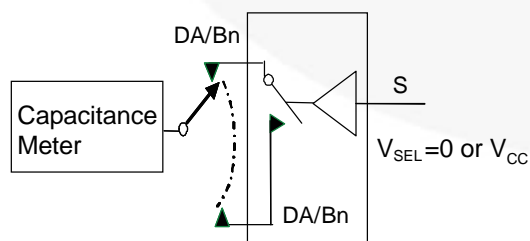


Figure 10. Channel Off Capacitance

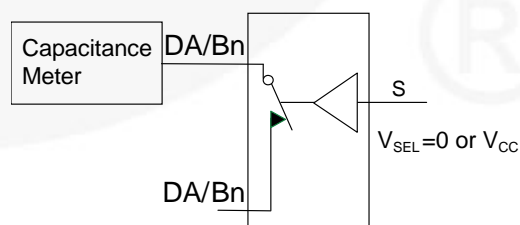


Figure 11. Channel On Capacitance

Test Diagrams (Continued)

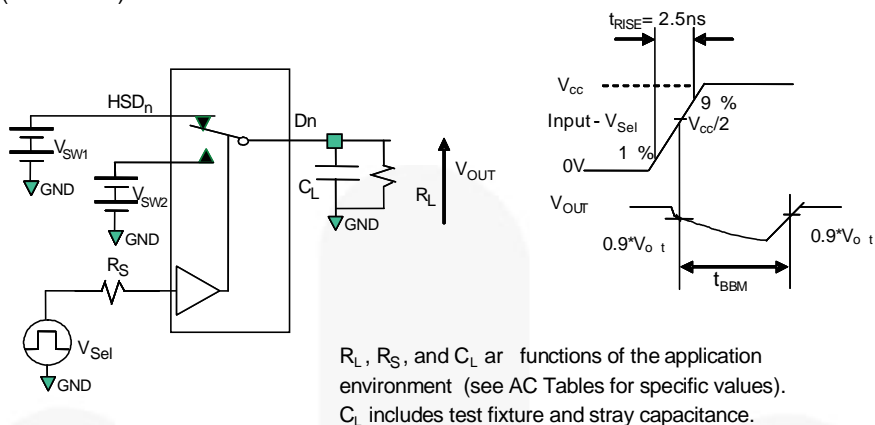


Figure 12. Break-Before-Make Interval Timing

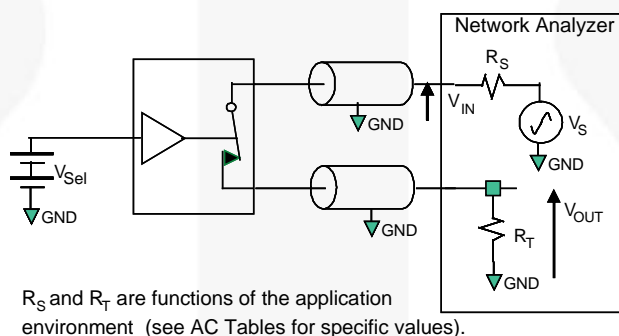
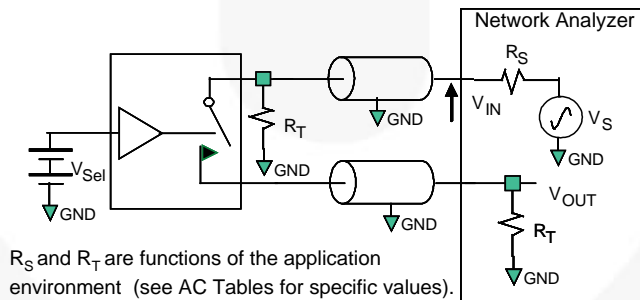
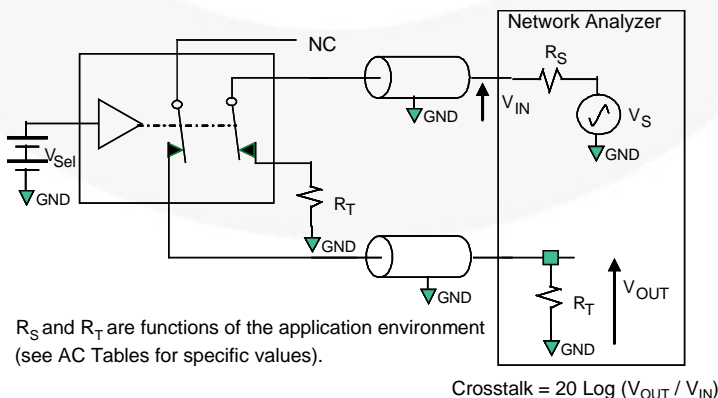


Figure 13. Bandwidth



$$\text{Off isolation} = 20 \log (V_{OUT} / V_{IN})$$

Figure 14. Channel Off Isolation



$$\text{Crosstalk} = 20 \log (V_{OUT} / V_{IN})$$

Figure 15. Non-Adjacent Channel-to-Channel Crosstalk

Physical Dimensions

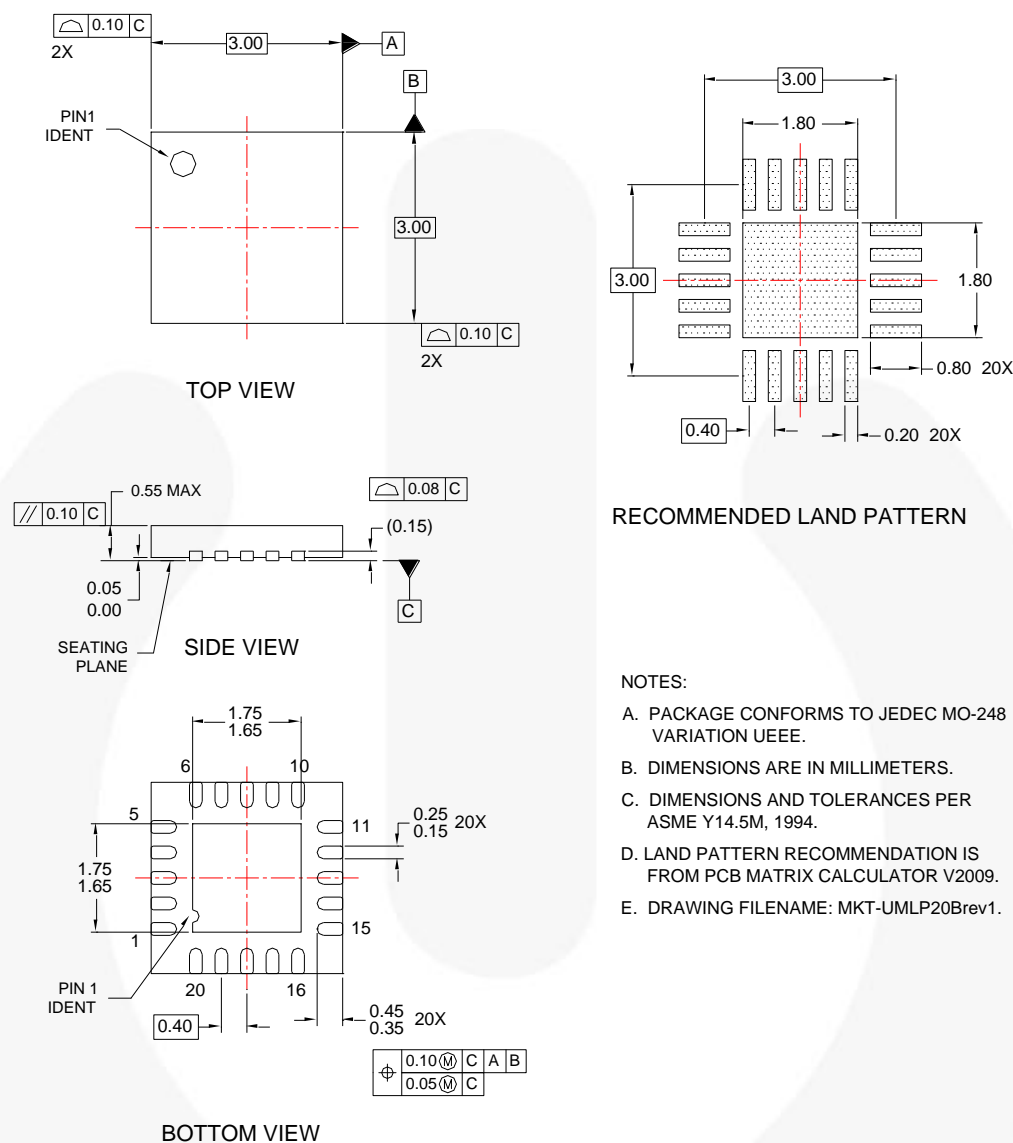


Figure 16. 20-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 3.0 x 3.0 mm

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http://www.fairchildsemi.com/packaging/3.0x3.0_UMLP_Pack_TNR_Spec.pdf.

Ordering Information

| Part Number | Top Mark | Operating Temperature Range | Package |
|-------------|----------|-----------------------------|---|
| FSA641UMX | F641 | -40 to +85°C | 20-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 3.0 x 3.0 mm |

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