HDR-60 Video Camera Development Kit

Real-time HD Video Camera with Fully Integrated HDR Image Signal Processing

The HDR-60 Video Camera Development Kit is a production-ready High Definition (HD) video camera development system based on the LatticeECP3™ FPGA family. Pre-loaded with a plug-and-play evaluation Image Signal Processing (ISP) pipeline based on Intellectual Property (IP) cores from Lattice partner Helion GmbH, the kit works right out of the box. The IP is capable of delivering 1080p performance at 60 frames per second with 2D noise reduction and High Dynamic Range (HDR).

Designed to fit into commercially available camera housings and capable of supporting two sensors simultaneously, the kit enables rapid evaluation and prototyping of high-definition HDR video cameras for security and surveillance, traffic control, video conferencing and automotive applications. Schematics and layout files are available for download to purchasers of the kit.

The HDR-60 Video Camera Development Kit has been designed using a LatticeECP3-70 FPGA; however, the ISP IP pipeline needed to implement a complete 1080p60 HDR camera requires only a 33K LUT LatticeECP3-35 device. The available space offers designers plenty of room for experimentation and adding custom IP.

The kit offers camera manufacturers several unique benefits, including a fully integrated HDR image signal processing pipeline from sensor to HDMI/DVI display. Equipped with an Aptina 720p HDR sensor, the kit also offers the industry's fastest auto-exposure, greater than 120dB system dynamic range, a highly-efficient auto white balance algorithm and 2D noise reduction – all in streaming mode through the FPGA without the need for an external frame buffer, enabling extremely low latency and further reducing system cost. On-board DDR2 memory also enables applications such as 3D noise reduction, image stitching from multiple sensors, image rotation and de-warping.

Key Features and Benefits

- FPGA-based Image Signal Processing
- Fully Production-ready HDR Camera Design
- IP is Capable of 1080p at 60fps
- IP Supports up to 16 Megapixel Sensors
- Full 60fps in Streaming Mode Needs No External Frame Buffer
- Fast Auto Exposure Quickly Adjusts to Changing Light
- Greater than 120dB High Dynamic Range (HDR) Performance
- Extremely Low Latency
- Comprehensive Image Processing IP Library
- On-board Broadcom® Broadreach™ PHY Enables Ethernet over Coaxial Cable for Distances up to 700m
- On-board FTDI Device provides Easy Programming via Standard USB Cable

Ordering Information

Product	Description	Ordering Part Number
HDR-60 Video Camera Develoment Kit	• HDR-60 Base Board with LatticeECP3 FPGA, pre-loaded with Image Signal Processing (ISP) Demo • NanoVesta Head Board with Aptina A-1000 720p HDR Sensor and Sunex lens • Two USB cables • HDMI cable with HDMI-to-DVI adapter • 12V AC adapter power supply • QuickSTART Guide	LFE3-70EA-HDR60-DKN

HDR-60 Base Board with NanoVesta Head Board – Top View

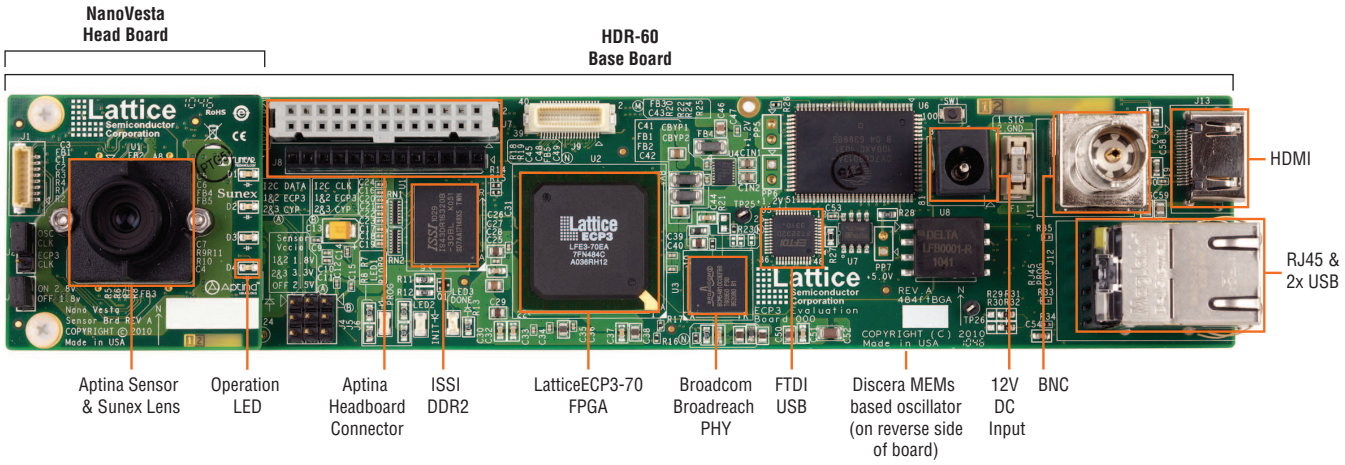


Image Signal Processing Demo

The pre-loaded Image Signal Processing pipeline demo is plug-and-play, and works directly with a compatible HDMI/DVI monitor. Simple instructions are provided to demonstrate Fast Auto Exposure, Auto White Balance and High Dynamic Range for evaluation of the pipeline's capabilities.

HDR ISP Pipeline Reference Design

The pre-loaded demo bitstream contains a fully functional HDR ISP Pipeline with the following IP blocks:

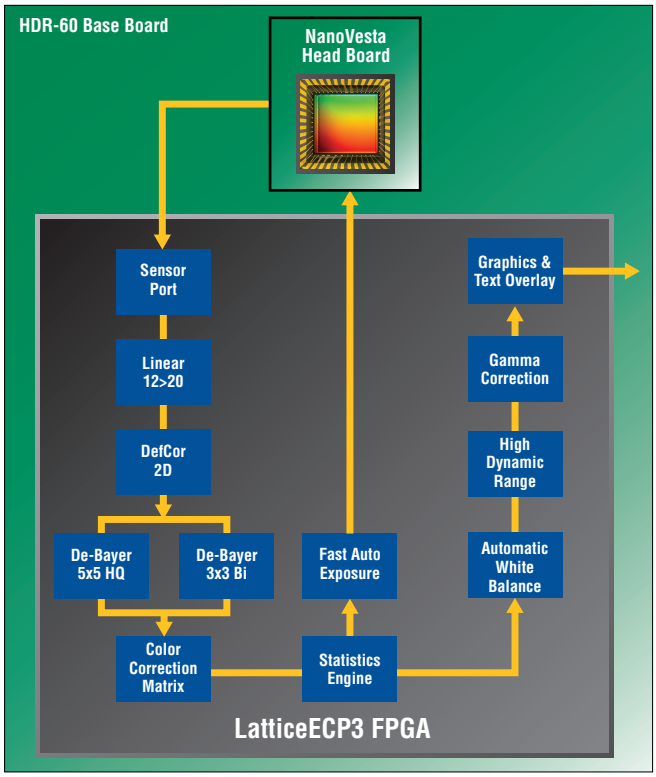
- Sensor Port
- Linearization Block
- Defective Pixel Correction/2D Noise Reduction
- High-Quality 5 x 5 De-Bayer Block
- Color Correction Matrix
- Statistics Engine
- Fast Auto Exposure Block
- Auto White Balance Block
- Helion BLENDFEST™ HDR Block
- Gamma Correction
- Graphics and Text Overlay

Comprehensive IP Library

The kit is supported by a comprehensive intellectual property (IP) library. Containing more than 90 individual pieces of IP, the library is available for licensing either entirely or in parts. Developed by Lattice partner Helion GmbH, the library provides complete sensor to display ISP support including:

- Sensor and Display Interfaces
- Color Pipeline
- Image Enhancement
- Peripherals and Overlay

HDR Image Signal Processing Pipeline Reference Design Block Diagram



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