# MachXO Family

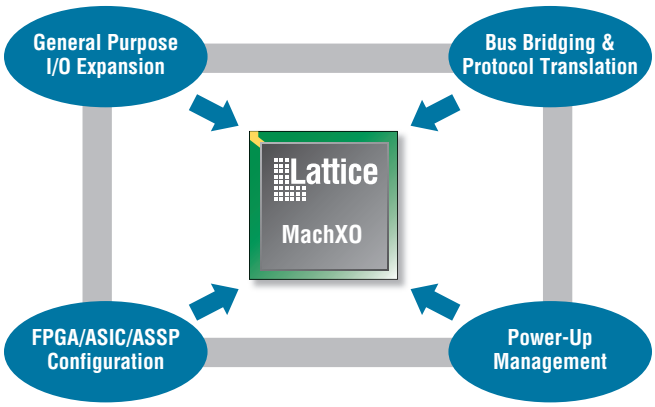
## *Optimized for Low Density Applications*

The MachXO™ family of non-volatile infinitely reconfigurable Programmable Logic Devices (PLDs) is designed for applications traditionally implemented using CPLDs or low-density FPGAs. Combining an optimized look-up table (LUT) architecture with low-cost embedded Flash process technology, the instant-on, easy-to-use MachXO devices are the most versatile, non-volatile PLDs for low-density applications.

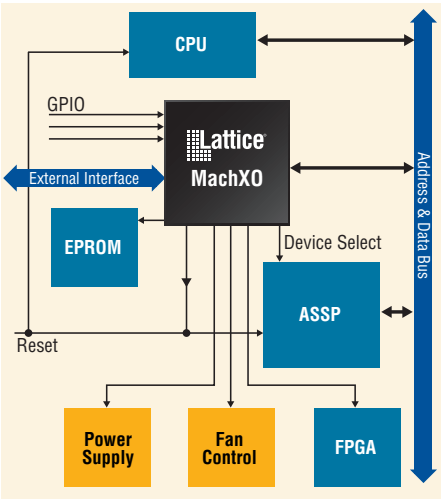
The MachXO PLD family offers the benefits of increased system integration by providing embedded memory, built-in PLLs, flexible multi-voltage high-performance LVDS I/Os, remote field upgrade (TransFR™ technology) and low-power sleep mode, all in a single device.

Designed for a broad range of low-density applications that include general purpose I/O expansion, control, bus bridging and power-up management functions, the MachXO PLD family is used in a variety of end markets such as consumer, automotive, communications, computing, industrial and medical.

### *Broad Range of Applications*




### *MachXO Application Example*





### *Key Features and Benefits*

- **Non-Volatile, Infinitely Reconfigurable**
  - Instant-on, powers up in less than 1mS
  - Single-chip, no external configuration memory
  - Excellent design security, no bitstream to intercept
- **Performance to 3.5ns Pin-to-Pin**
- **TransFR Technology Allows Simple Field Upgrades**
- **Flexible LUT Architecture**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
- **Embedded and Distributed Memory**
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Includes dedicated FIFO control logic
  - Up to 7.7 Kbits distributed RAM
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI*
    - LVDS*, Bus-LVDS*, LVPECL*, RSDS*
- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide and phase shifting
- **Sleep Mode Reduces Standby Power to <100µA**
- **System-Level Support**
  - IEEE Standard 1149.1 Boundary Scan
  - On-board 20MHz oscillator for configuration and user logic
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
- **Broad Device Offering**
  - Commercial: 0 to 85°C ($T_{JCOM}$)
  - Industrial: -40 to 100°C ($T_{JIND}$)
  - AEC-Q100 qualified: -40 to 125°C ($T_{JAUTO}$)

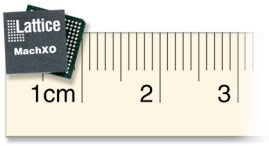
* MachXO1200 and 2280 devices only.

# MachXO Architecture

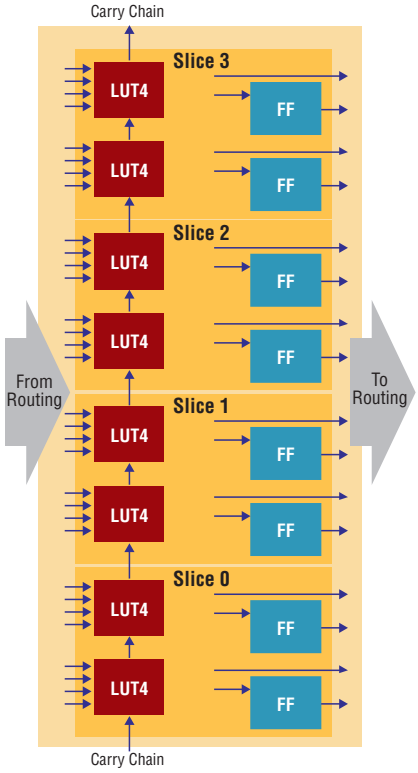
## *Architecture Overview*

MachXO PLDs are designed to offer a low-cost, flexible alternative for applications traditionally served by CPLDs or low-density FPGAs. Built with an extremely efficient architecture, MachXO PLDs deliver excellent pin-to-pin performance, support for high-speed I/Os, embedded block RAM, and sysCLOCK PLLs.

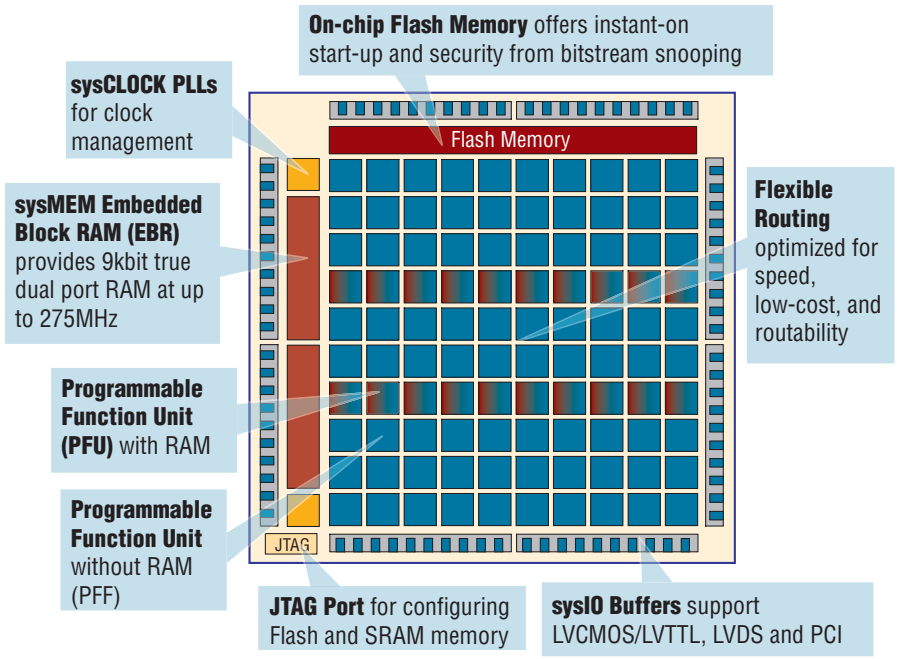
*Available in space saving, RoHS compliant package options, MachXO PLDs can be used in a broad range of space constrained applications.*




### PFU BLOCK DIAGRAM



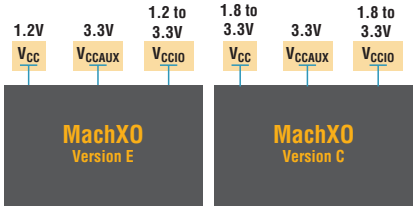

## *MachXO Block Diagram*




### sysMEM CONFIGURATION OPTIONS

| Single Port | Dual Port | Pseudo-Dual Port | FIFO |
|---|---|---|---|
| 8192 x 1 | 8192 x 1 | 8192 x 1 | 8192 x 1 |
| 4096 x 2 | 4096 x 2 | 4096 x 2 | 4096 x 2 |
| 2048 x 4 | 2048 x 4 | 2048 x 4 | 2048 x 4 |
| 1024 x 9 | 1024 x 9 | 1024 x 9 | 1024 x 9 |
| 512 x 18 | 512 x 18 | 512 x 18 | 512 x 18 |
| 256 x 36 | – | 256 x 36 | 256 x 36 |

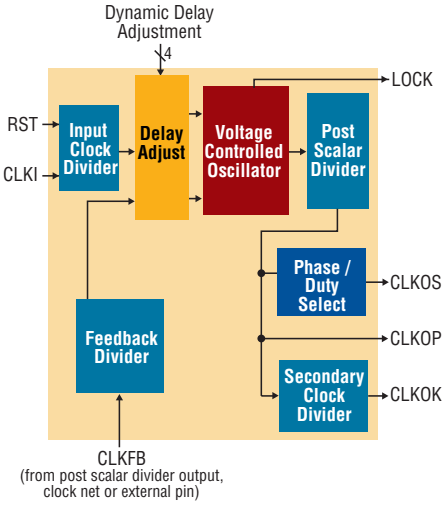
### MachXO VOLTAGE OPTIONS




### sysIO BUFFER SUPPORTS HIGH-BANDWIDTH I/O STANDARDS

- LVCMOS / LVTTL
  - – Hotsocketing capable
  - – Programmable slew rate
  - – Programmable drive strength
  - – Programmable pull-up, pull-down, bus friendly
  - – Programmable open drain
  - – Programmable Schmitt element
- PCI, LVDS, LVPECL, Bus-LVDS, RSDS

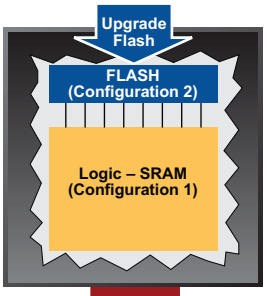
### sysCLOCK PLL BLOCK DIAGRAM



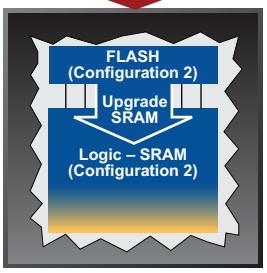
## *Easy Field Updates*

MachXO PLDs include Lattice's exclusive Transparent Field Reconfiguration (TransFR) technology. TransFR technology allows logic to be updated in the field without interrupting system operation.

**Step 1**
Program Flash in background while logic functions

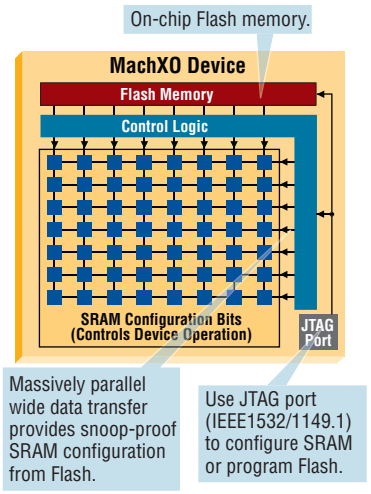



**Step 2**
Precisely control I/O and initiate Flash to SRAM transfer through JTAG. Alternatively, toggle sleep pin to load new configuration without cycling the power.




## *MachXO Configuration*

MachXO PLDs include both Flash and SRAM technology to provide "instant-on" capabilities in a single low-cost device. At power-up, configuration data is transferred from Flash to SRAM cells in less than 1mS. Both SRAM and Flash memory can be programmed from a JTAG port. This combination of SRAM and Flash enables easy field updates via Lattice's unique TransFR technology. MachXO PLDs have a security scheme that prevents readback and, by using Flash internally, Lattice eliminates bit stream snooping.

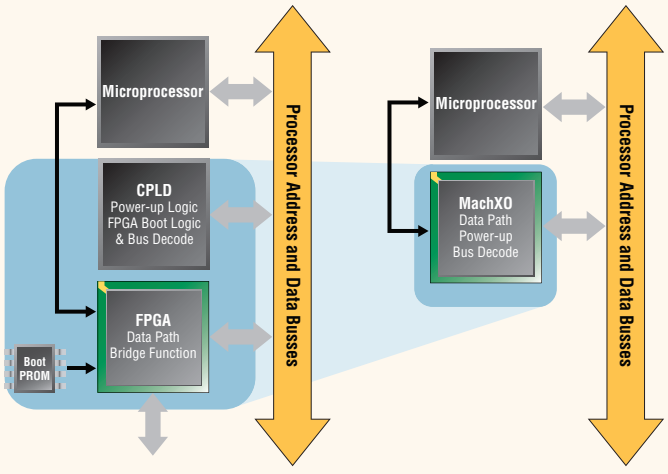



### MachXO SLEEP MODE REDUCES POWER BY A FACTOR OF 100X!

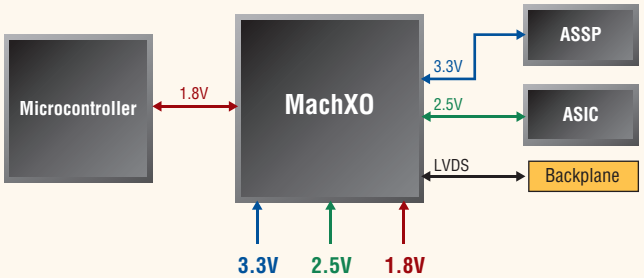
| Characteristic | Normal Mode | Off | Sleep Mode |
|---|---|---|---|
| **SLEEPN Pin** | High | X | Low |
| **Static Icc** | Typically <10mA | 0 | Typically <100µA |
| **Power Supplies** | Normal Range | 0 | Normal Range |
| **Logic Operation** | User Defined | Non Operational | Non Operational |
| **I/O Operation** | User Defined | Tri-State (<1mA leakage) | Tri-State (<10µA leakage) |

# MachXO Application Examples

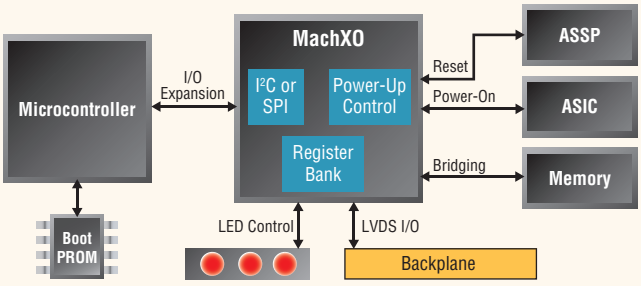
### LOW-COST SYSTEM INTEGRATION



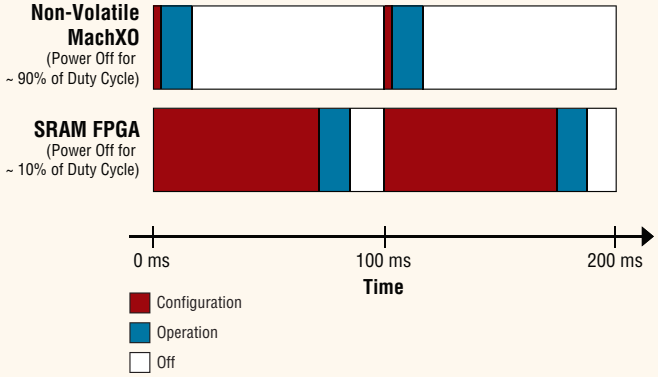

### FLEXIBLE MULTI-VOLTAGE LEVEL SHIFTING




### POWER UP AND CONTROL




### LOW POWER CYCLING



## Free ispLEVER Starter Development Tools

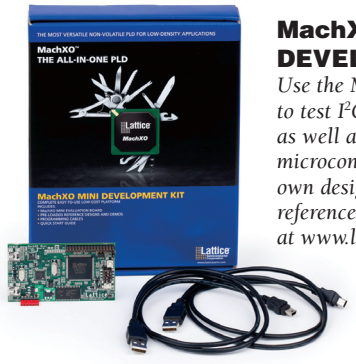
Lattice's ispLEVER Starter development tools offer a comprehensive design environment for the MachXO architecture and other select PLD families. ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floor planning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Aldec® and Synplicity® are included with ispLEVER.

## Evaluation and Development Boards

Lattice offers a number of evaluation and development boards that provide a complete and easy-to-use platform to evaluate the performance of the MachXO, or aid in the development of custom designs.

## Reference Design Portfolio

Lattice offers an expanding portfolio of IP cores and reference designs targeted for low-density applications. Optimized for the MachXO architecture these include popular protocol and connectivity standards such as I2C, SPI, UART and PCI. The reference designs, source codes and documentation can be downloaded for free from the Lattice website. For more information, go to www.latticesemi.com/ip.




### MachXO MINI DEVELOPMENT KIT

*Use the MachXO Mini Development Kit to test I²C, SPI, UART, SRAM interfaces as well as the 8-bit LatticeMico8™ microcontroller within minutes. Build your own design in less than an hour using free reference designs from Lattice. Learn more at www.latticesemi.com/machxo-mini.*

### MachXO CONTROL DEVELOPMENT KIT

*Use the MachXO Control Development Kit to test board diagnostic functions including fan speed control based on temperature monitoring, complete power supply monitoring and reset distribution in conjunction with the Power Manager II POWR1014A and 8-bit LatticeMico8 microcontroller. Test these functions within minutes and build your own designs in less than an hour using the free reference designs from Lattice. Learn more at www.latticesemi.com/machxo-control-kit.*

## Device Selection Guide

| Parameter | LCMXO256 | LCMXO640 | LCMXO1200 | LCMXO2280 |
|---|---|---|---|---|
| **LUTs** | 256 | 640 | 1200 | 2280 |
| **Distributed RAM (Kbits)** | 2 | 6.1 | 6.4 | 7.7 |
| **Embedded Block RAM – EBR (Kbits)** | – | – | 9.2 | 27.6 |
| **Number of EBR Blocks** | – | – | 1 | 3 |
| **$V_{CC}$ Voltage (V) Options** | 1.2V or 1.8/2.5/3.3V | 1.2V or 1.8/2.5/3.3V | 1.2V or 1.8/2.5/3.3V | 1.2V or 1.8/2.5/3.3V |
| **Number of PLLs** | – | – | 1 | 2 |
| **Number of I/O Banks** | 2 | 4 | 8 | 8 |
| **Maximum Number of I/Os** | 78 | 159 | 211 | 271 |
| **Maximum Number of LVDS Pairs*** | – | – | 27 | 33 |
| **Packages & I/O Combinations** | | | | |
| **100-pin TQFP (14 x 14 mm)**** | 78 | 74 | 73 | 73 |
| **144-pin TQFP (20 x 20 mm)** | | 113 | 113 | 113 |
| **100-ball csBGA (8 x 8 mm)** | 78 | 74 | | |
| **132-ball csBGA (8 x 8 mm)** | | 101 | 101 | 101 |
| **256-ball caBGA (14 x 14 mm)** | | 159 | 211 | 211 |
| **256-ball ftBGA (17 x 17 mm)** | | 159 | 211 | 211 |
| **324-ball ftBGA (19 x 19 mm)** | | | | 271 |

** Number of LVDS outputs can be increased by emulating with external resistors.*

*** In the 100-pin TQFP package, designs can not migrate from LCMXO640 to 1200.*

**Applications Support**
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