

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL CLOCK GENERATOR

ICS843252-04

GENERAL DESCRIPTION



The ICS843252-04 is a 10Gb/12Gb Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS843252-04 can synthesize 10 Gigabit Ethernet and 12 Gigabit Ethernet with a 25MHz crystal. It can also generate SATA and 10Gb Fibre Channel reference clock frequencies with the appropriate choice of crystals. The ICS843252-04 has excellent phase jitter performance and is packaged in a small 16-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- Two differential 3.3V LVPECL output
- Crystal oscillator interface designed for 18pF parallel resonant crystals
- Crystal input frequency range: 19.33MHz - 30MHz
- Output frequency range: 145MHz - 187.5MHz
- VCO frequency range: 580MHz - 750MHz
- RMS phase jitter at 156.25MHz (1.875MHz - 20MHz): 0.39ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

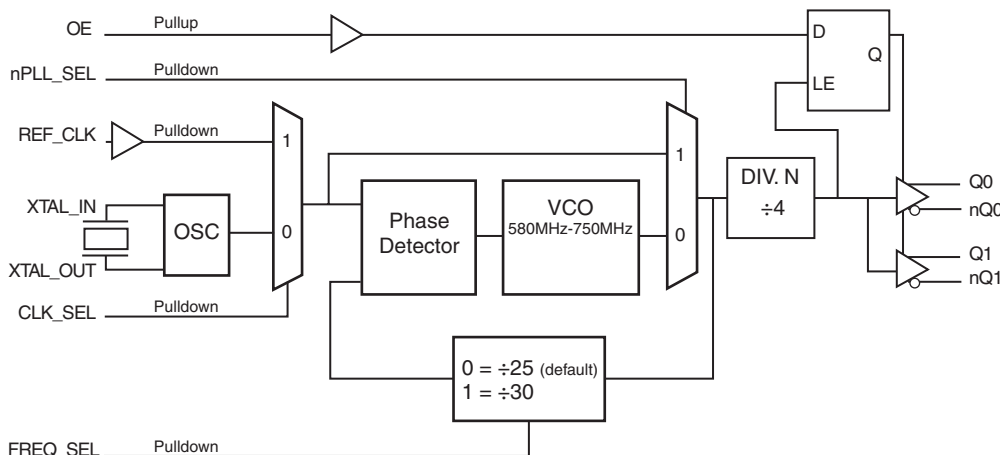
CONFIGURATION TABLE WITH 25MHz CRYSTAL

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
25	30	750	4	187.5	12 Gigabit Ethernet
25	25	625	4	156.25	10 Gigabit Ethernet

CONFIGURATION TABLE WITH SELECTABLE CRYSTALS

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
20	30	600	4	150	SATA
21.25	30	637.5	4	159.375	10 Gigabit Fibre Channel
24	25	600	4	150	SATA
25.5	25	637.5	4	159.375	10 Gigabit Fibre Channel
30	25	750	4	187.5	12 Gigabit Ethernet

BLOCK DIAGRAM



PIN ASSIGNMENT

nQ1	1	16	XTAL_IN
Q1	2	15	XTAL_OUT
Vcco	3	14	VEE
OE	4	13	REF_CLK
nPLL_SEL	5	12	CLK_SEL
Vcco	6	11	Vcc
Q0	7	10	VCCA
nQ0	8	9	FREQ_SEL

ICS843252-04

16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm

package body

G Package

Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential clock outputs. LVPECL interface levels.
3, 6	V _{CCO}	Power		Output supply pins.
4	OE	Input	Pullup	Output enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL interface levels.
5	nPLL_SEL	Input	Pulldown	Selects between the PLL and reference clock as input to the divider. When Low, selects PLL. When High, selects reference clock. LVCMOS/LVTTL interface levels.
7, 8	Q0, nQ0	Output		Differential clock outputs. LVPECL interface levels.
9	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
10	V _{CCA}	Power		Analog supply pin.
11	V _{CC}	Power		Core supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When Low, selects crystal inputs. When High, selects REF_CLK. LVCMOS/LVTTL interface levels.
13	REF_CLK	Input	Pulldown	Reference clock input. LVCMOS/LVTTL interface levels.
14	V _{EE}	Power		Negative supply pin.
15, 16	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	92.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current			60		mA
I_{CCA}	Analog Supply Current			11		mA
I_{EE}	Power Supply Current			80		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, CLK_SEL, FREQ_SEL, nPLL_SEL	$V_{CC} = V_{IN} = 3.465V$		150	μA
		OE	$V_{CC} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	REF_CLK, CLK_SEL, FREQ_SEL, nPLL_SEL	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		μA
		OE	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		μA

TABLE 3C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.33		30	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		145		187.5	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	156.25MHz @ Integration Range: 1.875MHz - 20MHz		0.39		ps
		159.375MHz @ Integration Range: 1.875MHz - 20MHz		0.38		ps
		187.5MHz @ Integration Range: 1.875MHz - 20MHz		0.38		ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3					ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

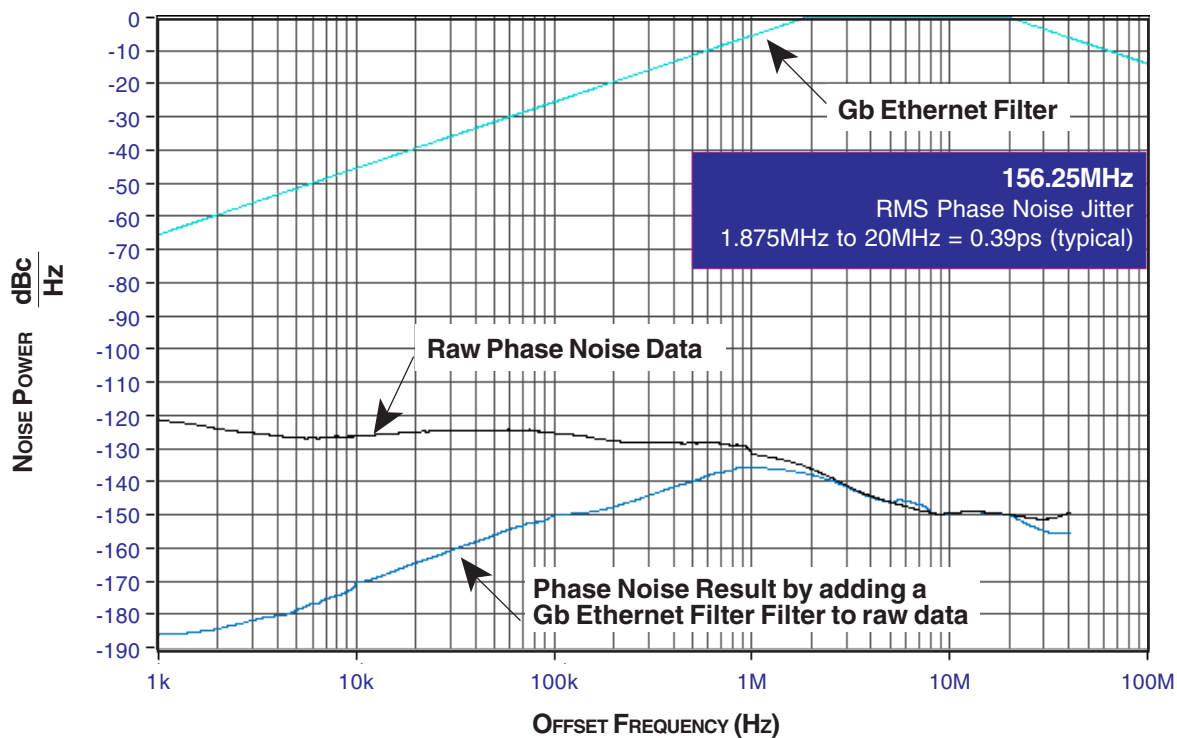
NOTE 1: Please refer to the Phase Noise Plots following this section.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

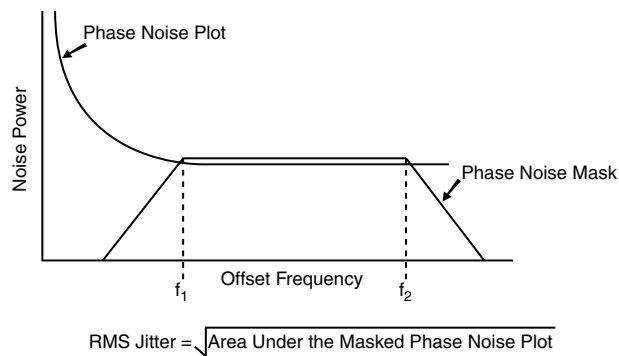
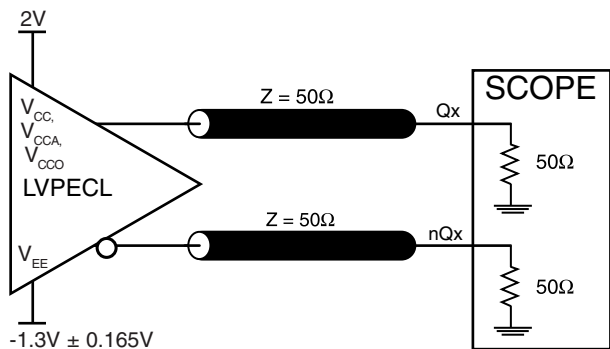
Measured at $V_{CCO}/2$.

NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

TYPICAL PHASE NOISE AT 156.25MHz

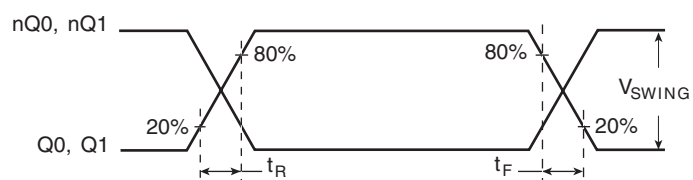
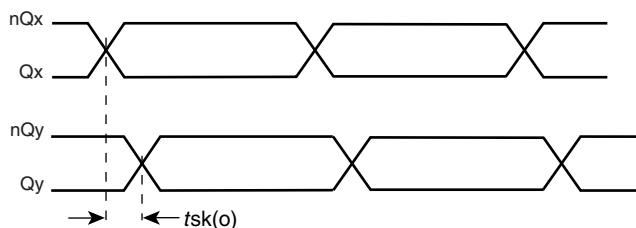


PARAMETER MEASUREMENT INFORMATION



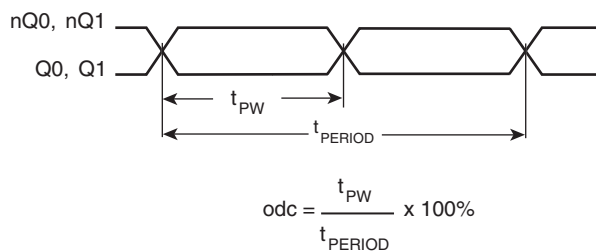
3.3V OUTPUT LOAD AC TEST CIRCUIT

RMS PHASE JITTER



OUTPUT SKEW

OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843252-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} , and V_{CCO} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{CCA} pin.

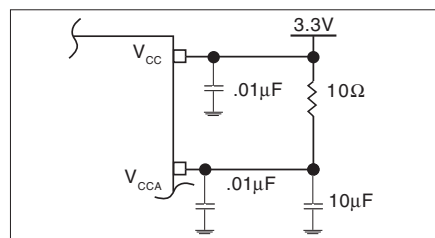


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the REF_CLK to ground.

LVC MOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CRYSTAL INPUT INTERFACE

The ICS843252-04 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

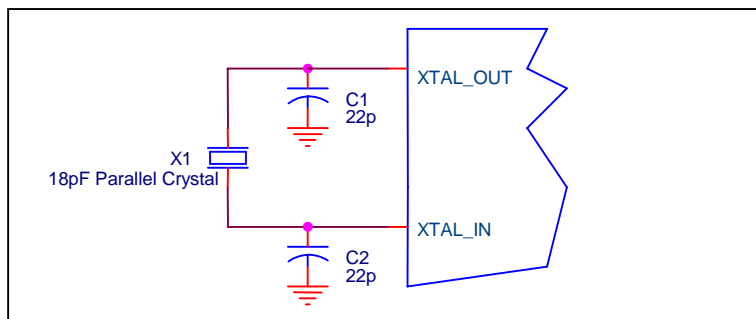


FIGURE 2. CRYSTAL INPUT INTERFACE

LVC MOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

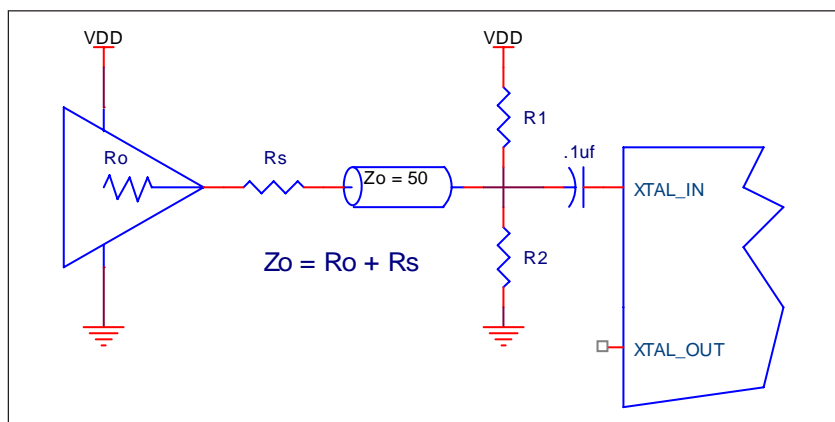


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

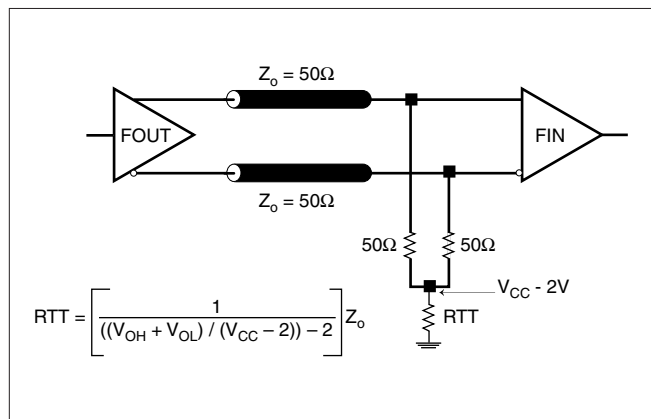


FIGURE 4A. LVPECL OUTPUT TERMINATION

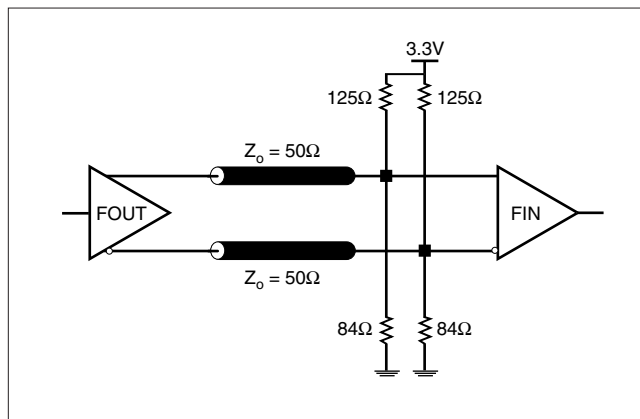


FIGURE 4B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843252-04. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843252-04 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 80mA = 277.2mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30mW = 60mW$

$$\text{Total Power}_{_MAX} (3.465V, \text{ with all outputs switching}) = 277.2mW + 60mW = 337.2mW$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.4°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.337W * 92.4^\circ C/W = 101.1^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16 LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

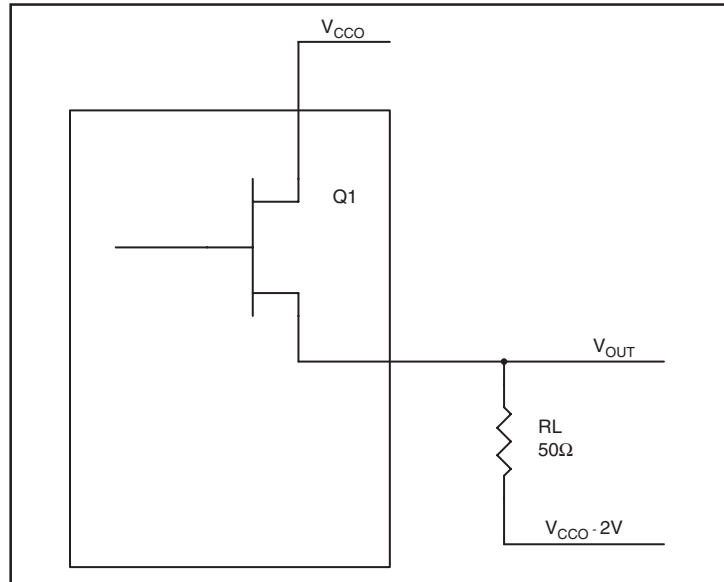


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$
 $(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$
 $(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

	θ_{JA} by Velocity (Meters per Second)		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

TRANSISTOR COUNT

The transistor count for ICS843252-04 is: 2210

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

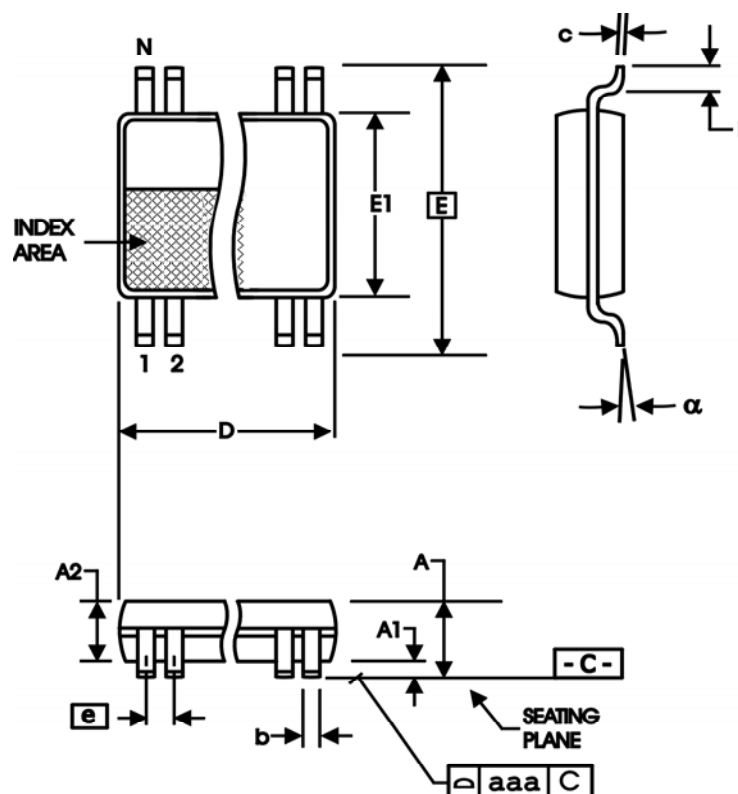


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843252AG-04	43252A04	16 Lead TSSOP	tube	0°C to 70°C
843252AG-04T	43252A04	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
843252AG-04LF	3252A04L	16 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
843252AG-04LFT	3252A04L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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