FEMTOCLOCKS™ CRYSTAL-TO-LVDS CLOCK GENERATOR

ICS844031-01

General Description

The ICS844031-01 is an Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS844031-01 uses an 18pF parallel resonant crystal over the range of 19.6MHz - 27.2MHz. For Ethernet applications, a 25MHz crystal is used to generate 312.5MHz. The ICS844031-01 has excellent <1ps phase jitter performance, over the 1.875MHz - 20MHz integration range. The ICS844031-01 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

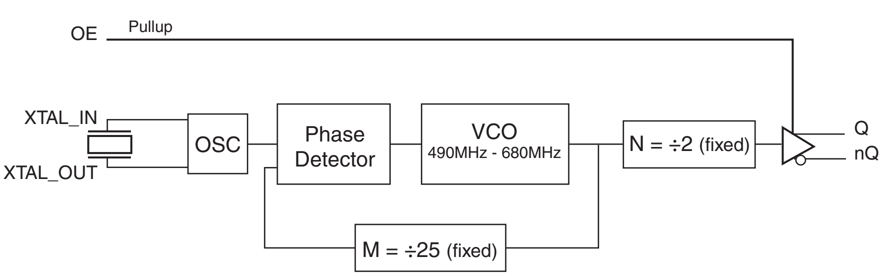
Features

- One differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (19.6MHz - 27.2MHz)
- Output frequency range: 245MHz - 340MHz
- VCO range: 490MHz - 680MHz
- RMS phase jitter @ 312.5MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.53ps (typical)
- 3.3V or 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

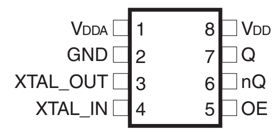
Common Configuration Table

Inputs				Output Frequency (MHz)
Crystal Frequency (MHz)	M	N	Multiplication Value M/N	
25	25	2	12.5	312.5

Block Diagram



Pin Assignment



ICS844031-01
8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Output enable pin. When HIGH, Q/nQ output is active. When LOW, the Q/nQ output is in a high impedance state. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVDS interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
I_{DD}	Power Supply Current				75	mA
I_{DDA}	Analog Supply Current				10	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	2.5	V_{DD}	V
I_{DD}	Power Supply Current				70	mA
I_{DDA}	Analog Supply Current				10	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 3D. LVDS DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		275		425	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15	1.33	1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 3E. LVDS DC CHARACTERISTICS, V_{DD} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		215		430	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.05	1.26	1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.6		27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 5A. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		245		340	MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.53		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		400	ps
odc	Output Duty Cycle		48		52	%

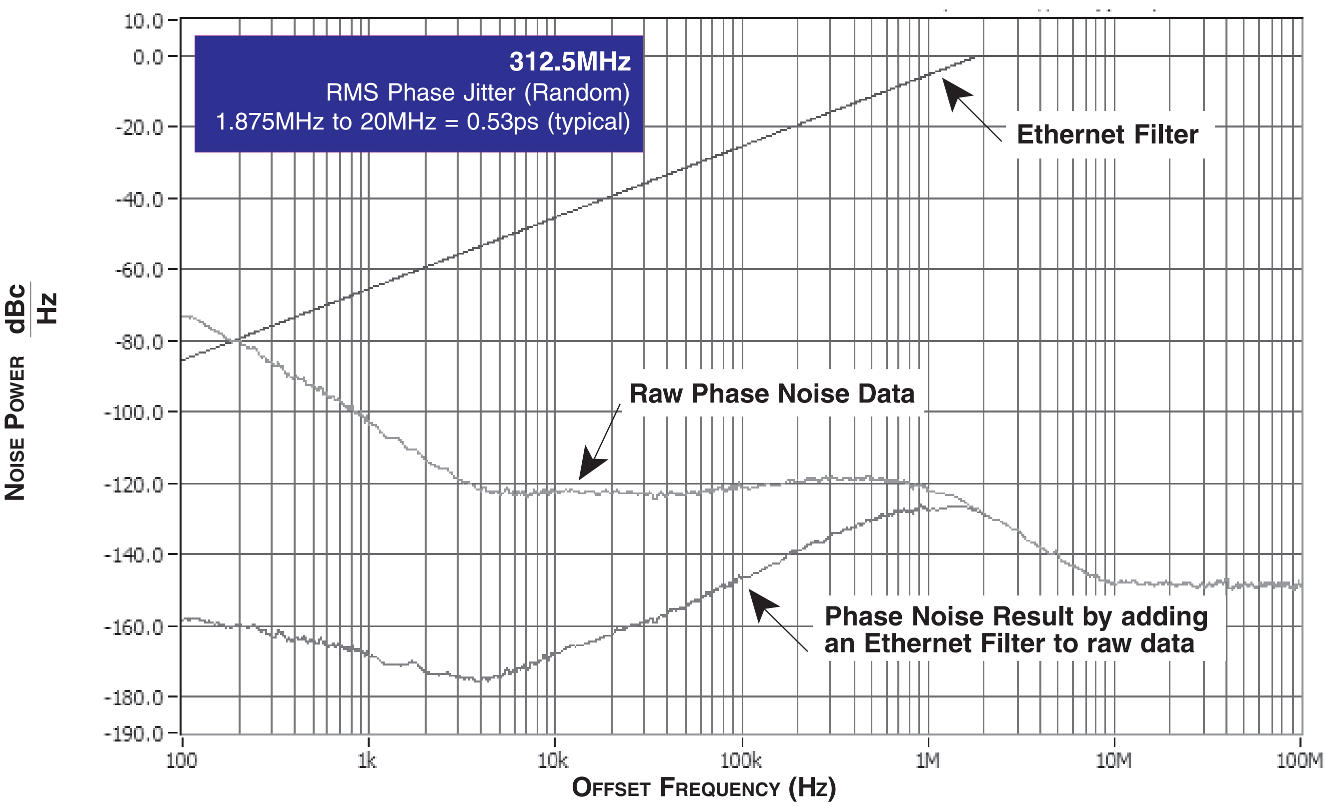
NOTE 1: Please refer to the Phase Noise Plots following this section.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, TA = 0°C TO 70°C

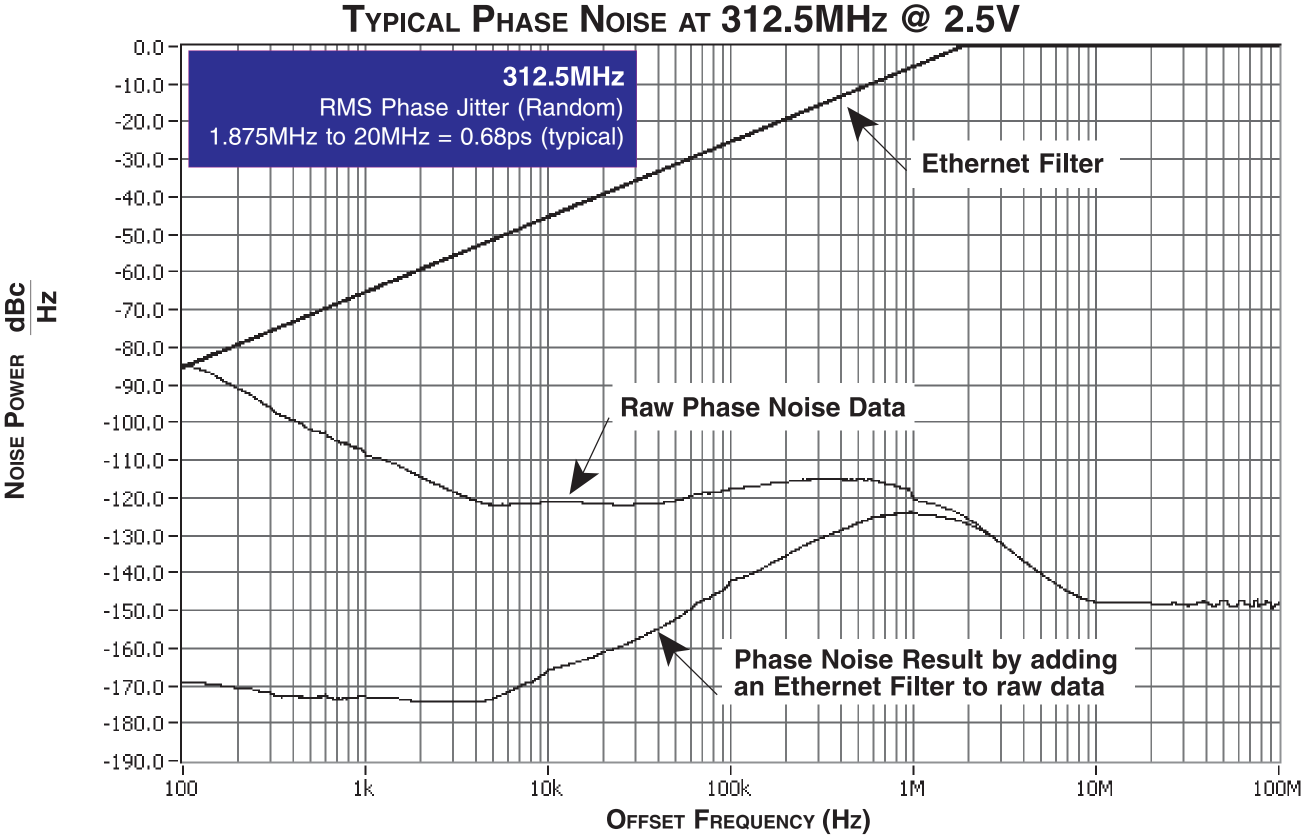
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		245		340	MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.68		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		400	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to the Phase Noise Plots following this section.

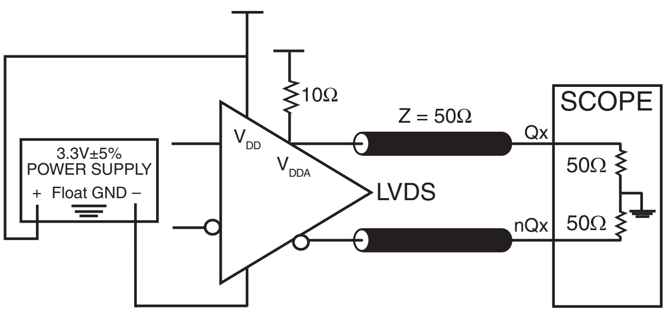
Typical Phase Noise at 312.5MHz @ 3.3V



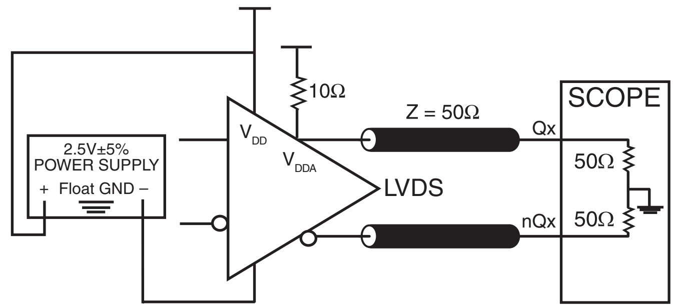
Typical Phase Noise at 312.5MHz @ 2.5V



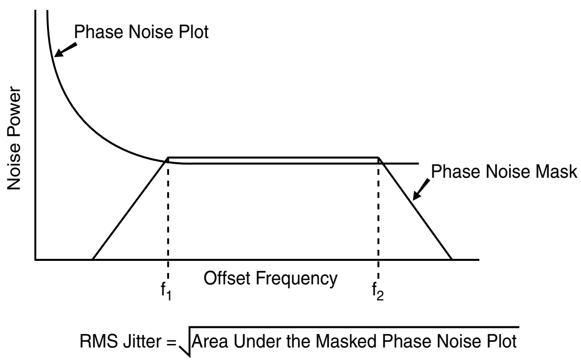
PARAMETER MEASUREMENT INFORMATION



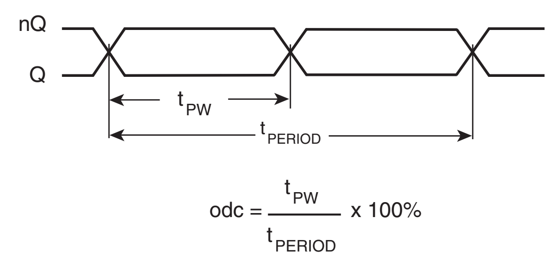
LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT



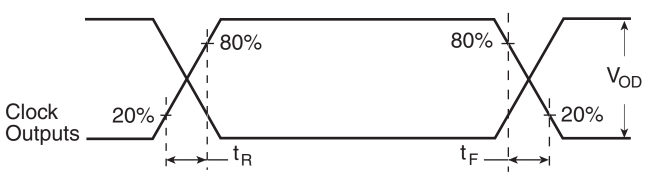
LVDS 2.5V OUTPUT LOAD AC TEST CIRCUIT



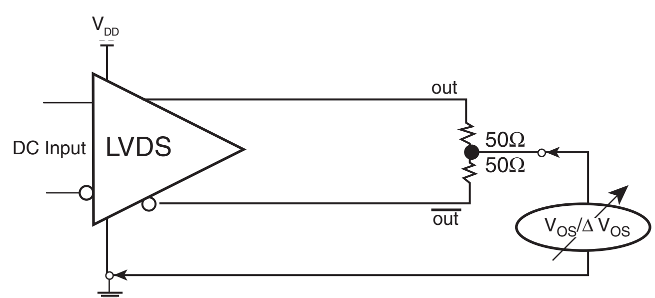
RMS PHASE JITTER



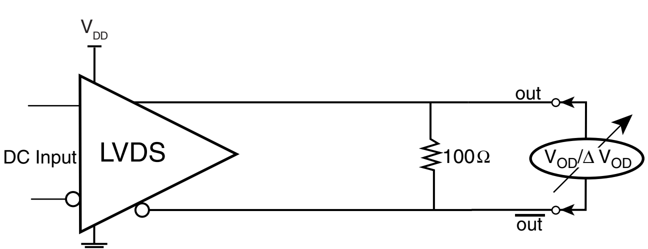
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844031-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

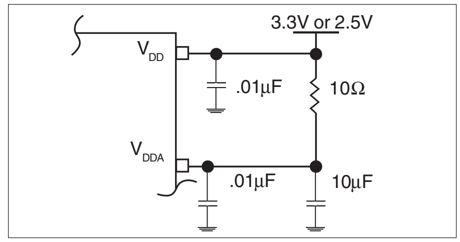


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844031-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

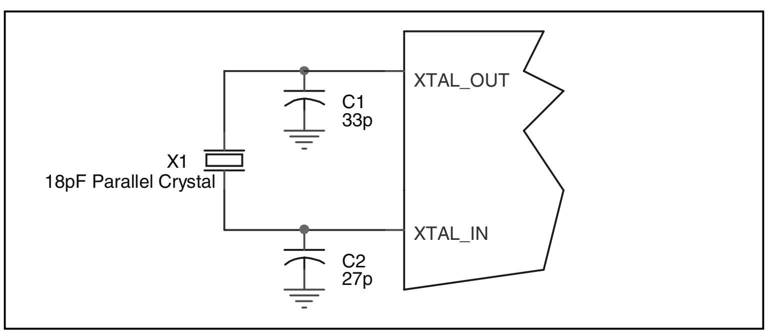


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

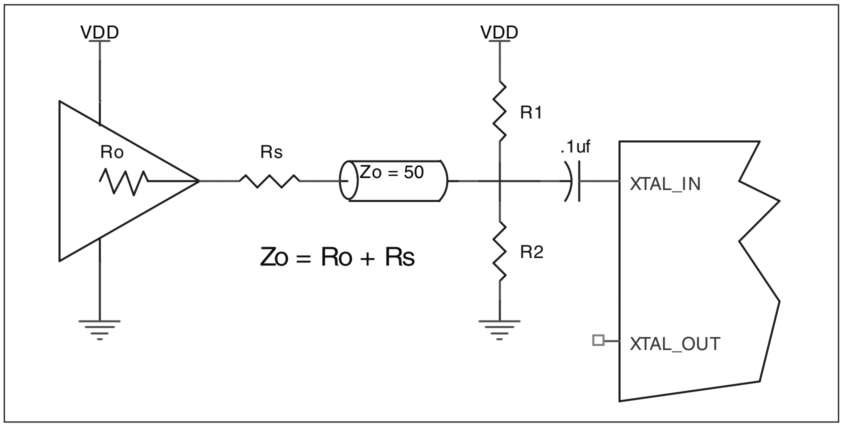


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

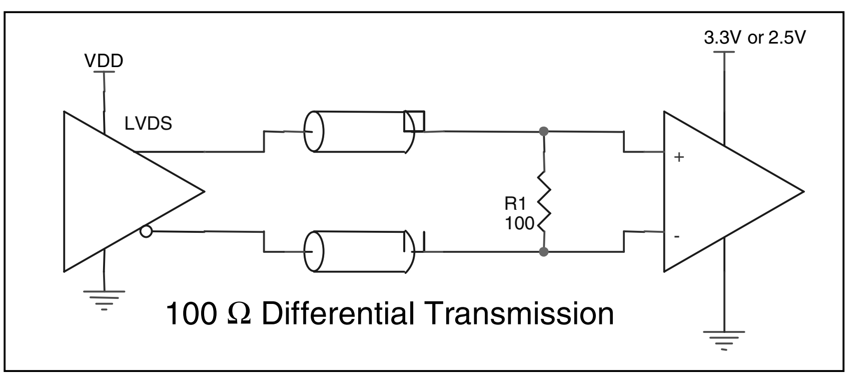


Figure 4. Typical LVDS Driver Termination

Application Schematic

Figure 5A provides a schematic example of ICS844031-01. In this example, an 18 pF parallel resonant crystal is used. The C1= 22pF and C2 = 22pF are recommended for frequency. The C1 and C2 values may be slightly adjusted for optimizing frequency accuracy. At least one decoupling capacitor near the power pin is required. Suggested value range is from 0.01uF to 0.1uF. Other filter type can be added depending on the system power supply noise type.

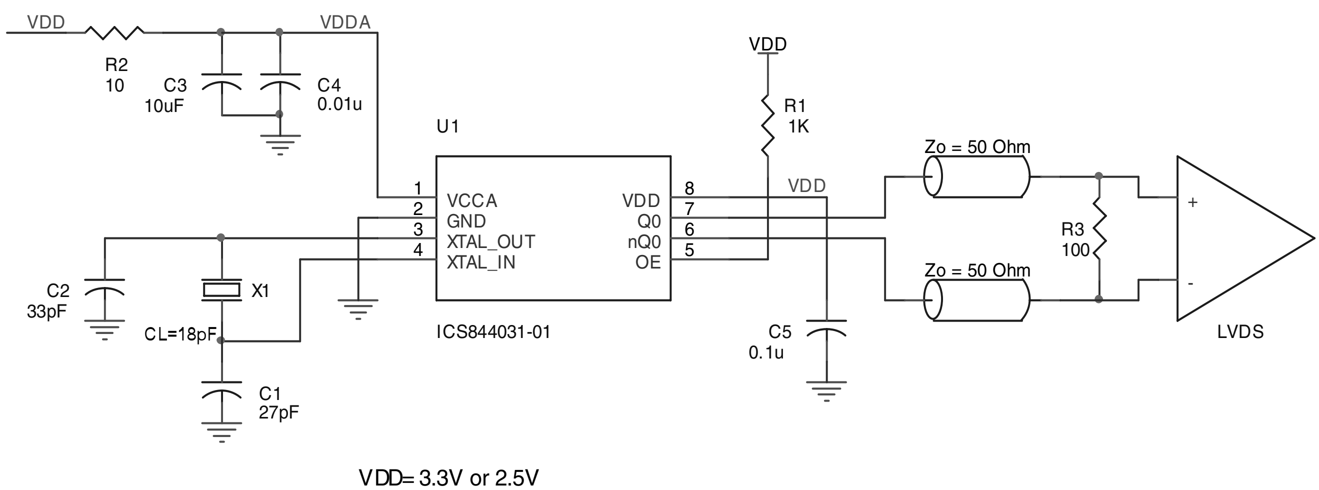


Figure 5A. Application Schematic Example

PC Board Layout Example

Figure 5B shows an example of ICS844031-01 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

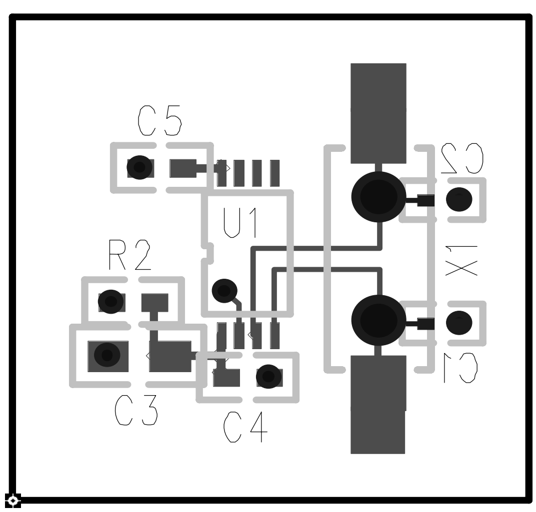


Figure 5B. ICS844031-01 PC Board Layout Example

Table 6. Footprint Table

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2	0603

NOTE: Table 6, lists component sizes shown in this layout example.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844031-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844031-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (75mA + 10mA) = **294.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.294W * 129.5°C/W = 108.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 8-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 8 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Transistor Count

The transistor count for ICS844031-01 is: 2519

Package Outline - G Suffix for 8 Lead TSSOP

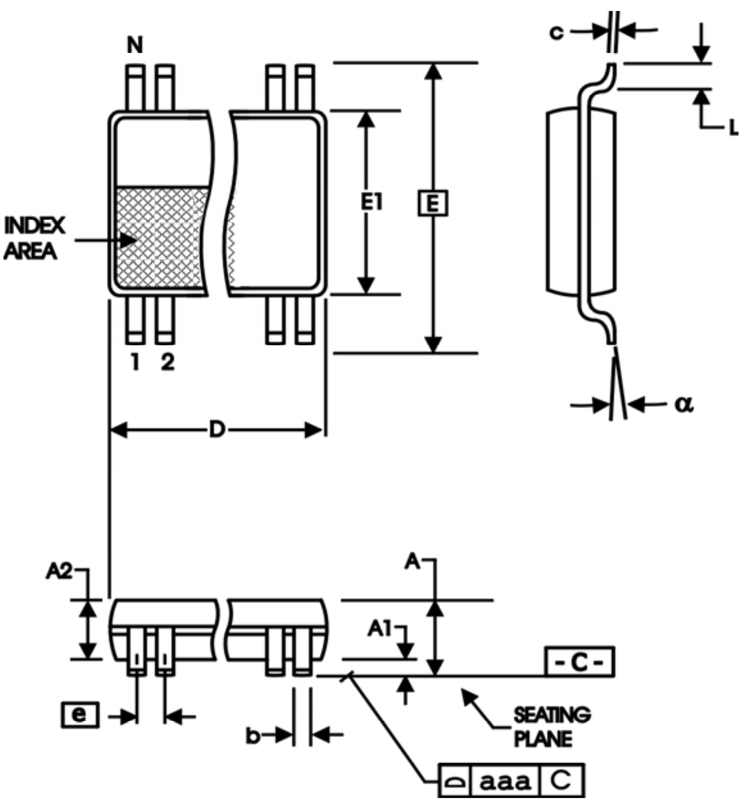


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844031BG-01	TBD	8 lead TSSOP	tube	0°C to 70°C
ICS844031BG-01T	TBD	8 lead TSSOP	2500 tape & reel	0°C to 70°C
ICS844031BG-01LF	1B01L	8 lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS844031BG-01LFT	1B01L	8 lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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For Tech Support
netcom@idt.com
+480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)