12:1, Differential-to-3.3V, 2.5V LVPECL Clock/Data Multiplexer

ICS853S012I

PRELIMINARY DATA SHEET

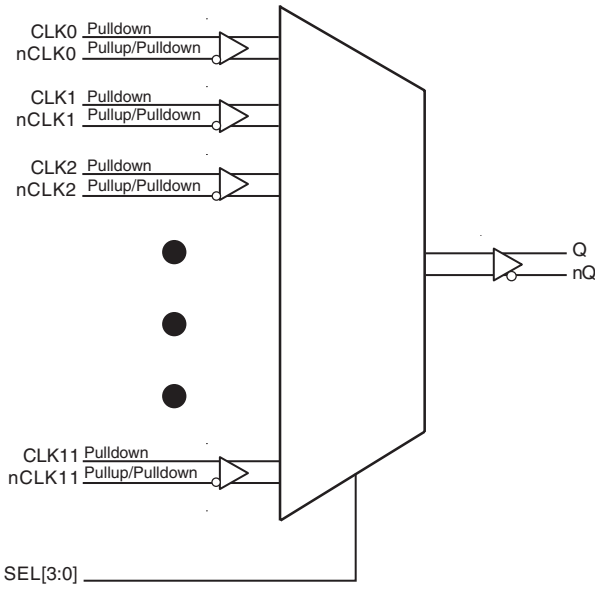
General Description

The ICS853S012I is an 12:1 Differential-to-3.3V or 2.5V LVPECL Clock/Data Multiplexer which can operate up to 3.2GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS853S012I has 12 differential selectable clock inputs. The CLK, nCLK input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors.

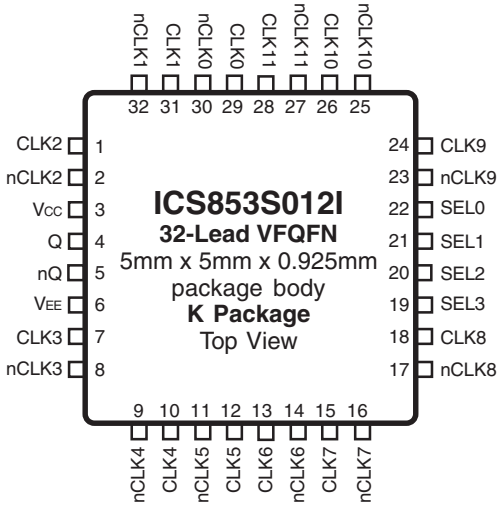
Features

- High speed 12:1 differential multiplexer
- One differential 3.3V or 2.5V LVPECL output
- Twelve selectable differential clock or data inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 3.2GHz (typical)
- Translates any single ended input signal to LVPECL levels with resistor bias on nCLKx input
- Additive phase jitter, RMS: 0.13ps (typical)
- Part-to-part skew: TBD
- Propagation delay: 685ps (typical)
- Full 3.3V or 2.5V operating supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK2	Input	Pulldown	Non-inverting differential clock input.
2	nCLK2	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
3	V_{CC}	Power		Positive supply pin.
4, 5	Q, nQ	Output		Differential output pair. LVPECL interface levels.
6	V_{EE}	Power		Negative supply pin.
7	CLK3	Input	Pulldown	Non-inverting differential clock input.
8	nCLK3	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
9	nCLK4	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
10	CLK4	Input	Pulldown	Non-inverting differential clock input.
11	nCLK5	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
12	CLK5	Input	Pulldown	Non-inverting differential clock input.
13	CLK6	Input	Pulldown	Non-inverting differential clock input.
14	nCLK6	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
15	CLK7	Input	Pulldown	Non-inverting differential clock input.
16	nCLK7	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
17	nCLK8	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
18	CLK8	Input	Pulldown	Non-inverting differential clock input.
19, 20 21, 22	SEL3, SEL2, SEL1, SEL0	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
23	nCLK9	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
24	CLK9	Input	Pulldown	Non-inverting differential clock input.
25	nCLK10	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
26	CLK10	Input	Pulldown	Non-inverting differential clock input.
27	nCLK11	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
28	CLK11	Input	Pulldown	Non-inverting differential clock input.
29	CLK0	Input	Pulldown	Non-inverting differential clock input.
30	nCLK0	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
31	CLK1	Input	Pulldown	Non-inverting differential clock input.
32	nCLK1	Input	Pullup/Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Pulldown Resistor			50		kΩ
$R_{VCC}/2$	Pullup/Pulldown Resistor			50		kΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Control Inputs				Outputs	
SEL3	SEL2	SEL1	SEL0	Q	nQ
0	0	0	0	CLK0	nCLK0
0	0	0	1	CLK1	nCLK1
0	0	1	0	CLK2	nCLK2
0	0	1	1	CLK3	nCLK3
0	1	0	0	CLK4	nCLK4
0	1	0	1	CLK5	nCLK5
0	1	1	0	CLK6	nCLK6
0	1	1	1	CLK7	nCLK7
1	0	0	0	CLK8	nCLK8
1	0	0	1	CLK9	nCLK9
1	0	1	0	CLK10	nCLK10
1	0	1	1	CLK11	nCLK11
1	1	X	X	L	H

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA} For 32 Lead VFQFN	39.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			70		mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			65		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SEL0:SEL3	$V_{CC} = V_{IN}$ = 3.465V, $V_{CC} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	SEL0:SEL3	V_{CC} = 3.465V, V_{IN} = 0V, V_{CC} = 2.625V, V_{IN} = 0V	-10			µA

Table 4D. Differential DC Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0:CLK11 nCLK0:nCLK11	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK0:CLK11	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		nCLK0:nCLK11	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.5	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{CC}	V

NOTE 1: V_{IL} should not be less than -0.3V
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage Voltage; NOTE 1		V_{CC} - 1.125		V_{CC} - 0.935	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 1.895		V_{CC} - 1.670	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4F. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage Voltage; NOTE 1			V_{CC} – 1.0V		V
V_{OL}	Output Low Voltage; NOTE 1			V_{CC} – 1.4V		V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5A. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			3.2		GHz
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, 12kHz - 20MHz		0.13		ps
t_{PD}	Propagation Delay	CLKx, nCLKx to Q, nQ; NOTE 1A		685		ps
		SEL[3:0] to Q, nQ; NOTE 1B				ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					ps
*t*sk(i)	Input Skew			35		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		135		ps
$MUX_{—ISOLATION}$	Mux Isolation	155.52MHz, Input Peak-to-Peak = 800mV		60		dB

All parameters measured up to 1.3GHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditons.
NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.
NOTE 1B: Measured from the 50% point of the single-ended input signal to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			3.2		GHz
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, 12kHz - 20MHz		0.14		ps
t_{PD}	Propagation Delay	CLKx, nCLKx to Q, nQ; NOTE 1A		690		ps
		SEL[3:0] to Q, nQ; NOTE 1B				ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					ps
*t*sk(i)	Input Skew			55		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		125		ps
$MUX_{\_ISOLATION}$	Mux Isolation	155.52MHz, Input Peak-to-Peak = 800mV		60		dB

All parameters measured up to 1.3GHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditons.
NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.
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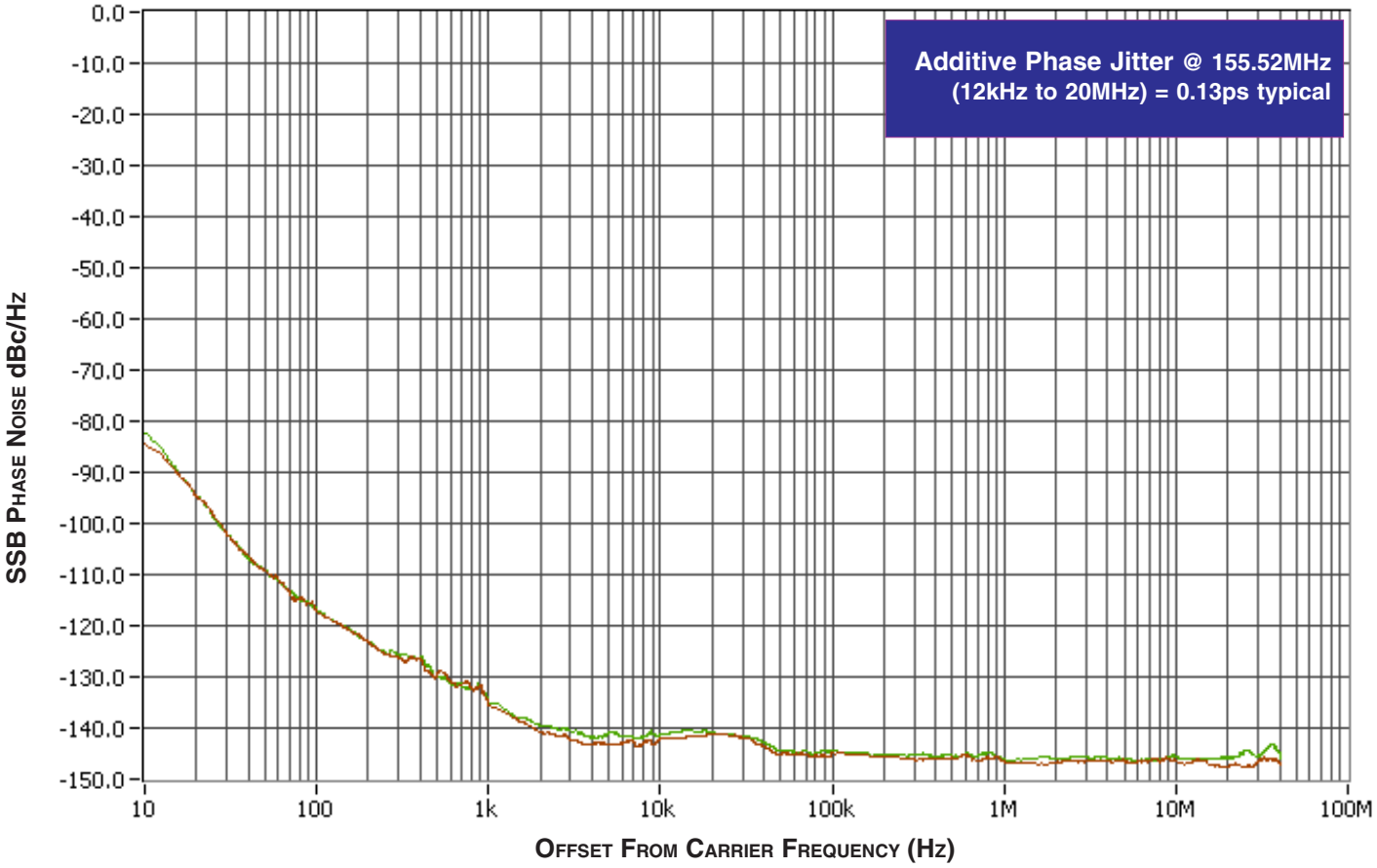
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.

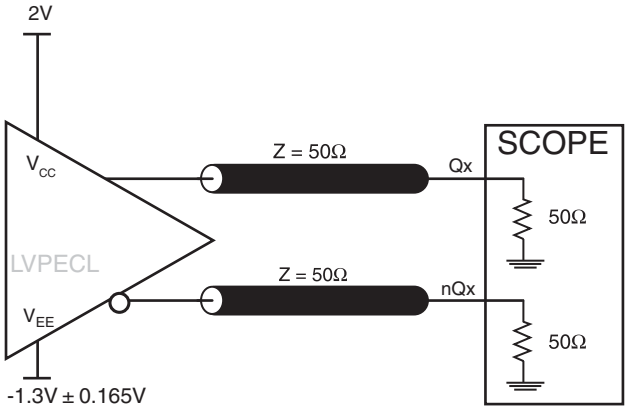
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

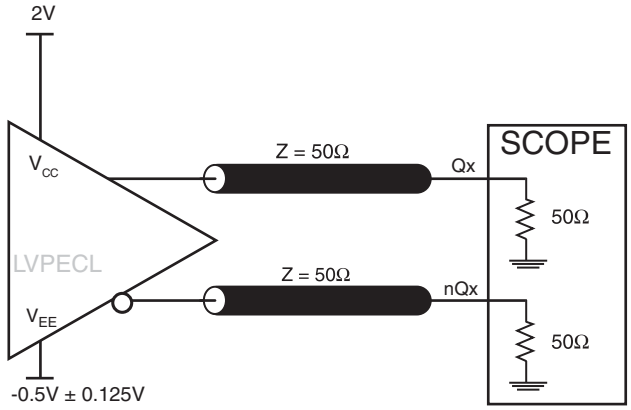


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

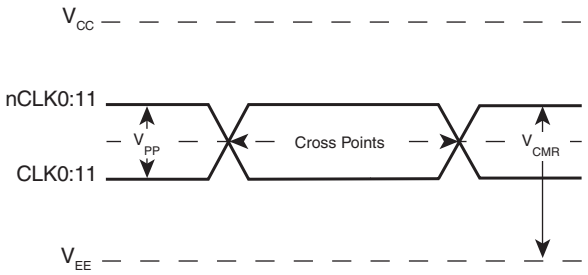
PARAMETER MEASUREMENT INFORMATION



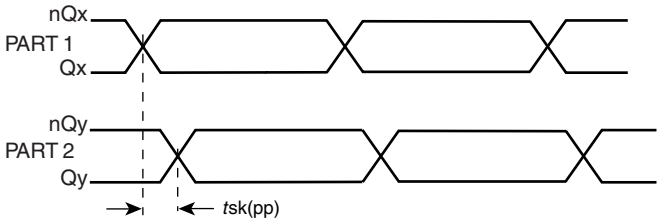
OUTPUT LOAD 3.3V AC TEST CIRCUIT



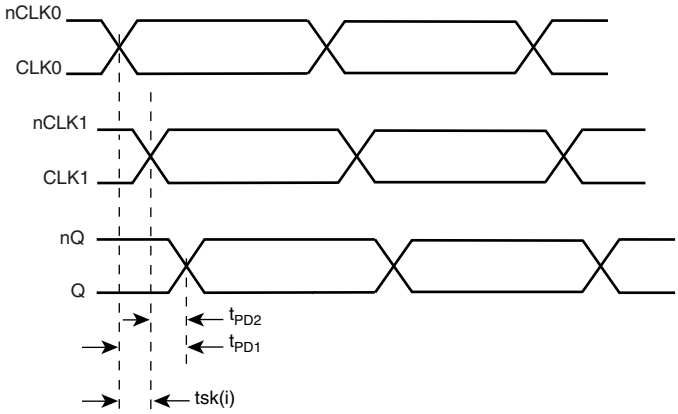
OUTPUT LOAD 2.5V AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL

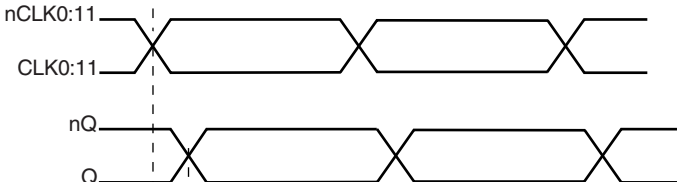


PART-TO-PART SKEW

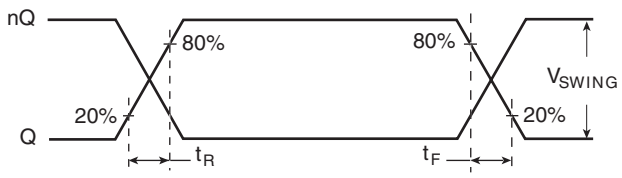


$$tsk(i) = |t_{PD1} - t_{PD2}|$$

INPUT SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

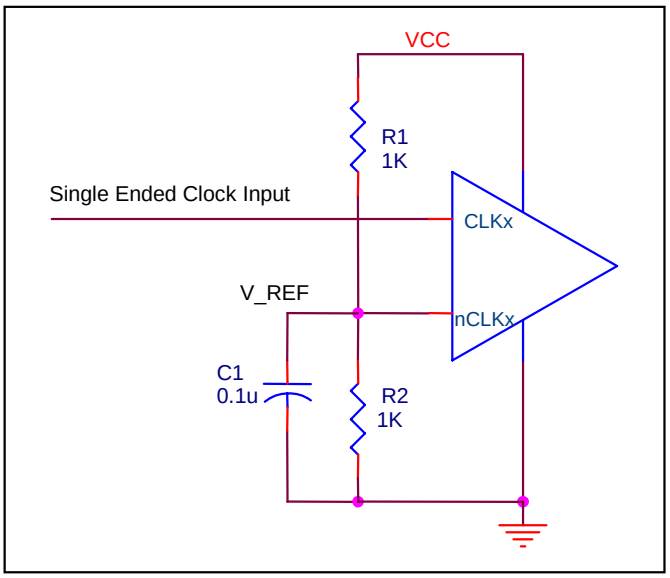


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

The unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

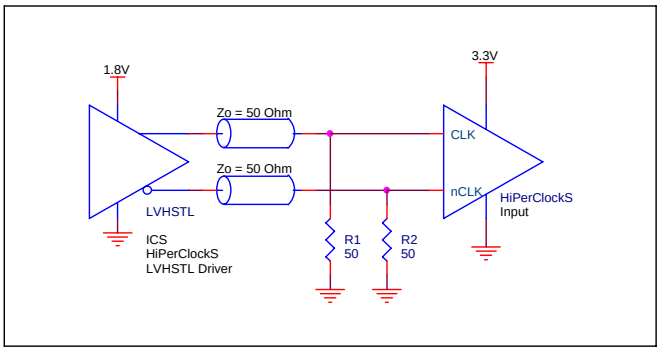


Figure 2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

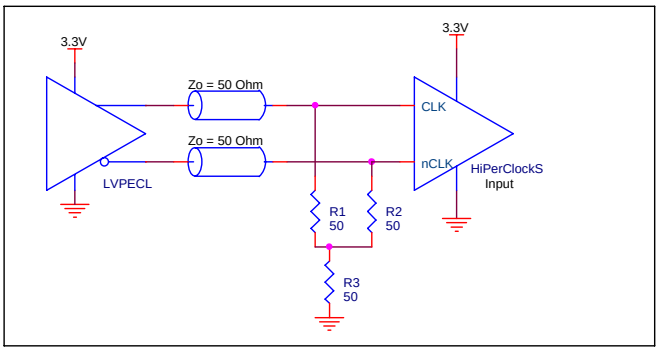


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

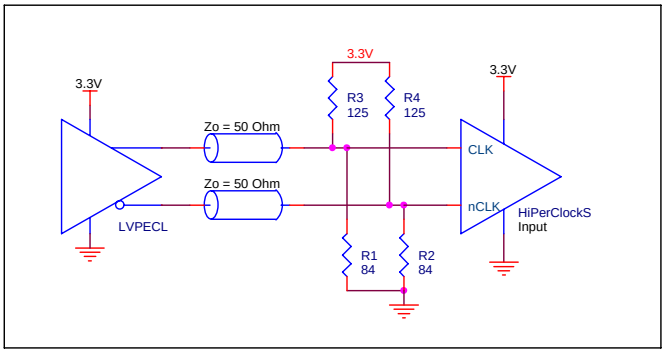


Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

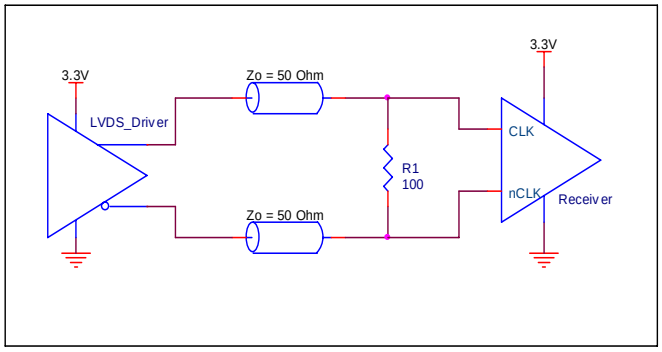


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

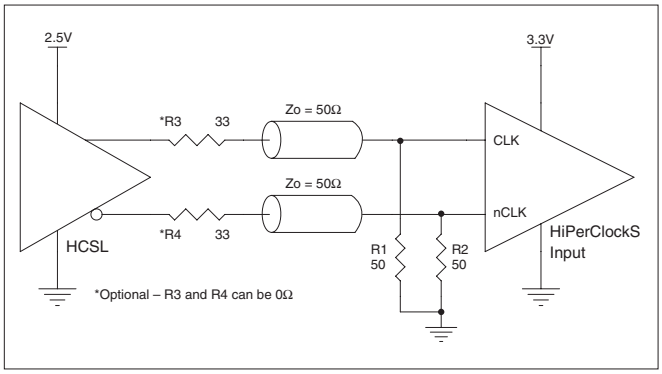


Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

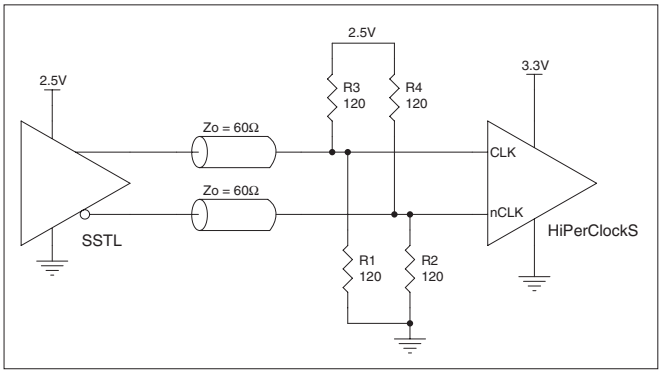


Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

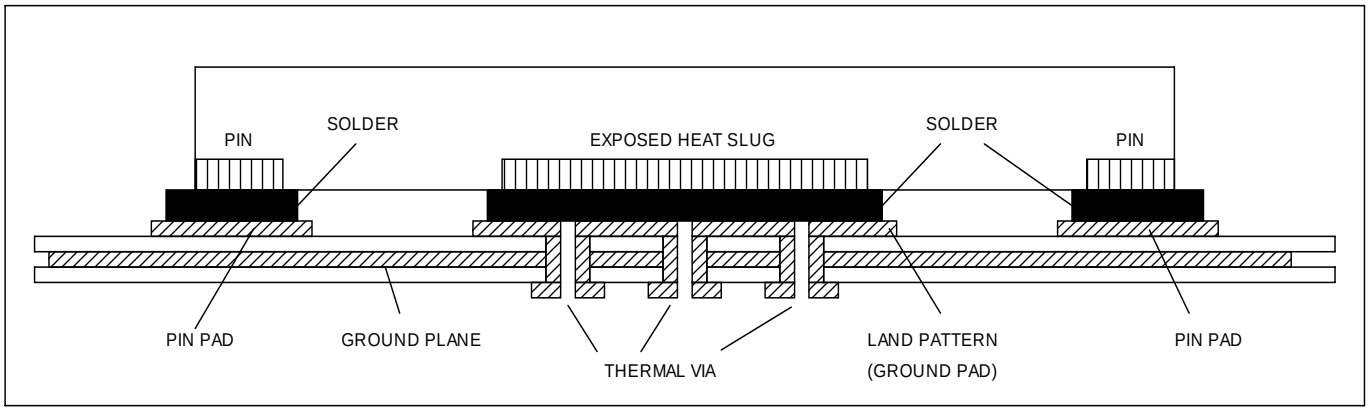


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

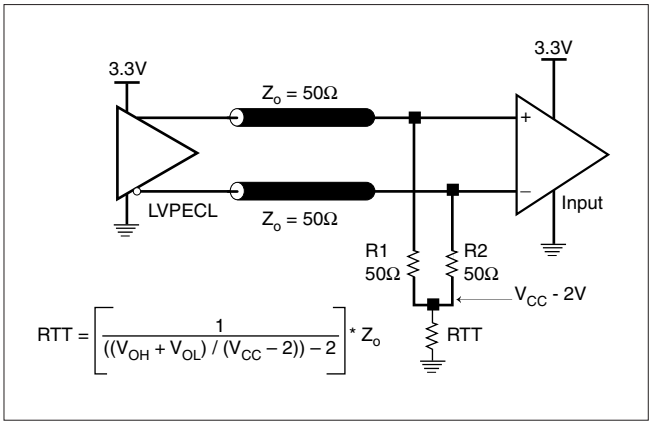


FIGURE 4A. LVPECL OUTPUT TERMINATION

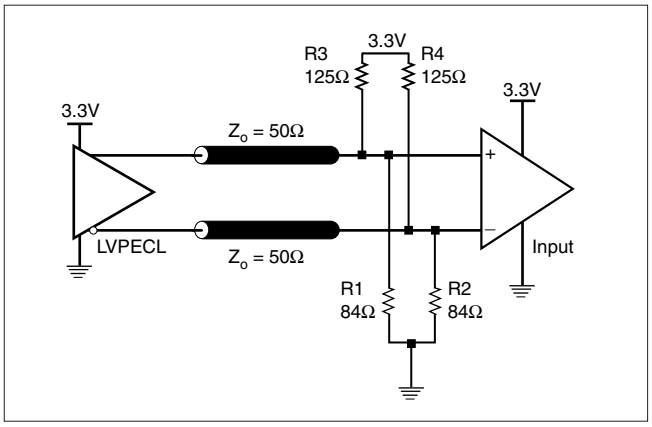


FIGURE 4B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

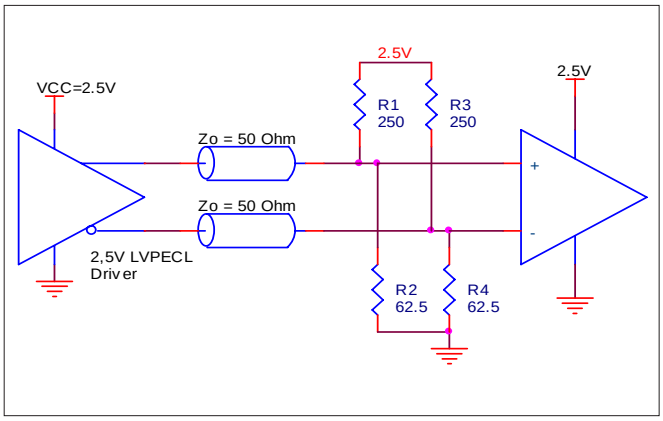


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

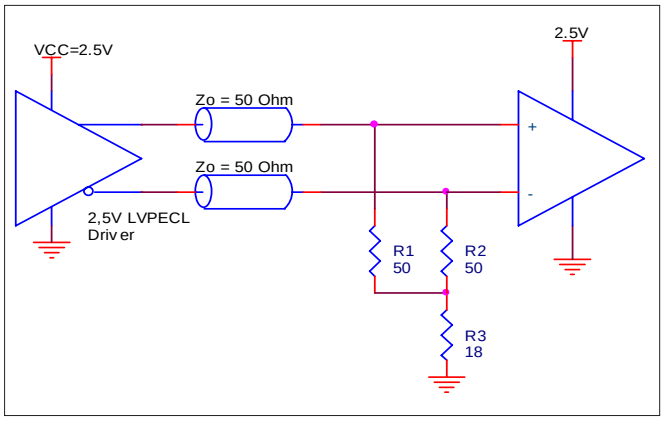


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

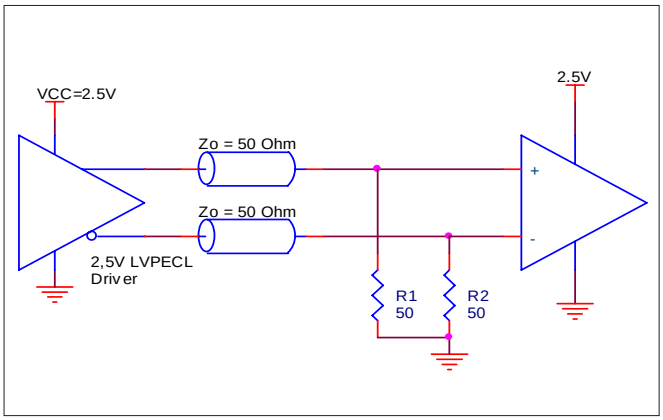


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853S012I. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853S012I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 70mA = **242.6mW**
- Power (outputs)$_{MAX}$ = **30.94mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 242.6mW + 30.94mW = **273.5mW**

2. Junction Temperature.
Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.274W * 39.5°C/W = 95.85°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32 LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

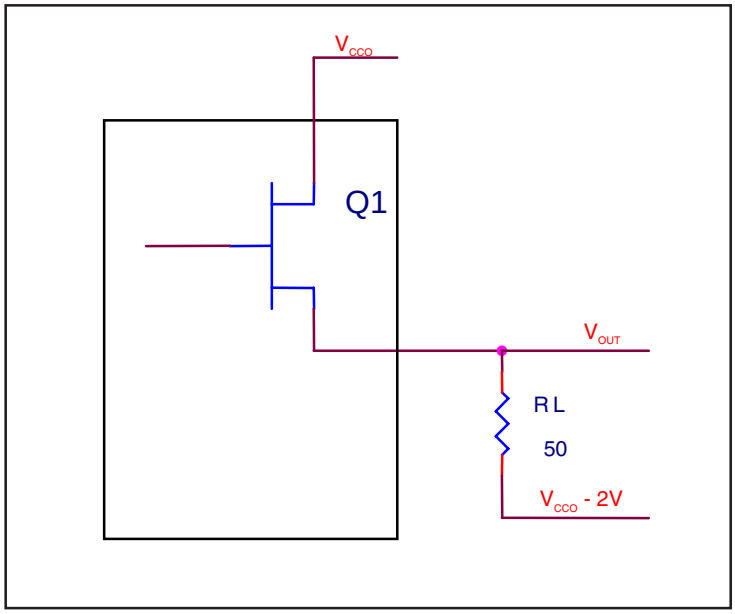


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} – 0.935V$

  $(V_{CC\_MAX} - V_{OH\_MAX}) =$ **0.935V**

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} – 1.67V$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) =$ **1.67V**

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$

[(2V - 0.935V)/50Ω] * 0.935V = **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$

[(2V - 1.67V)/50Ω] * 1.67V = **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

RELIABILITY INFORMATION

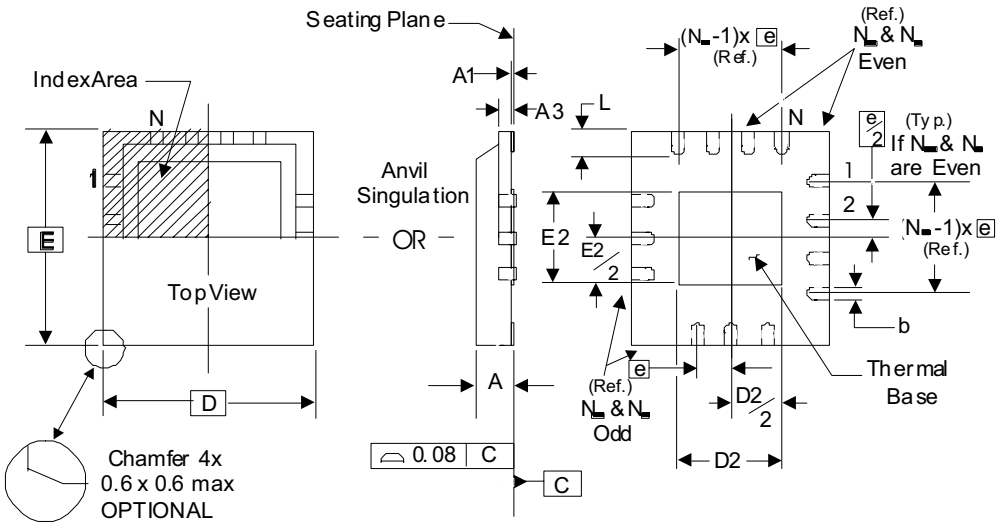
TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

TRANSISTOR COUNT

The transistor count for ICS853S012I is: 8,537

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N_D			8
N_E			8
D	5.00 BASIC		
D2	3.0		3.30
E	5.00 BASIC		
E2	3.0		3.30
e	0.50 BASIC		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S012AKI	ICS53S012AI	32 Lead VFQFN	Tray	-40°C to 85°C
853S012AKIT	ICS53S012AI	32 Lead VFQFN	1000 Tape & Reel	-40°C to 85°C
853S012AKILF	ICS3S012AIL	32 Lead "Lead-Free" VFQFN	Tray	-40°C to 85°C
853S012AKILFT	ICS3S012AIL	32 Lead "Lead-Free" VFQFN	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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