LOW SKEW, 2:1 LVPECL MUX WITH 1:6 FANOUT AND INTERNAL TERMINATION

ICS8S58035I

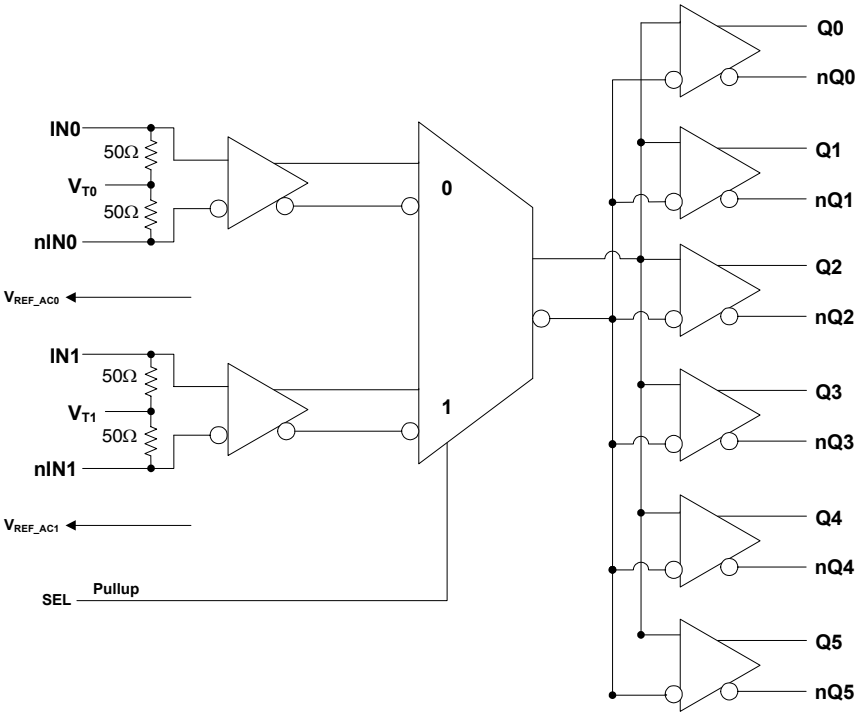
General Description

The ICS8S58035I is a high speed 2-to-6 Differential-to-LVPECL/ECL Fanout Buffer and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS8S58035I is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential inputs and V_{REF_AC} pins allow other differential signal families such as LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The device also has a 2:1 MUX input, allowing for easy selection between two clock reference sources. The ICS8S58035I is packaged in a small 5mm x 5mm 32-pin VFQFN package which makes it ideal for use in space-constrained applications.

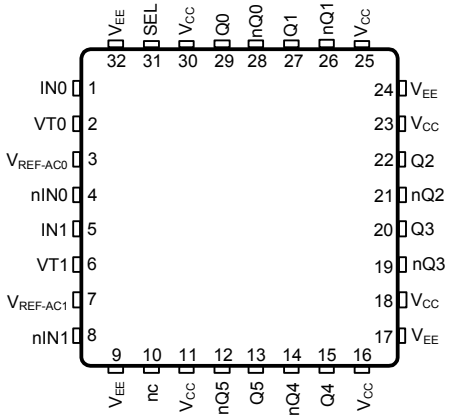
Features

- Six LVPECL/ECL outputs
- INx, nINx inputs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Two selectable differential input pairs.
- Maximum output frequency: 3.2GHz
- Output Skew: 15ps (typical)
- Part-to-Part Skew: TBD
- Additive phase jitter, RMS: 0.12ps (typical)
- Propagation Delay: 700ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.5V±5%, 3.3V±10%, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.3V±10%, 2.5V±5%
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages.

Block Diagram



Pin Assignment



ICS8S58035I
32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 5	IN0, IN1	Input		Non-inverting differential LVPECL clock inputs. RT = 50Ω termination to V_T.
2, 6	VT0, VT1	Input		Termination inputs.
3, 7	V_{REF_AC0}, V_{REF_AC1}	Output		Reference voltage for AC-coupled applications.
4, 8	nIN0, nIN1	Input		Inverting differential LVPECL clock inputs. RT = 50Ω termination to V_T.
9, 17, 24, 32	V_{EE}	Power		Negative supply pins.
10	nc			No connect pin.
11, 16, 18, 23, 25, 30	V_{CC}	Power		Positive supply pins.
12, 13	nQ5, Q5	Output		Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ4, Q4	Output		Differential output pair. LVPECL/ECL interface levels.
19, 20	nQ3, Q3	Output		Differential output pair. LVPECL/ECL interface levels.
21, 22	nQ2, Q2	Output		Differential output pair. LVPECL/ECL interface levels.
26, 27	nQ1, Q1	Output		Differential output pair. LVPECL/ECL interface levels.
28, 29	nQ0, Q0	Output		Differential output pair. LVPECL/ECL interface levels.
31	SEL	Input	Pullup	Input select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3. SEL Function Table

SEL	Function
0	IN0/nIN0 input selected
1	IN/nIN1 input selected (default)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	42.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.6	V
I_{EE}	Power Supply Current			72		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.375V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{CC} = 3.6V	2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.6V	-0.3		0.8	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.6V	-125		20	µA
I_{IL}	Input Low Current	V_{CC} = 3.6V, V_{IN} = 0V			-300	uA

.

Table 4C. Differential DC Characteristics, V_{CC} = 2.375V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	IN0/ nIN0, IN1/nIN1			100		Ω
V_{IH}	Input High Voltage	IN0/ nIN0, IN1/nIN1		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	IN0/ nIN0, IN1/nIN1		0		V_{CC} – 0.15	V
V_{IN}	Input Voltage Swing			0.15		2.8	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_{IN}	Input Current	IN0/ nIN0, IN1/nIN1				45	mA
V_{REF_AC}	Bias Voltage				V_{CC} – 1.35		V

Table 4D. LVPECL DC Characteristics, V_{CC} = 2.375V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE1			V_{CC} – 1.005		V
V_{OL}	Output Low Voltage; NOTE 1			V_{CC} – 1.78		V
V_{OUT}	Output Voltage Swing			800		mV
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Input and output terminations vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V

AC Electrical Characteristics

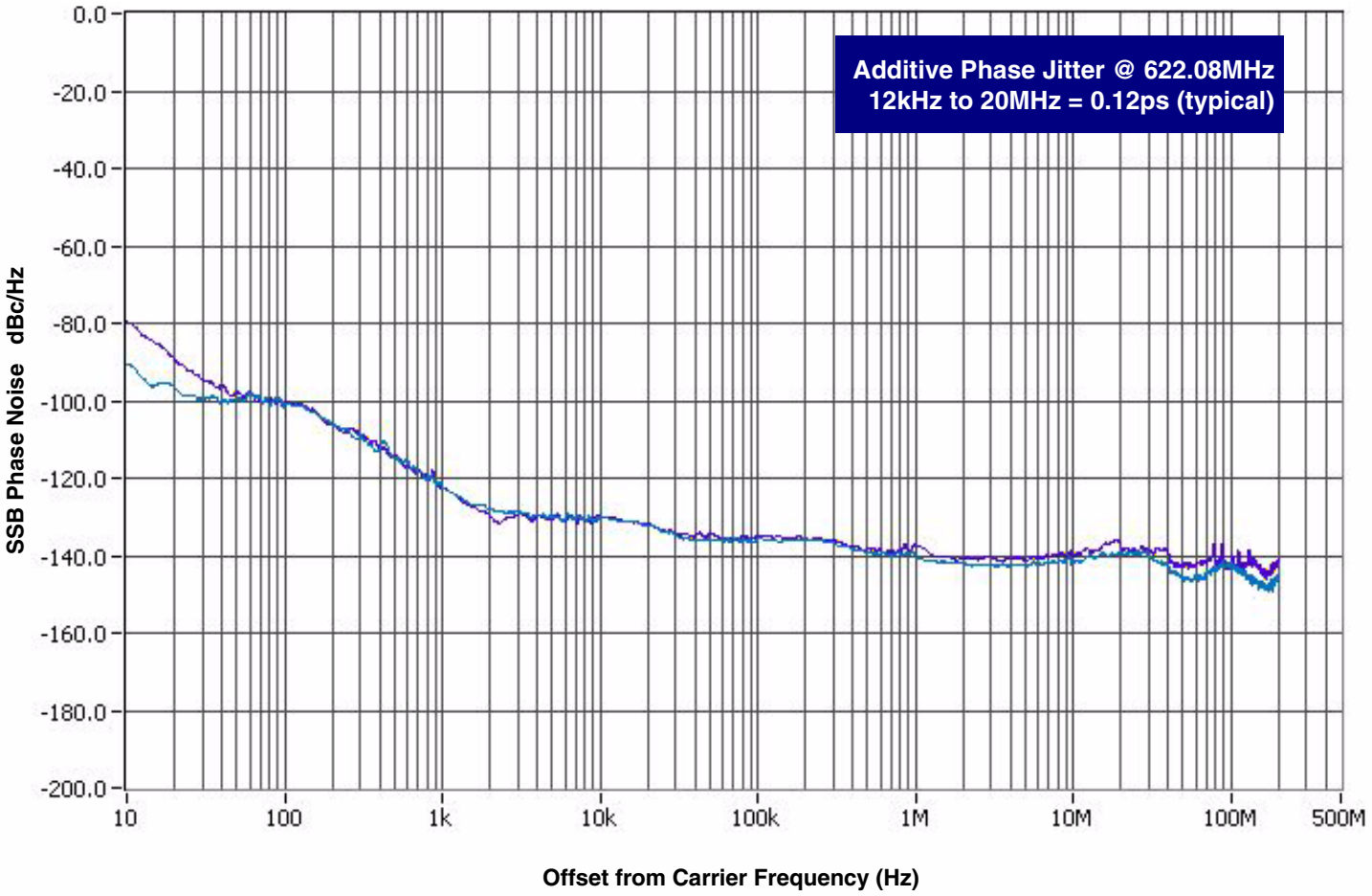
Table 5. AC Characteristics, V_{CC} = 2.375V to 3.6V, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					3.2	GHz
t_{PD}	Propagation Delay; NOTE 1	INx to Qx			700		ps
tsk(o)	Output Skew; NOTE 2, 4				15		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4						ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section		622.08MHz, Integration Range: 12kHz to 20MHz		0.12		ps
t_R / t_F	Output Rise/Fall Time		20% - 80%		150		ps

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

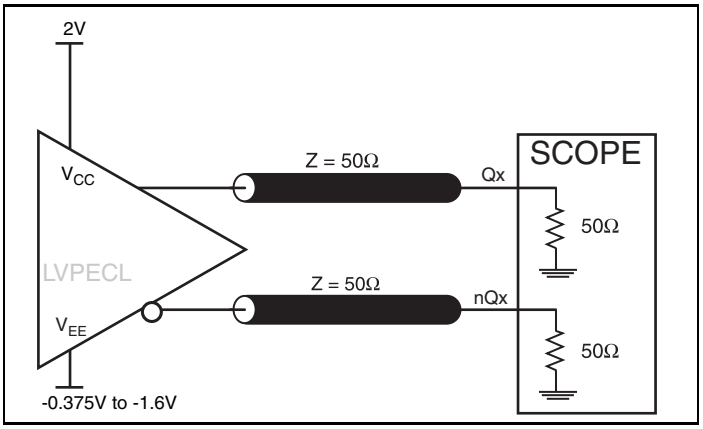
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

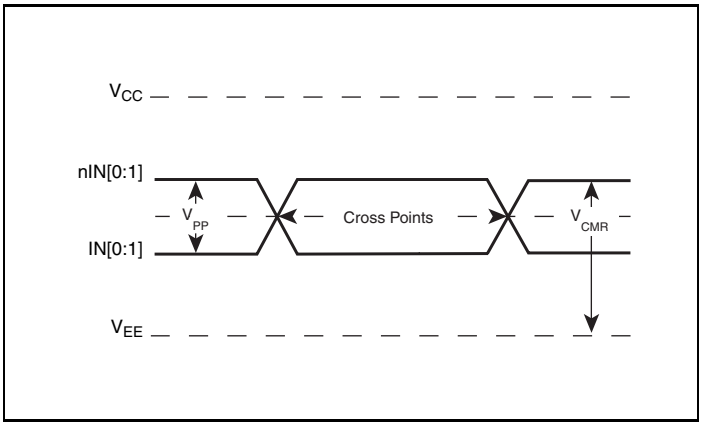


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

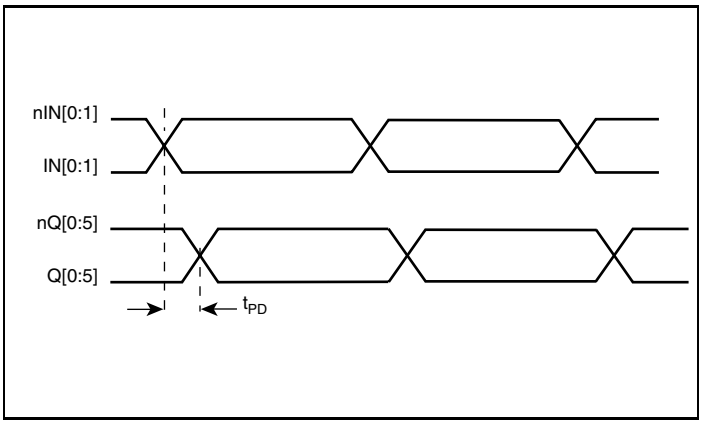
Parameter Measurement Information



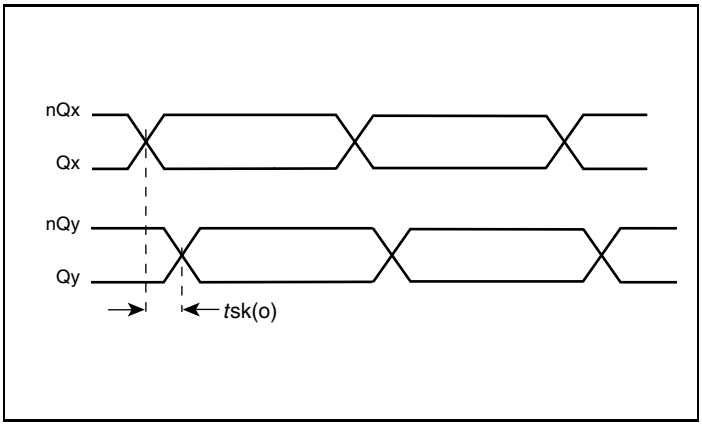
Output Load AC Test Circuit



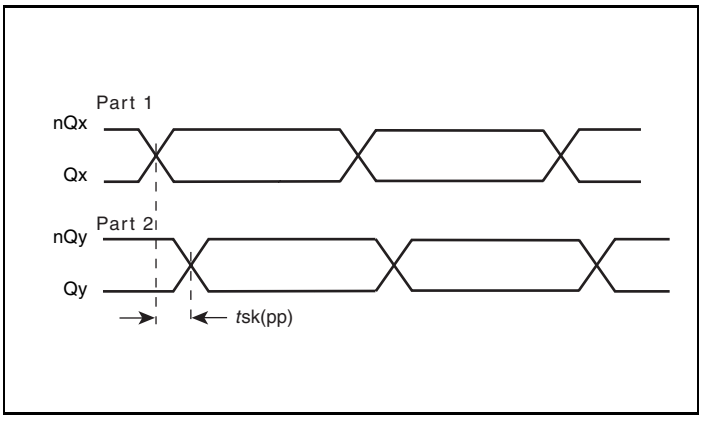
Differential Input Level



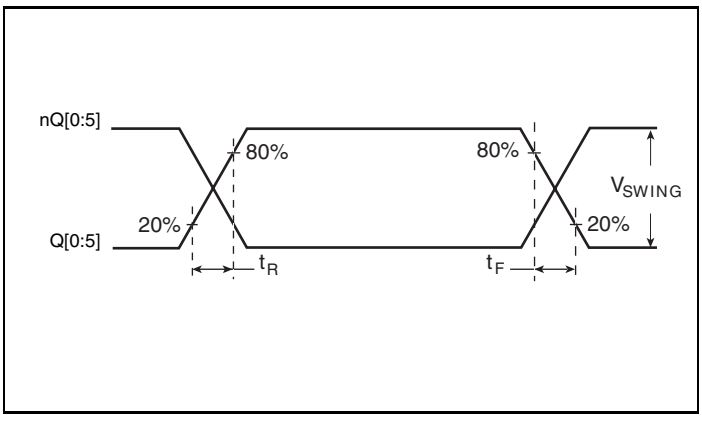
Propagation Delay



Output Skew



Part-to-Part Skew



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

IN/nIN Inputs

For applications not requiring the use of the differential input, both IN and nIN can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from IN to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{cc}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{cc} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

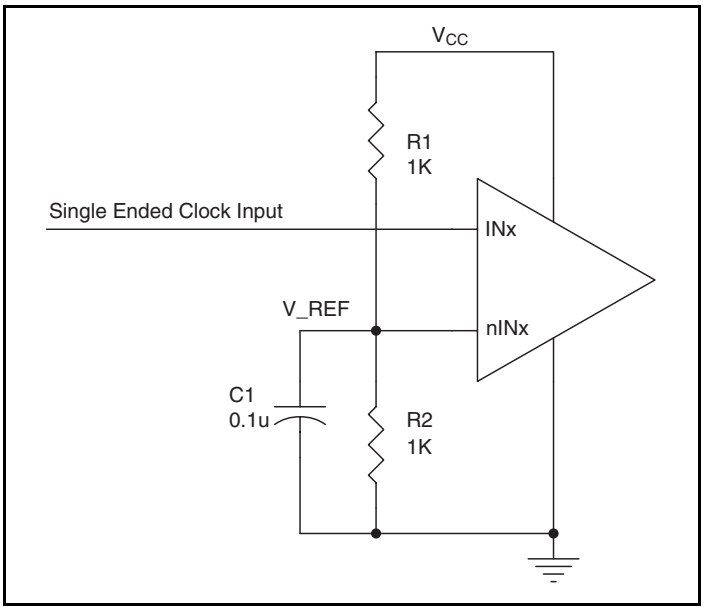


Figure 1. Single-Ended Signal Driving Differential Input

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

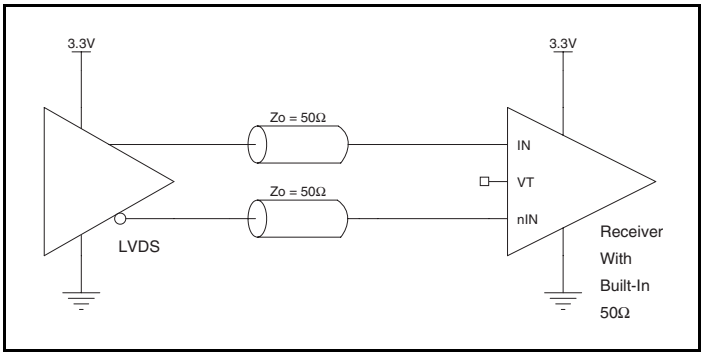


Figure 2A. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

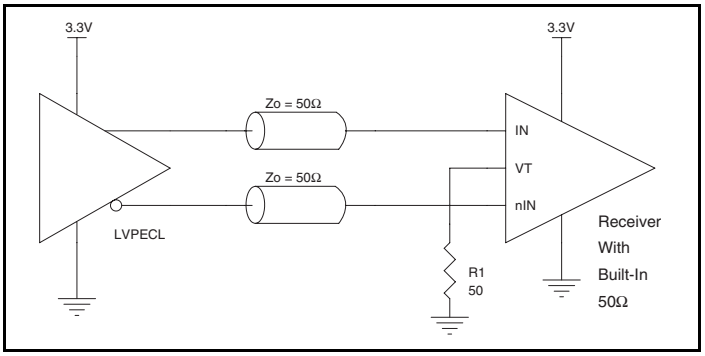


Figure 2B. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

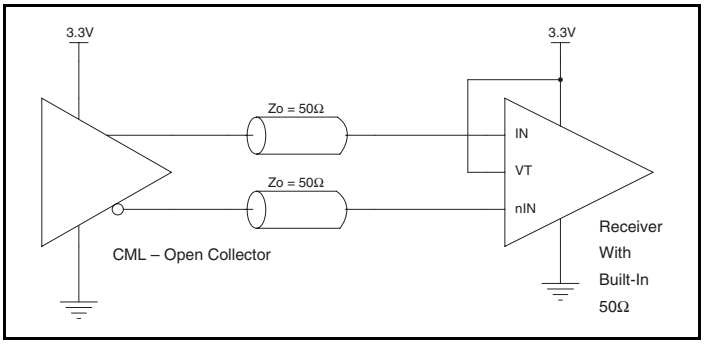


Figure 2C. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

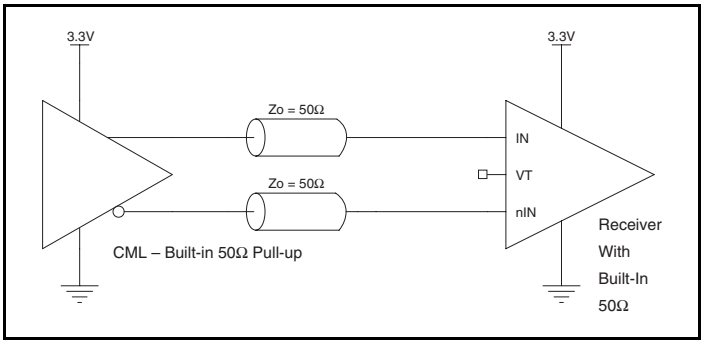


Figure 2D. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

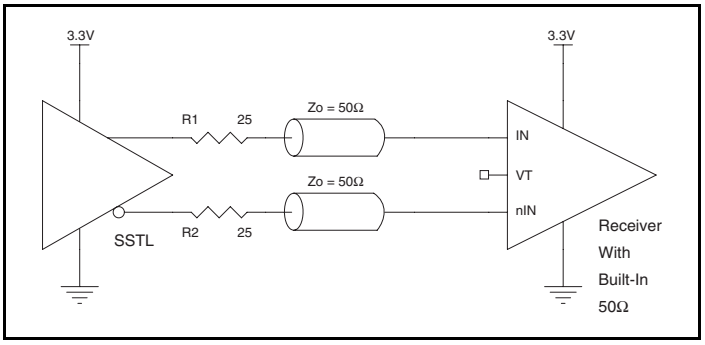


Figure 2E. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML, SSTL and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

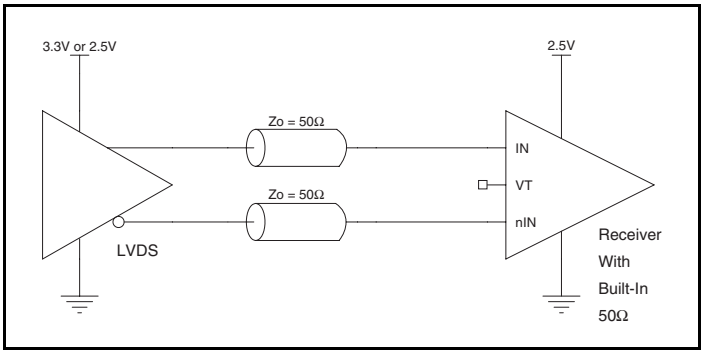


Figure 3A. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

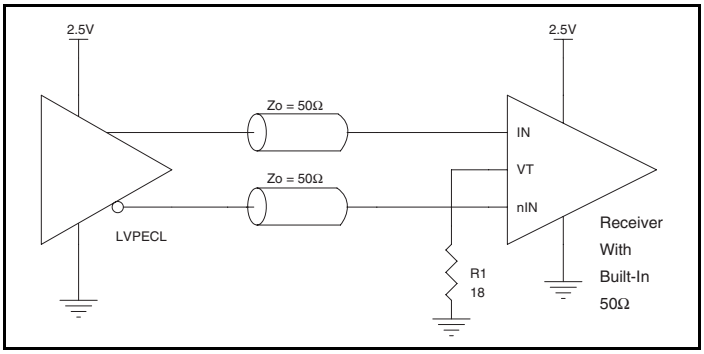


Figure 3B. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

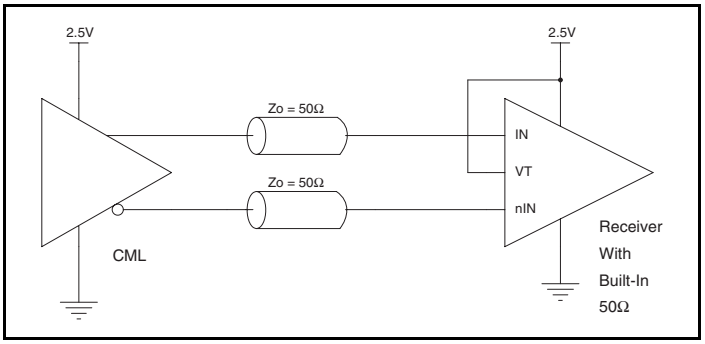


Figure 3C. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

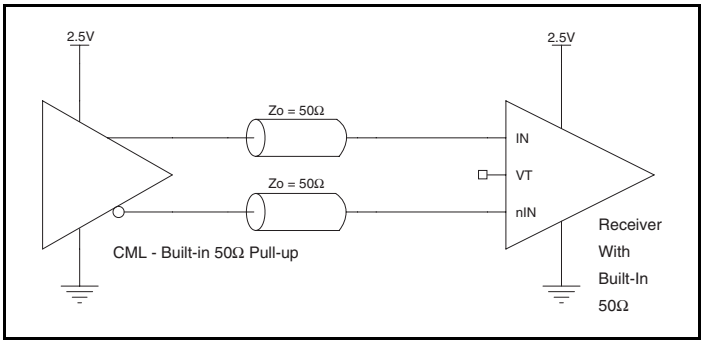


Figure 3D. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

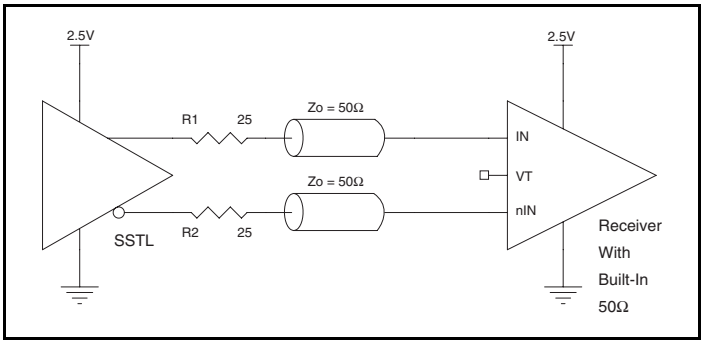


Figure 3E. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

2.5V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 4A.*

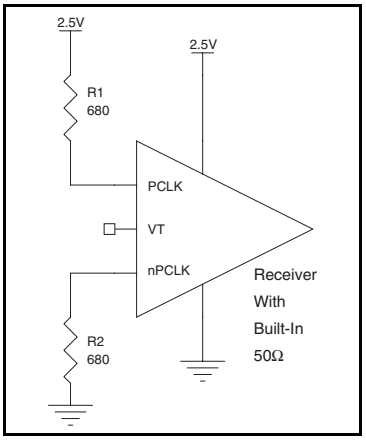


Figure 4A. Unused Input Handling

3.3V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 4B.*

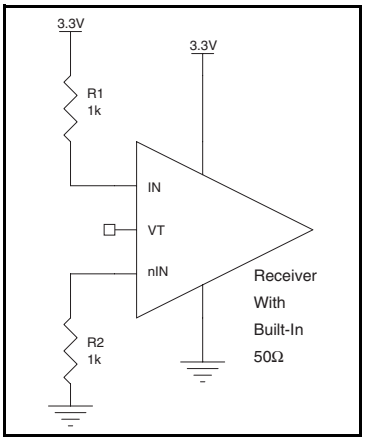


Figure 4B. Unused Input Handling

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

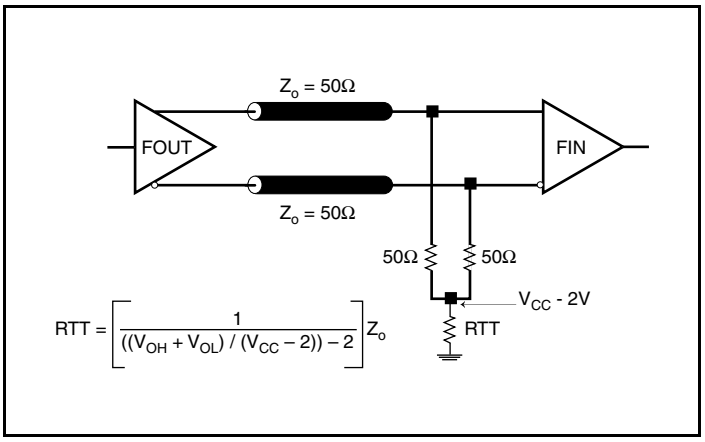


Figure 5A. 3.3V LVPECL Output Termination

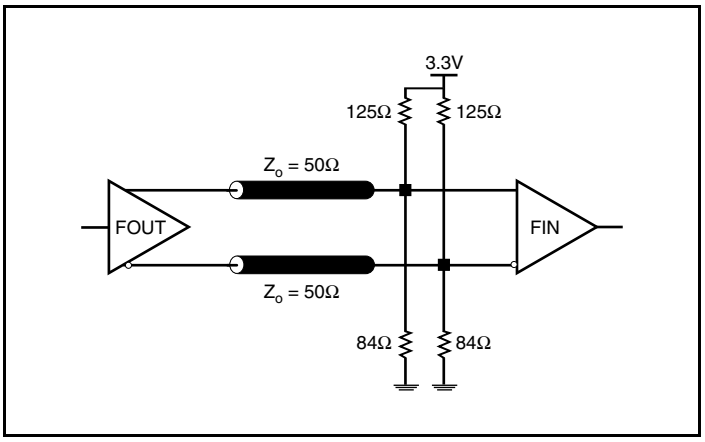


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

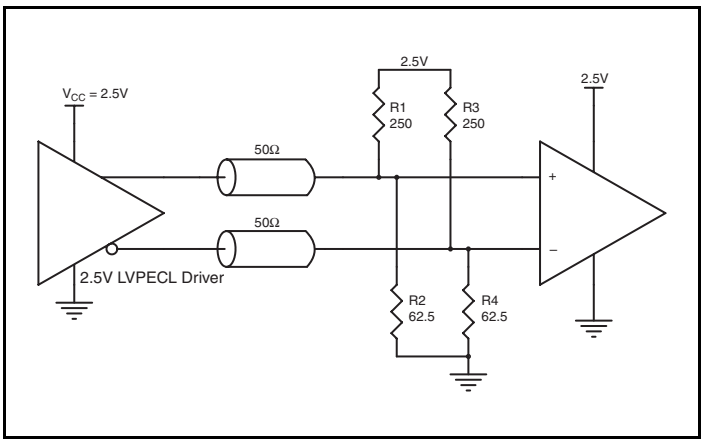


Figure 6A. 2.5V LVPECL Driver Termination Example

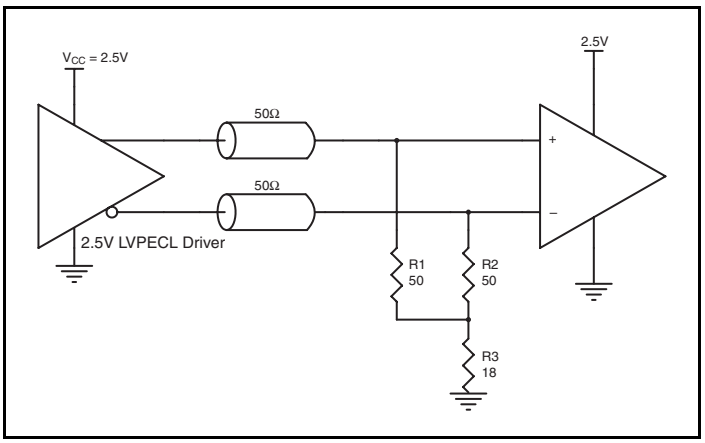


Figure 6B. 2.5V LVPECL Driver Termination Example

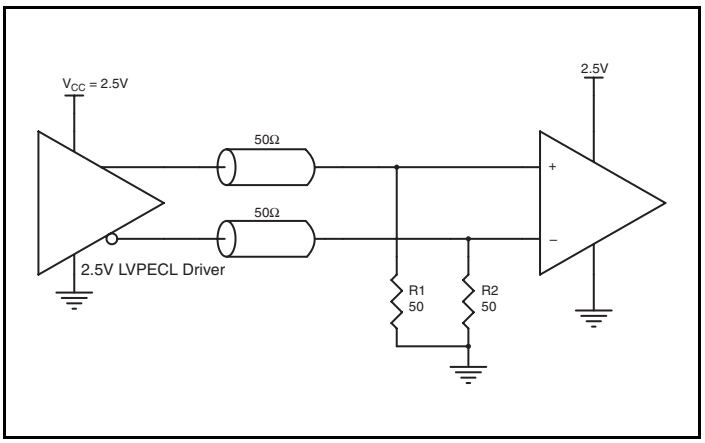


Figure 6C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

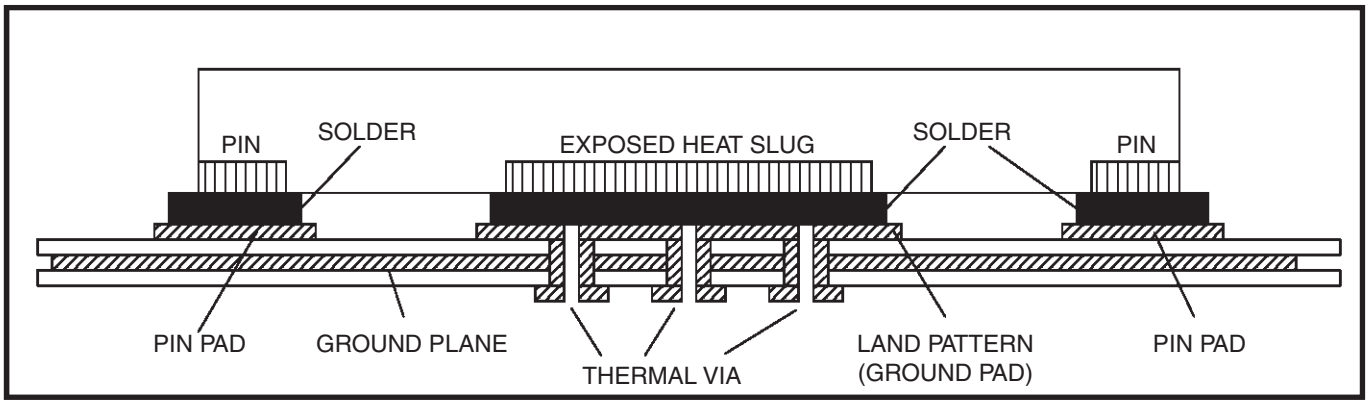


Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8S58035I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8S58035I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.6V * 72mA = **259.2mW**
- Power $(outputs)_{MAX}$ = **27.83mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 27.83mW = **166.98mW**

Total Power$_{\_MAX}$ (3.6V, with all outputs switching) = 259.2mW + 166.98mW = **426.18mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.426W * 42.7°C/W = 103.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 6. Thermal Resistance θ_{JA} for 48 Lead TQFP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

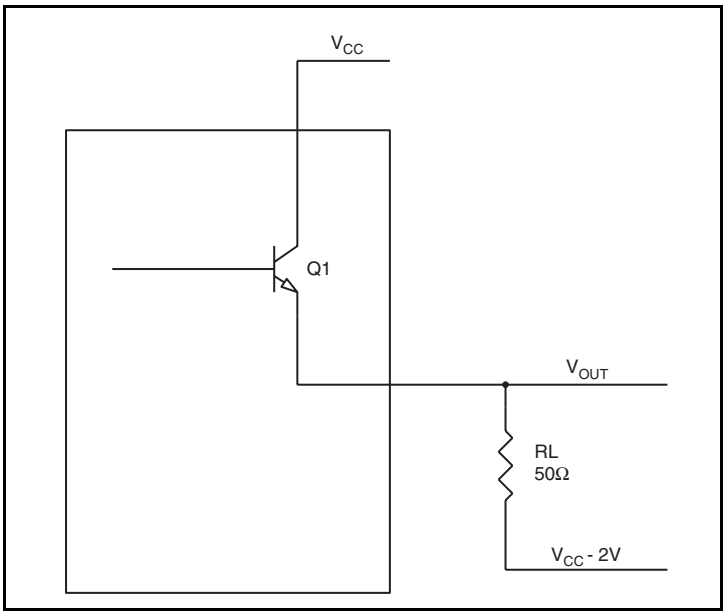


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CC_MAX} – 1.005V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **1.005V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CC_MAX} – 1.78V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.78V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 1.005V)/50Ω] * 1.005V =$ **20mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.78V)/50Ω] * 1.78V =$ **7.83mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.83mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

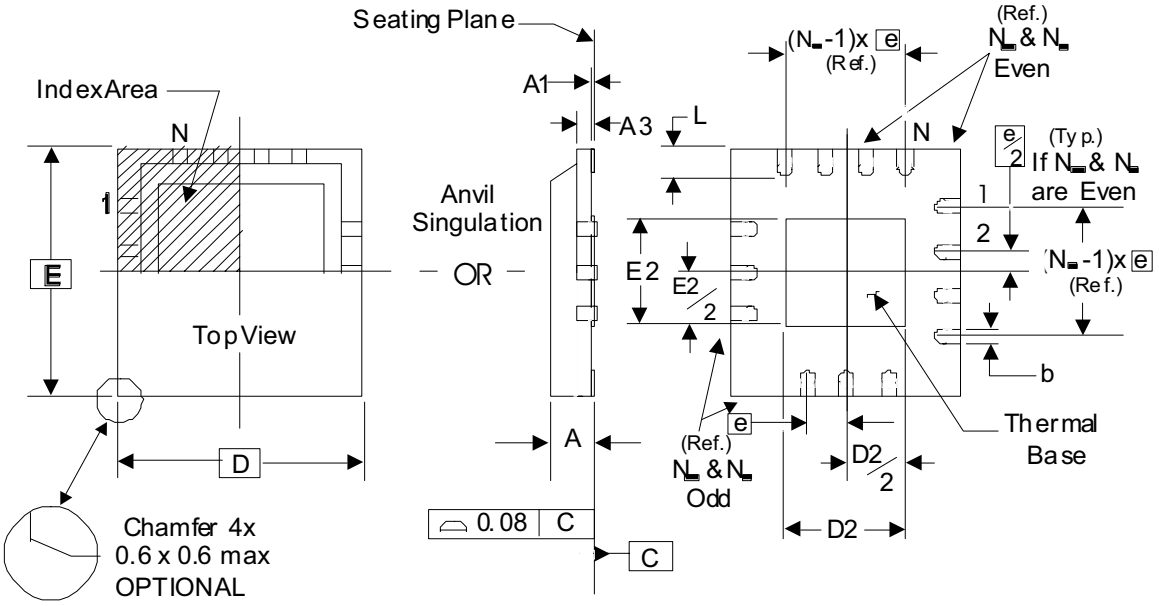
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Transistor Count

The transistor count for ICS8S58035I: 348

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S58035AKILF	ICS58035AIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8S58035AKILFT	ICS58035AIL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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