ATP Industrial Grade CFast Card Specification

Revision 1.1

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Revision History

Date	Version	Changes compared to previous issue
Mar.22nd, 2012	0.1	- Preliminary version
Mar.28th, 2012	0.2	- Update S.M.A.R.T. tool screenshot
May 31st, 2012	1.0	- Official released version
Jul. 5th, 2012	1.1	- Add TBW Sequential write information - Add NCQ/TRIM Command information

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1 ATP Industrial Grade CFast Card Overview

1.1 ATP Product Availability

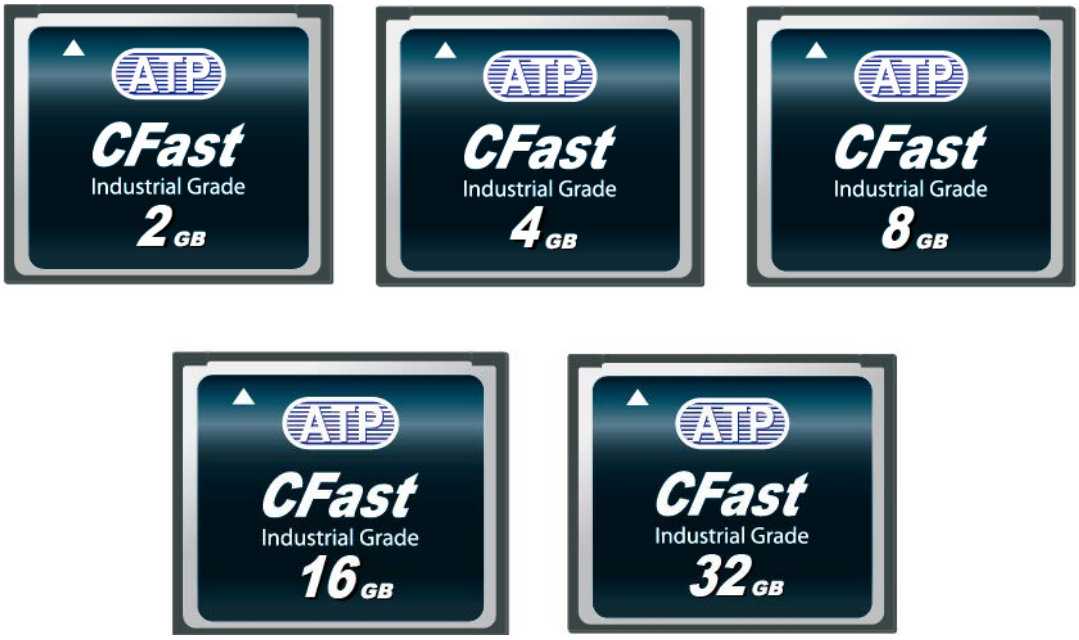


Figure 1-1: ATP Product Availability

Table 1-1: Capacities

ATP P/N	CAPACITY
AF2GCSI-OAAXP	2GB
AF4GCSI-OAAXP	4GB
AF8GCSI-OAAXP	8GB
AF16GCSI-OAAXP	16GB
AF32GCSI-OAAXP	32GB

Note: ” P” stands for PowerProtector feature

1.2 Introduction

With a form factor similar to CompactFlash card and a faster and more advanced SATA interface, ATP Industrial Grade CFast card is the ideal replacement of CompactFlash card. ATP Industrial Grade CFast card is fully compliant with CFA CFast specification version 1.1 with a SATA 3Gb/s interface. The CFast card contains a 24-pin connector consisting of a SATA compatible 7-pin signal connector and a 17-pin power and control connector. Compared to traditional CompactFlash card with ATA/IDE interface, ATP CFast card features high-speed data transfer capability of up to 142MB/s read speed, and a 112MB/s write speed.

By utilizing SLC NAND flash memory and Global Wear Leveling technology, the ATP Industrial Grade CFast cards have enhanced endurance levels and longer product life spans. The produce line implements ECC (Error Correction Code) and StaticDataRefresh technologies, which correct and monitor the error bit levels to ensure data integrity.

Incorporating the S.M.A.R.T. (Self-Monitoring, Analysis, and Reporting Technology) function, users are able to monitor various parameters of endurance and reliability. This information helps to predict storage failure with preventative action.

ATP PowerProtector technology guarantees reliable controller and lasting NAND flash operation with a back power circuit during a power outage. The standalone design of PowerProtector ensures a sufficient amount of backup power during any power abnormalities such as unstable voltages.

1.3 Application

The new CFast specification, a combination of CF and ATA serial Transport (AST), is recommended as new boot and storage device in embedded and industrial markets. These markets include military/aerospace, automation, marine navigation, embedded system, telecommunication equipment/ networking and medical equipment where mission-critical data requires the highest level of reliability, durability, and data integrity.

1.4 Main Features

- **Single-Level-Cell (SLC) NAND Flash**
- **Host Interface:**
  - Compliant with SATA Specification 2.6 and CFast Specification 1.1
  - SATA 3.0Gb/s interface
  - 24-pin connector: 7-pin signal connector and 17-pin power and control connector
- **High performance:**
  - Sequential read up to 142MB/s
  - Sequential write up to 112MB/s
  - Capacity: 2GB to 32GB
- **Industrial grade operating temp.**: -40^{o}C to 85^{o}C
- **Endurance:**
  - Enhanced endurance by Global Wear Leveling algorithm and bad block management
  - BCH-ECC engine can correct up to 40 bit errors per 1,024 Bytes data
  - TBW (Total Bytes Written): up to 640 Terabyte random write (32GB CFast card)
- **StaticDataRefresh technology to ensure data integrity in read operations.**
- **ATP PowerProtector, built-in hardware power-down data protection**
- **S.M.A.R.T. function support for life time monitor**
- **Support NCQ/TRIM command (require OS/HW/Driver support)**

2 Product Specification

2.1 Supply Voltage

Table 2.1 Supply Voltage

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.15	3.3	3.45	V

2.2 Current Consumption

Table 2.2 Current Consumption

Current Consumption	3.3V	Unit
Read (typ/max)	270 / 310	mA
Write (typ/max)	330 / 410	mA
Idle	194	mA

Note: The value is measured based on 32GByte CFast card at 25°C and normal supply voltage. The consumption of each CFast card may be different and the maximum value is for reference purpose.

2.3 Environment Specification

Table 2-3: Environment Specification

TYPE		MEASUREMENT
Temperature	Operation	-40°C to +85°C
	Non-Operation	-40°C to +85°C
Humidity	Storage	+40ºC, 93% RH / 500hrs +85ºC, 85% RH / 1000hrs
Random Vibration Test (JESD22-B103)	Non-Operation	20G Peak, 20~2000Hz
Shock Test (JESD22-B110)	Non-Operation	1500G, 0.5ms duration, half sine wave
UV Light Exposure Test (ISO 7816-1)	Non-Operation	254nm, 15Ws/cm2
Drop Test	Non-Operation	120cm/Free fall/9 times
ESD (IEC 61000-4-2)	Non-Operation	non-contact pad (Coupling plane discharge) +/- 8KV non-contact pad (Air discharge) +/- 15KV

2.4 Reliability

Table 2-4: Reliability

Type	Measurement	
Number of insertions	10,000 minimum	
Endurance	Global Wear Leveling algorithm SLC block endurance: 100,000 P/E cycles	
CFast Endurance TBW (Total Bytes Written)	2GB	40 terabyte random write 80 terabyte sequential write
	4GB	80 terabyte random write 160 terabyte sequential write
	8GB	160 terabyte random write 320 terabyte sequential write
	16GB	320 terabyte random write 640 terabyte sequential
	32GB	640 terabyte random write 1,280 terabyte sequential write
MTBF (25℃)	>5,000,000 hours	

Note: Endurance for flash products can be predicted based on the usage conditions applied to the device, the internal NAND flash cycles, the write amplification factor, and the wear leveling efficiency of the flash devices.

2.5 CFast Card Capacity

Table 2-5: CFast Card Capacity

Product Capacity	LBA (Sectors)	Physical Capacity (Bytes)
2GB	3864576	1,978,195,968
4GB	7839744	4,013,678,592
8GB	15458304	7,914,332,160
16GB	30916608	15,829,303,296
32GB	61849600	31,666,995,200

2.6 Performance

2.6.1 IOPS

Table 2-61: IOPS

Type	Value
4K Random Read IOPS (32GB)	4,609 IOPS

Notes: IOPS: Input / Output Operations per Second

2.6.2 Read/Write Performance

Table 2-62: Read/Write Performance

Model P/N	Seq. Read (KB/s)	Seq. Write (KB/s)	Random Read (KB/s)	Random Write (KB/s)
AF2GCSI-OAAXP	31950	14808	30117	6361
AF4GCSI-OAAXP	63900	30095	56888	9426
AF8GCSI-OAAXP	127601	69861	90319	13865
AF16GCSI-OAAXP	137912	113777	93515	18584
AF32GCSI-OAAXP	141485	111455	90319	18980

Note: Tested by HDBench 3.40 beta6 with 40MB file size. The performance may vary based on different testing environments.

2.7 Certification and compliance

Table 2-7: Certification table

Mark/Approval	Documentation	Certification
	The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French.	Yes
	FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15	Yes
	RoHS is the acronym for Restriction of Hazardous Substances. RoHS, also known as Directive 2002/95/EC, originated in the European Union and restricts the use of specific hazardous materials found in electrical and electronic products. All applicable products in the EU market after July 1, 2006 must pass RoHS compliance. For the complete directive, see Directive 2002/95/EC of the European Parliament.	Yes

2.8 Global Wear Leveling- Longer Life Expectancy

The program / erase cycle of each sector/page/block is finite. Writing constantly on the same spot will cause the flash to wear out quickly. Furthermore, bit errors are not proportioned to P/E cycles; sudden death may occur when the block is close to its P/E cycle limit. Then unrecoverable bit errors will cause fatal data loss (especially for system data or FAT).

Global Wear Leveling algorithm evenly distributes the P/E cycles of each block to minimize the possibility of one block exceeding its max P/E cycles before the rest. In return, the life expectancy of memory storage device is prolonged and the chance/occurrence of unrecoverable bit errors could be reduced.

2.9 SaticDataRefresh Technology – Ensure Data Integrity

Over time the error bits accumulate to the threshold in the flash memory cell and eventually become uncorrectable despite using the ECC engine. In the traditional handling method, the data is moved to a different location in the flash memory; despite the corrupted data is beyond repaired before the transition.

To prevent data corruption, ATP Industrial Grade CFast card monitors the error bit levels in each read operation. When it reaches the preset threshold value, StaticDataRefresh is activated by erasing and re-programming the data into another block. After the re-programming operation is completed, the controller reads the data and compares the data/parity to ensure data integrity.

2.10 ATP PowerProtector – Built-in Power Failure Data Protection

ATP PowerProtector technology ensures a sufficient amount of reserve power during any power abnormalities such as unstable voltages and power outages. PowerProtector's patent pending technology is a stand alone hardware design that does not require specific controllers or customized firmware. This feature provides greater flexibility during the design of a smaller form factor such as CFast cards.

During a sudden power failure, the drive then draws power from PowerProtector's solid state capacitors for reserve power, which guarantees reliable drive operations. The solid state capacitors allow the flash to finish processing the last command or data.

SuperCap, the traditional power protection design, is well known for its sensitivity to temperature change and has a tendency of losing its capacitance and functionality at extreme temperatures. The average life span of SuperCap is less than two years; the capacitance will degrade over time and eventually fail to perform.

ATP PowerProtector surpasses the natural limitations of SuperCap designs by supporting wide temperature and an average life span of over five years without capacitance degradation. PowerProtector offers an advanced level of protection ensuring that data integrity is not compromised during a power failure scenario, and preserves critical data in mission critical applications.

2.11 NCQ/TRIM Command Support

NCQ (Native Command Queuing) is to optimize the order in which received read and write commands are executed. Under certain circumstances, it could enhance performance up to 30%.

TRIM command is to allow an operating system to inform a SATA device which blocks of data are no longer considered in use and can be wiped internally. The result is the SATA device will have more free space enabling lower write amplification and higher performance. It enables garbage collection, which prevents performance from slowing down due to invalid blocks after using for a period of time.

NCQ and TRIM command require OS/HW/Driver support from host device.

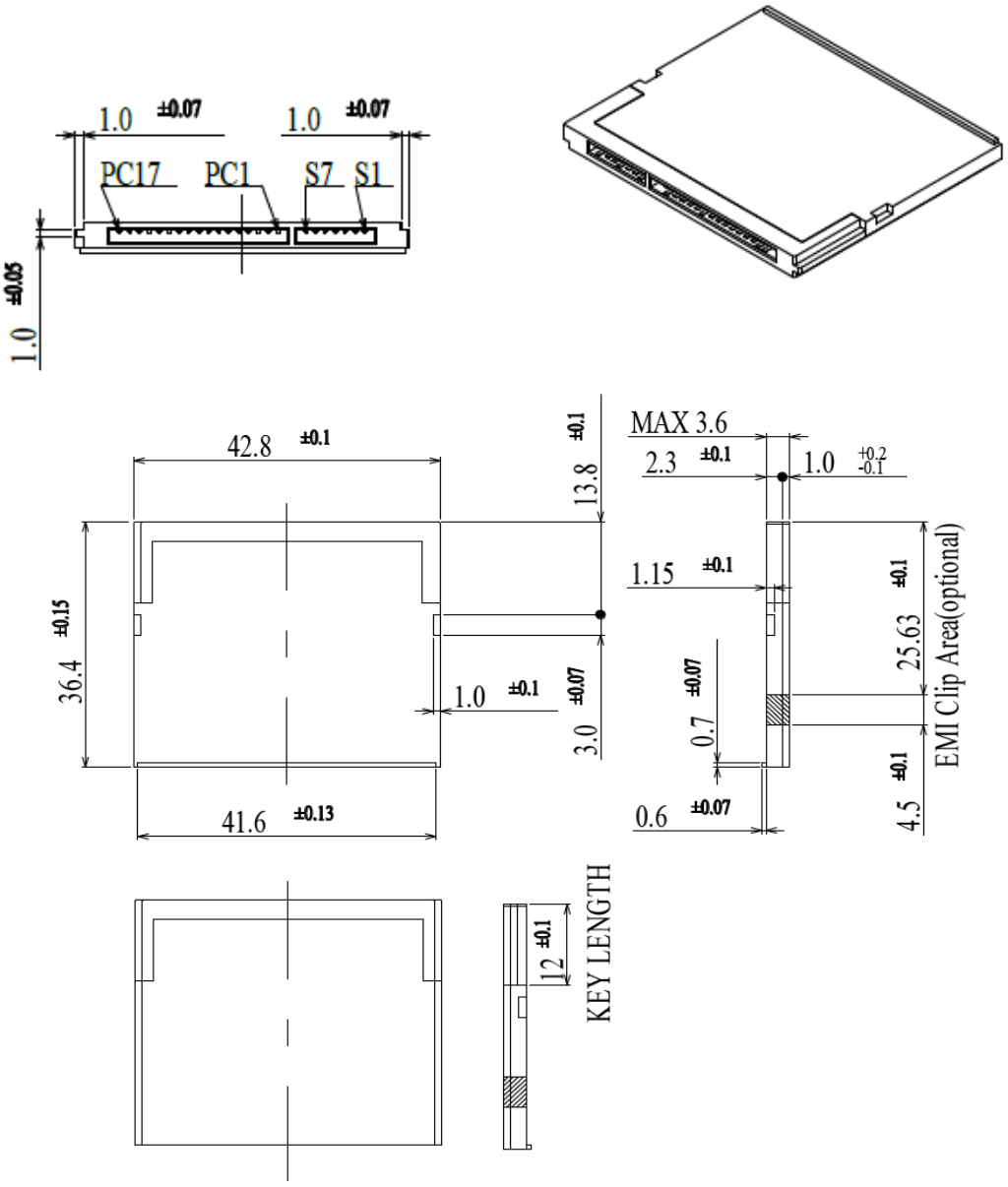
2.12 Physical Dimension Specification

Table 2-12: Physical Specifications

Type		Measurement
Type I	Length	36.4 ± 0.15 mm
	Width	42.80 ± 0.10 mm
	Thickness	3.6 mm maximum
	Weight	9.0 g typical

2.13 Mechanical Form Factor (Units in MM)

Figure 2-13: ATP CFast Physical Dimensions



3 Electrical Interface

3.1 Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 3-1: Pin Assignments and Pin Type

Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Section 3.3 defines the DC characteristics for all input and output type structures.

Table 3-1: Pin Assignments and Pin Type

Number	Segment	Name	Type	Description	Mate Sequence
S1	SATA	SGND	Signal GND	Ground for signal integrity	1st
S2	SATA	A+	SATA Differential	Signal Pair A	2nd
S3	SATA	A-	SATA Differential		2nd
S4	SATA	SGND	Signal GND	Ground for signal integrity	1st
S5	SATA	B-	SATA Differential	Signal Pair B	2nd
S6	SATA	B+	SATA Differential		2nd
S7	SATA	SGND	Signal GND	Ground for signal integrity	1st
	Key				
	Key				
PC1	PWR/CTL	CDI	CMOS Input	Card Detect In	3rd
PC2	PWR/CTL	GND	Device GND		1st
PC3	PWR/CTL	TBD	TBD		2nd
PC4	PWR/CTL	TBD	TBD		2nd
PC5	PWR/CTL	TBD	TBD		2nd
PC6	PWR/CTL	TBD	TBD		2nd
PC7	PWR/CTL	GND	Device GND		1st
PC8	PWR/CTL	LED1	LED Output	LED Output	2nd
PC9	PWR/CTL	LED2	LED Output	LED Output	2nd
PC10	PWR/CTL	IO1	CMOS Input/Output	Reserved Input/Output	2nd
PC11	PWR/CTL	IO2	CMOS Input/Output	Reserved Input/Output	2nd
PC12	PWR/CTL	IO3	CMOS Input/Output	Reserved Input/Output	2nd
PC13	PWR/CTL	PWR	3.3V	Device Power (3.3V)	2nd
PC14	PWR/CTL	PWR	3.3V	Device Power (3.3V)	2nd
PC15	PWR/CTL	PGND	Device GND	Device Ground	1st
PC16	PWR/CTL	PGND	Device GND	Device Ground	1st
PC17	PWR/CTL	CDO	CMOS Output	Card Detect Out	3rd

3.2 Electrical Description

Table 3-2: Signal Description describes the I/O signals. Signals whose source is in the host are designated as inputs while signals that the CFast Card sources are outputs.

Table 3-2: Signal Description

Description of SATA Segment Pins

NAME	TYPE	DESCRIPTION
SGND	Signal Ground	These are intended to provide isolation for the high speed differential signals.
A+, A-, B+, B-	SATA Differential	The functionality and electrical characteristics of these pins are defined in the **SATA** reference

Description of PWR/CTL Segment Pins

NAME	TYPE	DESCRIPTION
CDI	CMOS Input	This signal is driven by the CFast host, and shall be sampled by the CFast device This pin shall be shorted on a CFast device to CDO. This signal and CDO provide a mechanism for a CFast host to detect that a CFast device has been fully inserted, and so that power can be applied safely. The host may drive, and the device may sample, this pin to provide signaling to enable CFast Power Management Sleep state.
CDO	CMOS Output	This pin shall be shorted on the CFast device to CDI. It is effectively driven by CDI.
LED1	LED Output	LED Output
LED2	LED Output	LED Output
IO1	CMOS Input/Output	Unassigned Input/Output pin
IO2	CMOS Input/Output	Unassigned Input/Output pin
IO3	CMOS Input/Output	Unassigned Input/Output pin

3.3 Electrical Specification

The tables in this section define all D.C. Characteristics for the CFast Card Series. Unless otherwise stated, conditions are:

Vcc = 3.3V ±5%

Ta = -40°C to 85°C

Table 3-3: Absolute Maximum Conditions

PARAMETER	SYMBOL	CONDITIONS
Input Power	Vcc	-0.3Vmin. to 3.6Vmax.
Voltage on any pin except Vcc with respect to GND.	V	-0.5Vmin. to Vcc + 0.5Vmax.

The card does not need to operate, or to meet any operating specifications outside its operating conditions. Application of absolute maximum conditions shall not damage the card.

3.3.1 Maximum input current

Table 3-31: Maximum Input Current

POWER LEVEL	Voltage Temperature During Test	Average Current Range (Active)	Average Current Range (Partial)	Average Current Range (Slumber)	Average Current Range (PHYSLP)
0	3.3V±1% at 23°C±1°C	0 – 500mA	0 – 500mA	0-250mA	0-20mA
1	3.3V±1% at 23°C±1°C	0 – 1200mA	0 – 1200mA	0-250mA	0-20mA

To comply with this specification, current requirements shall not exceed the maximum limit.

For CFast cards, two power levels are defined. Power Level 0 has a maximum average current of 500 mA, while Power Level 1 has an increased maximum current of 1200 mA for 3.3V. If the CFast card does not support the CFA Feature Set, the card shall stay within the power envelope of Power Level 1.

CFast cards shall operate within the specifications for Power Level 0 at power on and after reset. CFast cards shall also support ATA Identify Device and Set Features commands in Power Level 0. This requirement allows the host device to determine the CFast card's capabilities and which Power Levels are supported. The possibilities are:

☐ Power Level 0,

☐ Power Level 1,

☐ Power Level 0 and Power Level 1.

The host shall use the Set Features command to set the desired power level to the card if it is compatible with it, or reject the CFast card.

An example of a CFast card using both Power Level 0 and Power Level 1 is a Flash memory card supporting both Power Levels. When set by the host to Power Level 0 (default) it shall have lower performance than when it is set to Power Level 1, but shall not exceed the Power Level 0 current consumption.

4 ATA Command Description

4.1 ATA Command Set

Table 4-1. ATA Command Set

COMMAND	CODE	FR	SC	SN	CY	DH
Check Power Mode	E5h or 98h	-	-	-	-	D
Erase Sector(s) (CFA)	C0h	Y	Y	Y	Y	-
Execute Drive Diagnostic	90h	-	-	-	-	-
Flush Cache	E7h	-	-	-	-	Y
Flush Cache Ext	EAh	-	-	-	-	Y
Identify Drive	ECh	-	-	-	-	D
Idle	E3h	-	Y	-	-	D
Idle Immediate	E1h	-	-	-	-	D
Initialize Drive Parameters	91h	-	Y	-	-	Y
Read DMA	C8h or C9h	-	Y	Y	Y	Y
Read DMA Ext	25h	-	Y	Y	Y	Y
Read FPDMA Queued	60h	Y	Y	Y	Y	Y
Read Log Ext	2Fh	Y	Y	Y	Y	Y
Read Multiple	C4h	-	Y	Y	Y	Y
Read Multiple Ext	29h	-	Y	Y	Y	Y
Read Sector(s)	20h or 21h	-	Y	Y	Y	Y
Read Sector(s) Ext	24h	-	Y	Y	Y	Y
Read Verify Sector(s)	40h or 41z	-	Y	Y	Y	Y
Read Verify Sector(s) Ext	42h	-	Y	Y	Y	Y
Recalibrate	1Xh	-	-	-	-	D
Security Disable Password	F6h	-	-	-	-	D
Security Erase Prepare	F3h	-	-	-	-	D
Security Erase Unit	F4h	-	-	-	-	D
Security Freeze Lock	F5h	-	-	-	-	D
Security Set Password	F1h	-	-	-	-	D
Security Unlock	F2h	-	-	-	-	D
Seek	7Xh	-	-	Y	Y	Y
Set Features	EFh	Y	-	-	-	D
Set Multiple Mode	C6h	-	Y	-	-	D
Set Sleep Mode	E6h	-	-	-	-	D
SMART	B0h	Y	-	-	Y	D
Stand By	E2h	-	-	-	-	D
Stand By Immediate	E0h	-	-	-	-	D
Write DMA	CAh or CBh	-	Y	Y	Y	Y
Write DMA Ext	35h	-	Y	Y	Y	Y
Write DMA FUA Ext	3Dh	-	Y	Y	Y	Y
Write FPDMA Queued	61h	Y	Y	Y	Y	Y
Write Multiple	C5h	-	Y	Y	Y	Y
Write Multiple Ext	39h	-	Y	Y	Y	Y
Write Multiple FUA Ext	CEh	-	Y	Y	Y	Y
Write Sector(s)	30h or 31h	-	Y	Y	Y	Y
Write Sector(s) Ext	34h	-	Y	Y	Y	Y

4.2 Identify Device Data

Table 4-2 Identify Device Data

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General Configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0000h	2	Obsolete
23-26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs) (Word57=LSW, Word58=MSW)
59	0100h	2	Multiple sector setting

Word Address	Default Value	Total Bytes	Data Field Type Information
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode (Word60=LSW, Word61=MSW)
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word
66	0078h	2	Recommended Multiword DMA transfer cycle time
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with lORDY flow control
69~75	0000h	20	Reserved
76	0060h	2	Serial ATA capabilities Support Serial ATA Gen1 Support Serial ATA Gen2
77~79	0000h	6	Reserved
80	0080h	2	Major version number (ATAPI-7)
81	0000h	2	Minor version number
82	742Bh	2	Command sets supported 0
83	5500h	2	Command sets supported 1
84	4002h	2	Command sets supported 2
85~87	XXXXh	6	Command set/feature enabled
88	007Fh	2	Ultra DMA supported and selected
89	0003h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	FFFEh	2	Master Pasword Revision Code
93~127	0000h	70	Reserved
128	0001h	2	Security status
129~159	0000h	62	Vendor unique bytes
160	0000h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0000h	2	CFA True lDE Timing Mode Capability and Setting
164	0000h	2	Reserved
165~175	0000h	22	Reserved
176~216	0000h	82	Reserved
217	0100h	2	Non-rotating media(SSD)
218~255	0000h	76	Reserved

5 S.M.A.R.T. Function

5.1 S.M.A.R.T. Feature

Self-monitoring analysis and reporting technology (S.M.A.R.T.) is used to protect the user from unscheduled downtime. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T. feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Informing the host system of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action.

5.2 S.M.A.R.T. Feature Register Values

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T .Function Set command. The subcommands are listed below.

Table 5-2: S.M.A.R.T. Feature Register Values

Value	Command	Value	Command
D0h	Read Data	D5h	Reserved
D1h	Read Attribute Threshold	D6h	Reserved
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

Note:

If the reserved size is below the threshold, the status can be read from the Cylinder Register using the Return Status command (DAh)

5.3 S.M.A.R.T. Data Structure

The following 512 bytes make up the device S.M.A.R.T. data structure. Users can obtain the data using the "Read Data" command (D0h).

Table 5-3: S.M.A.R.T. Data Structure

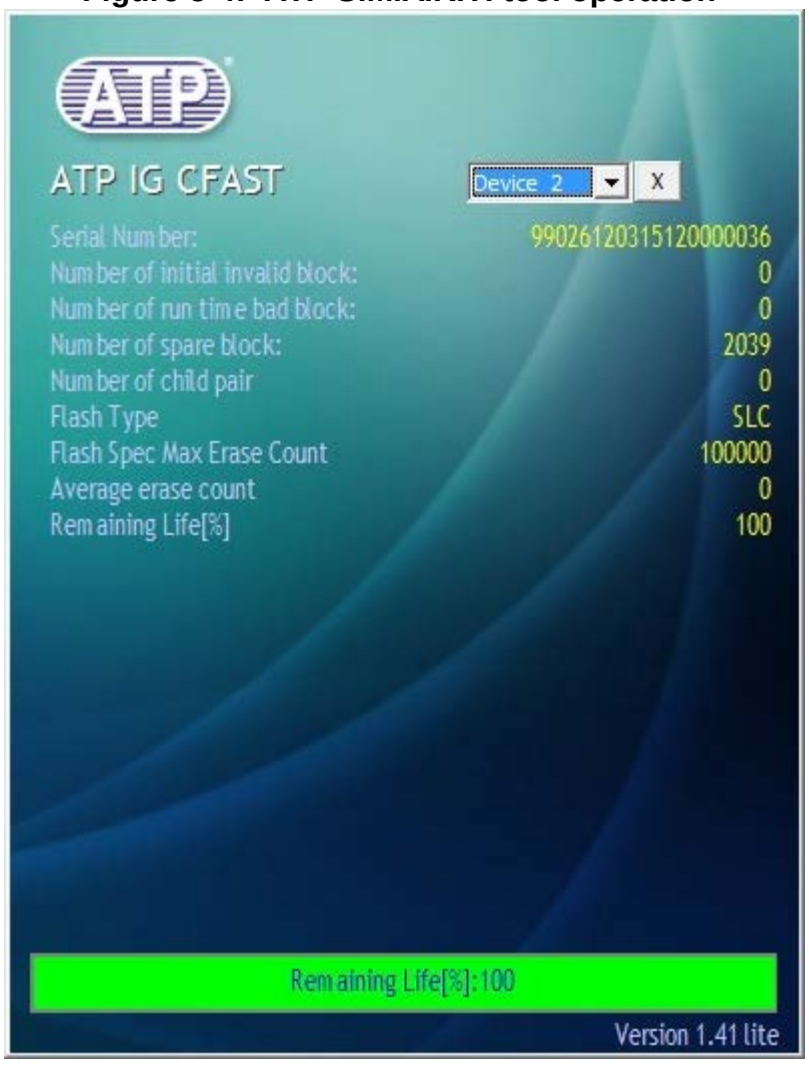
Byte	F/V	Description
0~1	X	Revision code
2~361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364~365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368~369	F	S.M.A.R.T. capability
370	F	Error logging capability：7-1 Reserved 0 1 = Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time(in minutes)
373	F	Extended self-test routine recommended polling time(in minutes)
374	F	Conveyance self-test routine recommended polling time(in minutes)
375~385	R	Reserved
386~395	F	Firmware Version/Date Code
396~397	F	Reserved
398~399	V	Reserved
400~406	F	Controller
407~415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418~419	V	Number of spare block
420~423	V	Average erase count
424~510	X	Vendor specific
511	V	Data structure checksum

Notes:
F=content (byte) is fixed and does not change
V=content (byte) is variable and maybe change depending on the state of the device or the command executed by the device
X= content (byte) is vendor specific and maybe fixed or variable
R=content (byte) is reserved and shall be zero

5.4 ATP S.M.A.R.T. Tool

ATP provides S.M.A.R.T. Tool for Windows 2000/XP/Vista/7 and Linux, It can monitor the state of Industrial Grad CFast card, and the following picture shows S.M.A.R.T. tool operation. This tool supports that users read spare and bad block information. Users can thus evaluate drive health at run time and receive an early warning before the drive life ends.

Figure 5-4: ATP S.M.A.R.T. tool operation



Note: The S.M.A.R.T. tool version will be updated from time to time. Please check with sales for the latest version.

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