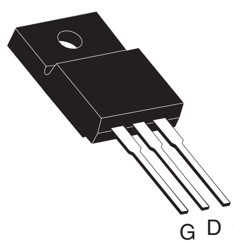
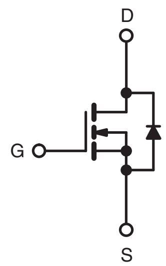
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	V_{GS} = 5.0 V	0.40
Q_g (Max.) (nC)	40	
Q_{gs} (nC)	5.5	
Q_{gd} (nC)	24	
Configuration	Single	

TO-220 FULLPAK





N-Channel MOSFET

FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS} = 4 V and 5V
- Fast Switching
- Ease of paralleling
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRLI630GPbF
	SiHLI630G-E3
SnPb	IRLI630G
	SiHLI630G

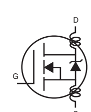
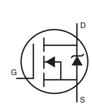
ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	200	V
Gate-Source Voltage			V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5.0 V	T_C = 25 °C	I_D	6.2	A
		T_C = 100 °C		3.9	
Pulsed Drain Current[a]			I_{DM}	25	
Linear Derating Factor				0.28	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	125	mJ
Repetitive Avalanche Current[a]			I_{AR}	6.2	A
Repetitive Avalanche Energy[a]			E_{AR}	3.5	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	35	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 2.4 mH, R_G = 25 Ω, I_{AS} = 6.2 A (see fig. 12).
c. $I_{SD} \le 9.0$ A, dI/dt ≤ 120 A/μs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.27	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 5.0 V, I_D = 3.7 A[b]	-	-	0.40	Ω
		V_{GS} =4.0 V, I_D = 3.1 A[b]	-	-	0.50	
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 5.4 A[b]	4.8	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	1100	-	pF
Output Capacitance	C_{oss}		-	220	-	
Reverse Transfer Capacitance	C_{rss}		-	70	-	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 9.0 A, V_{DS} = 160 V, see fig. 6 and 13[b]	-	-	40	nC
Gate-Source Charge	Q_{gs}		-	-	5.5	
Gate-Drain Charge	Q_{gd}		-	-	24	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 9.0 A, R_G = 6.0 Ω, R_D= 11Ω, see fig. 10[b]	-	8.0	-	ns
Rise Time	t_r		-	57	-	
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	
Fall Time	t_f		-	33	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6.2	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	25	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 6.2 A, V_{GS} = 0 V[b]	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 9.0 A, dI/dt = 100 A/µs[b]	-	230	350	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.7	2.6	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

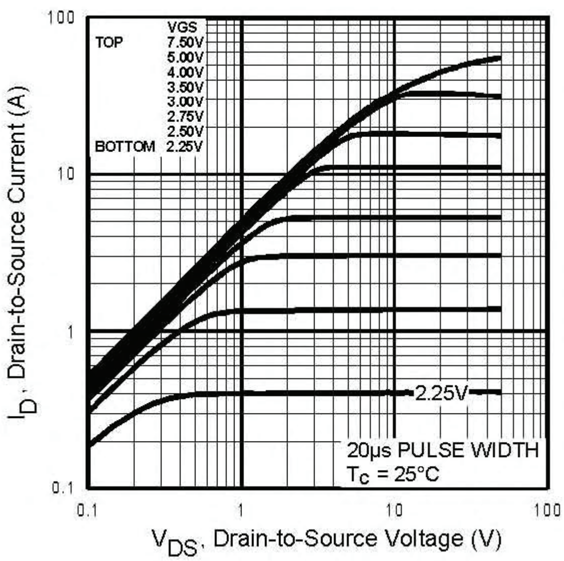


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

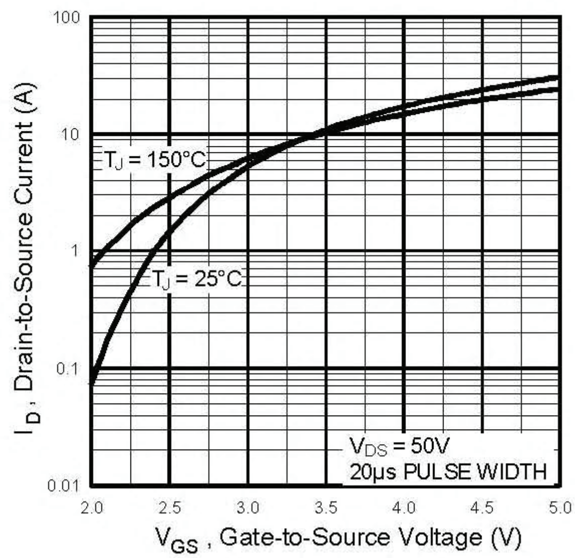


Fig. 3 - Typical Transfer Characteristics

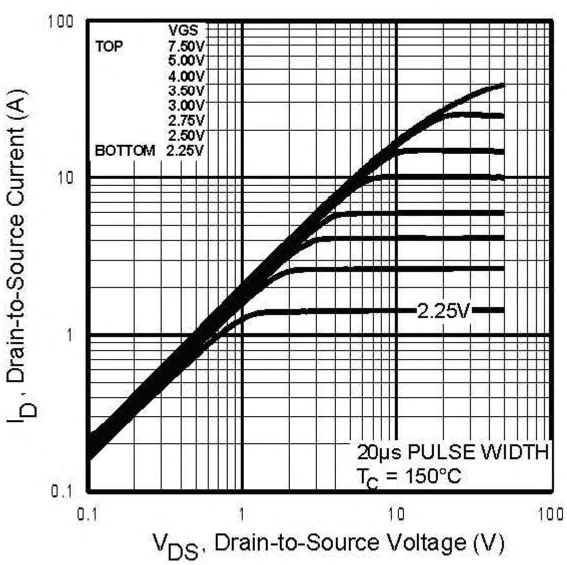


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

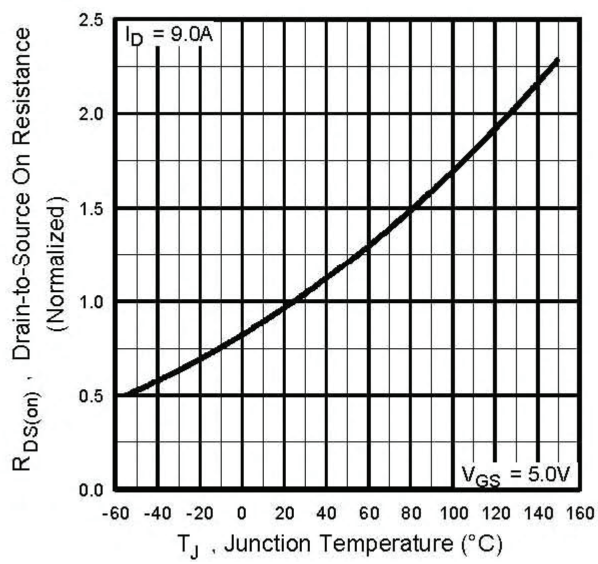


Fig. 4 - Normalized On-Resistance vs. Temperature

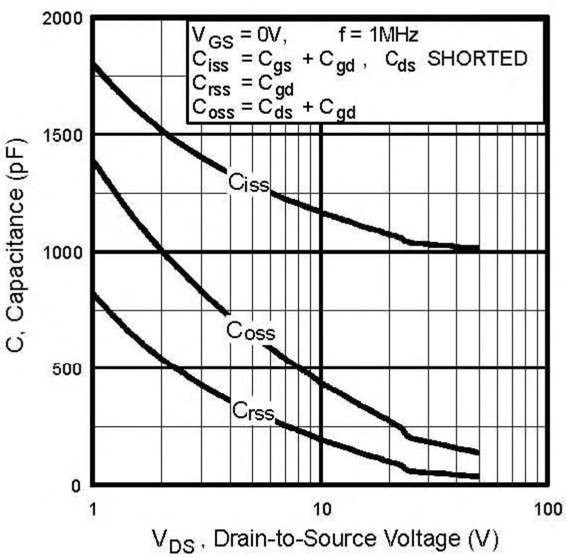


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

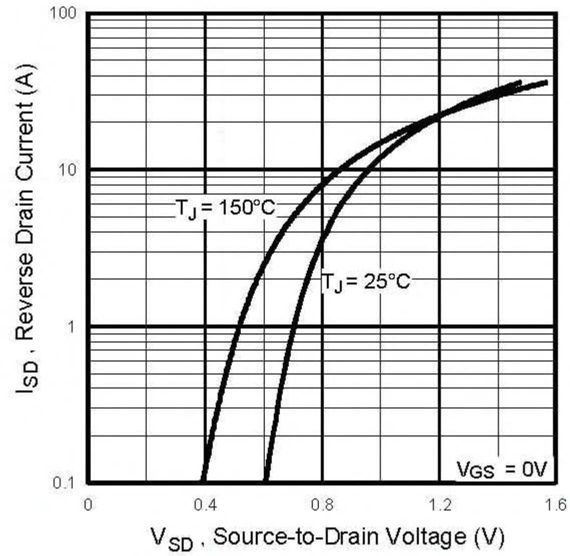


Fig. 7 - Typical Source-Drain Diode Forward Voltage

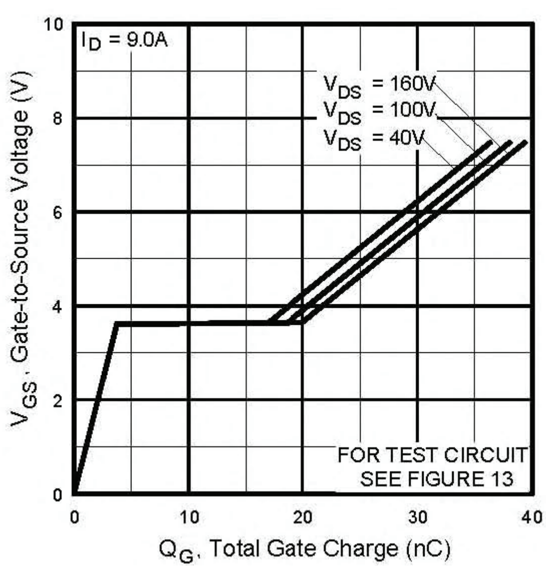


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

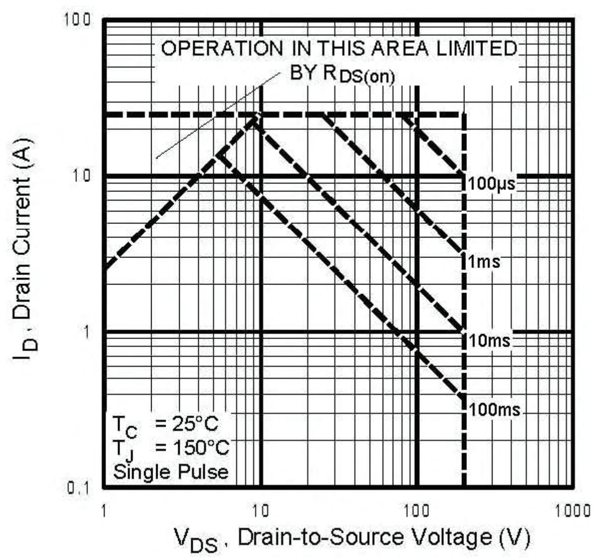


Fig. 8 - Maximum Safe Operating Area

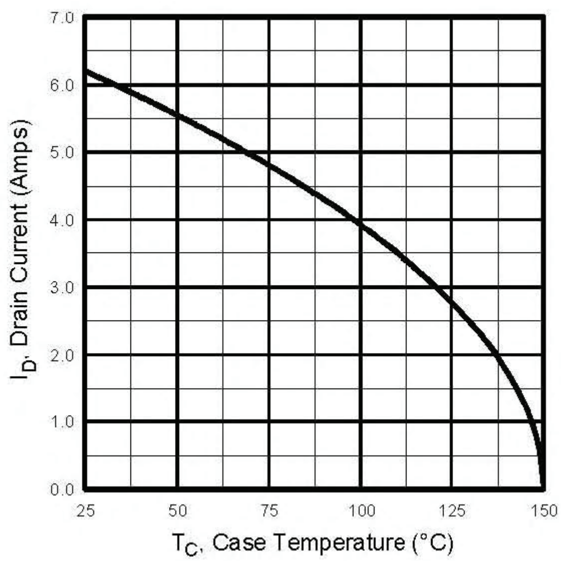


Fig. 9 - Maximum Drain Current vs. Case Temperature

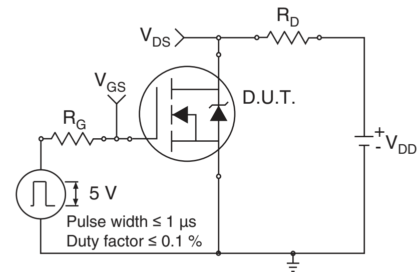


Fig. 10a - Switching Time Test Circuit

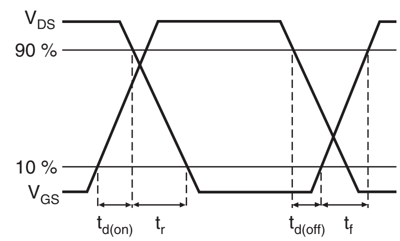


Fig. 10b - Switching Time Waveforms

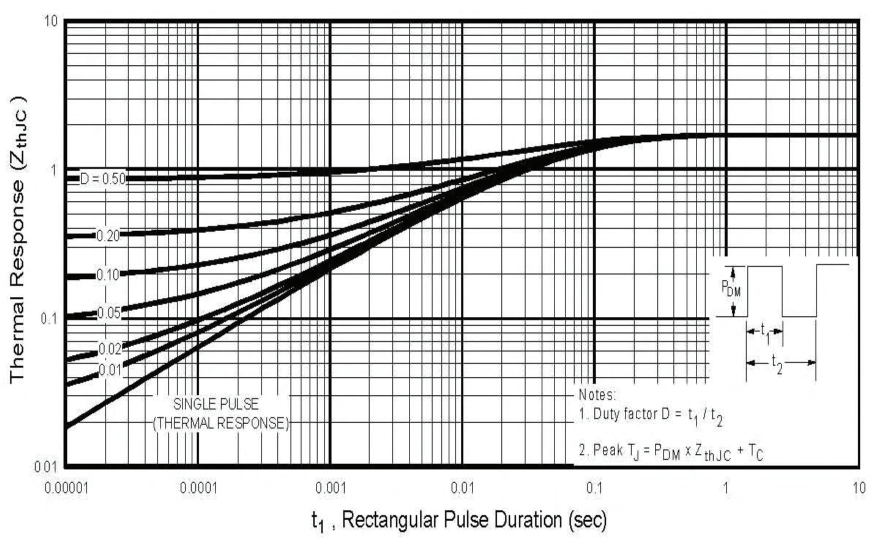


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

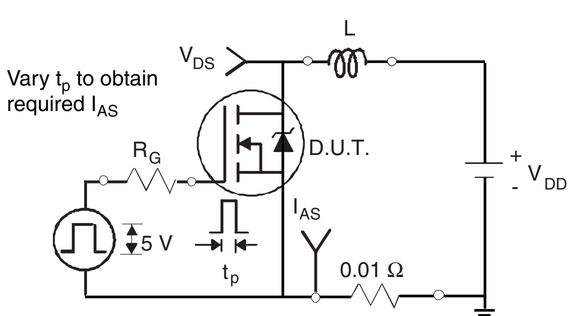


Fig. 12a - Unclamped Inductive Test Circuit

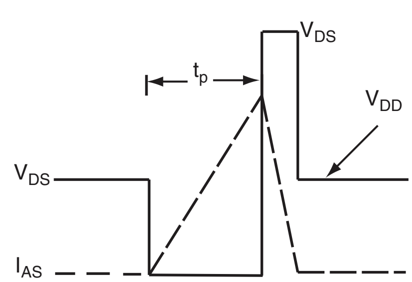


Fig. 12b - Unclamped Inductive Waveforms

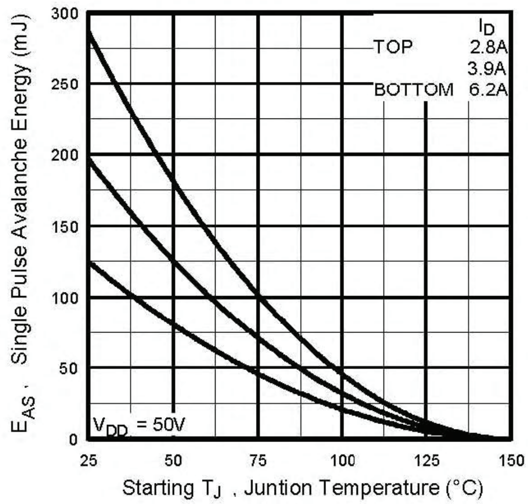


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

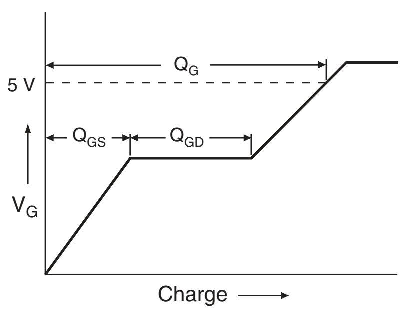


Fig. 13a - Basic Gate Charge Waveform

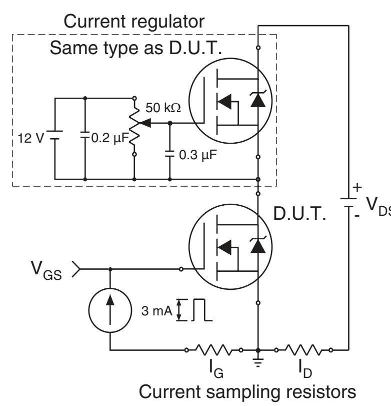
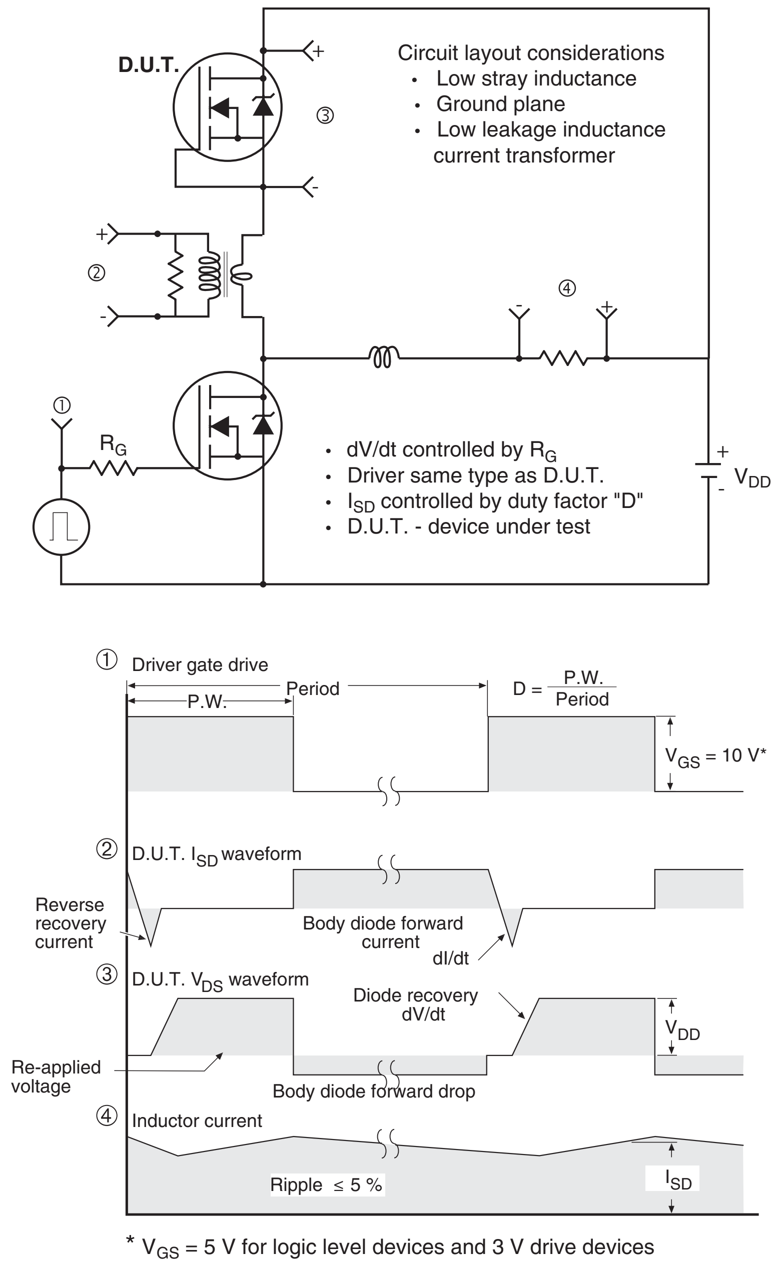


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* V_{GS} = 5 V for logic level devices and 3 V drive devices

Fig. 14 - For N-Channel

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