

KL02 Sub-Family Data Sheet

Supports the following:
MKL02Z32CAF4R and
KKL02Z32CAF4R

Key features

- Operating Characteristics
 - Voltage range: 1.71 to 3.6 V
 - Flash write voltage range: 1.71 to 3.6 V
 - Temperature range (ambient): -40 to 85°C
- Performance
 - Up to 48 MHz ARM® Cortex-M0+ core
- Memories and memory interfaces
 - Up to 32 KB program flash memory
 - Up to 4 KB RAM
- Clocks
 - 32 kHz to 40 kHz crystal oscillator
 - Multi-purpose clock source
- System peripherals
 - Nine low-power modes to provide power optimization based on application requirements
 - COP Software watchdog
 - SWD interface and Micro Trace buffer
 - Bit Manipulation Engine (BME)

KL02P20M48SF0



- Security and integrity modules
 - 80-bit unique identification (ID) number per chip
- Human-machine interface
 - General-purpose input/output
- Analog modules
 - 12-bit SAR ADC
 - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
- Timers
 - Two 2-channel Timer/PWM (TPM)
 - 16-bit low-power timer (LPTMR)
- Communication interfaces
 - One 8-bit SPI module
 - Two I2C modules
 - One low power UART module

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PKL02 and MKL02

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 1. Part number fields descriptions

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow, 3000 pieces reels • P = Prequalification • K = Fully qualified, general market flow, 100 pieces reels
KL##	Kinetis family	• KL02
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 32 = 32 KB

Table continues on the next page...

Table 1. Part number fields descriptions (continued)

Field	Description	Values
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• C = -40 to 85
PP	Package identifier	• AF = 20 WLCSP (1.99 mm x 1.94 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel

2.4 Example

This is an example part number:

MKL02Z32CAF4R

3 Small package marking

In order to save space, small package devices use special marking on the chip.

Q FS FF (TP)

Table 2. Small package marking

Field	Description	Values
Q	Qualification status	• M = M • P = P
FS	Kinetis family and CPU frequency	• (0)2T = KL02, 48 MHz of CPU
FF	Program flash memory size	• 5 = 32 KB
TP	Temperature range (°C) and package	• C = -40 to 85, 20 WLCSP

For example:

M02T5C = MKL02Z32CAFR

4 Terminology and guidelines

4.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

4.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

4.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

4.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

4.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

4.3.1 Example

This is an example of an attribute:

Terminology and guidelines

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

4.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

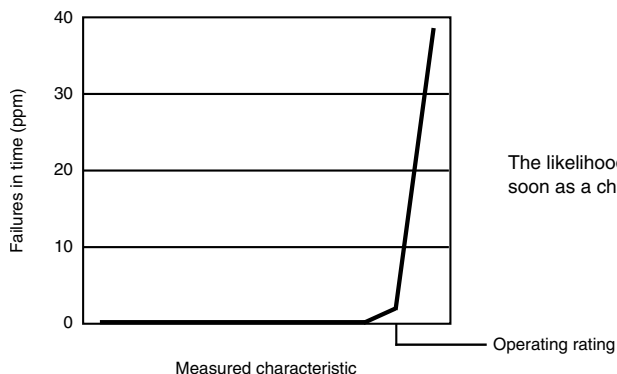
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

4.4.1 Example

This is an example of an operating rating:

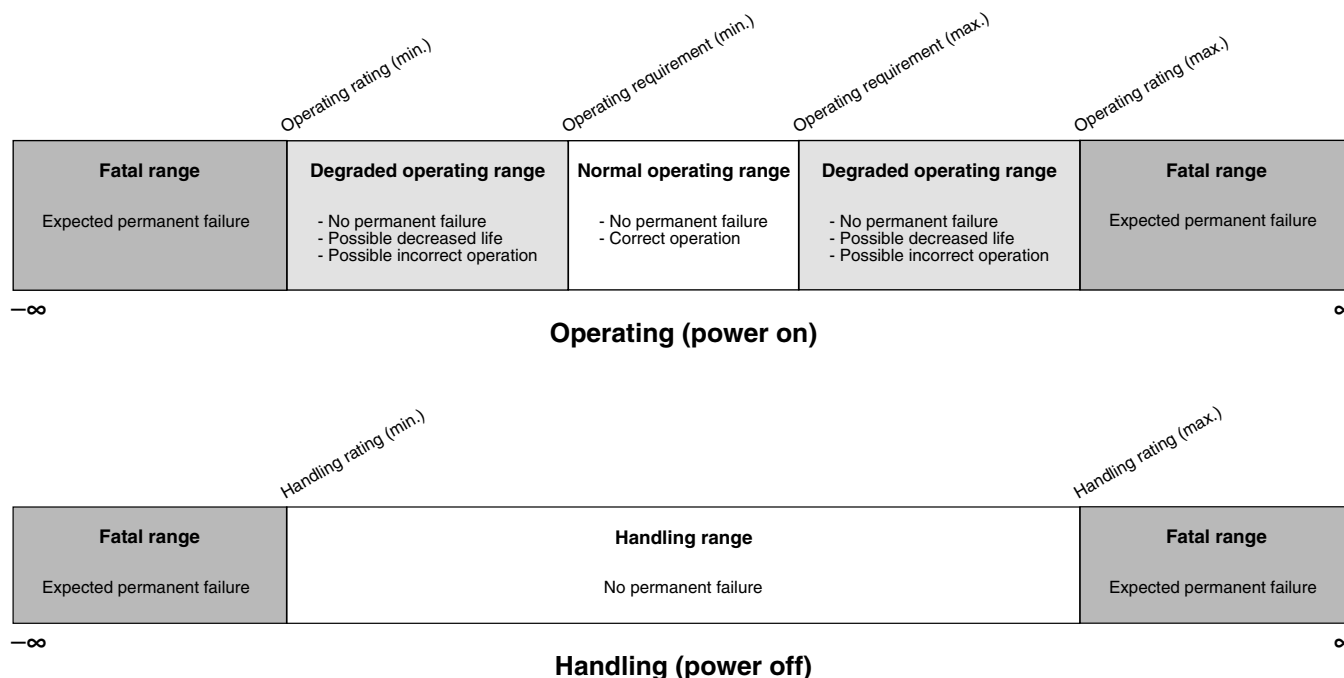
Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

4.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

4.6 Relationship between ratings and operating requirements



4.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

4.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

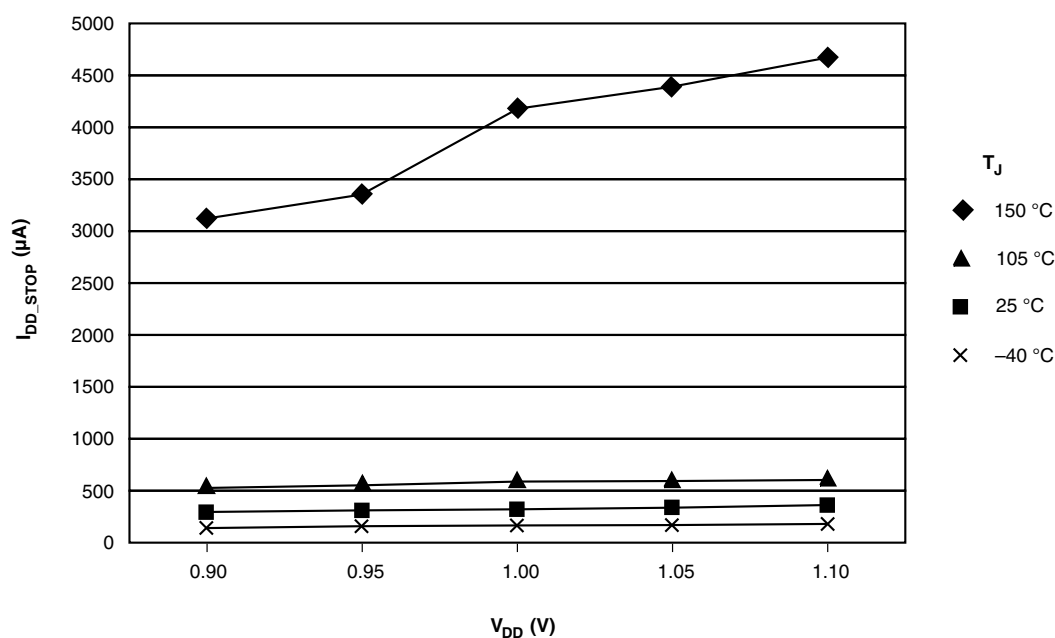
4.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

4.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



4.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 3. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	$^{\circ}C$

Table continues on the next page...

Table 3. Typical value conditions (continued)

Symbol	Description	Value	Unit
V _{DD}	3.3 V supply voltage	3.3	V

5 Ratings

5.1 Thermal handling ratings

Table 4. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2 Moisture handling ratings

Table 5. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.3 ESD handling ratings

Table 6. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

5.4 Voltage and current operating ratings

Table 7. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

6 General

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

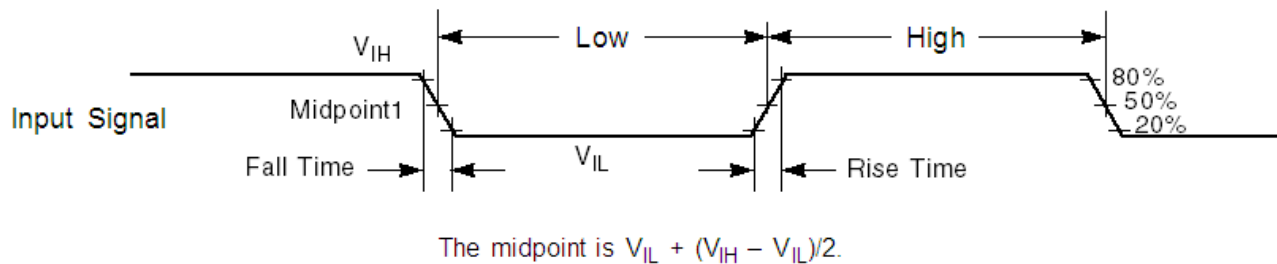


Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

6.2 Nonswitching electrical specifications

6.2.1 Voltage and current operating requirements

Table 8. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	—
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	—
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	—
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	—
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	—
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	—
I_{ICIO}	IO pin negative DC injection current—single pin $V_{IN} < V_{SS} - 0.3\text{V}$	-5	—	mA	1
I_{Ccont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins - Negative current injection - Positive current injection	-25	—	mA	—
		—	+25		
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	—

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS} - 0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.

6.2.2 LVD and POR operating requirements

Table 9. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LV DV = 01)	2.48	2.56	2.64	V	—
V_{LVW1H} V_{LVW2H}	Low-voltage warning thresholds — high range - Level 1 falling (LVWV = 00) - Level 2 falling (LVWV = 01)	2.62 2.72	2.70 2.80	2.78 2.88	V V	1

Table continues on the next page...

Table 9. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
V _{LVW1L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	1
V _{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V _{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V _{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	—

1. Rising thresholds are falling threshold + hysteresis voltage

6.2.3 Voltage and current operating behaviors

Table 10. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — Normal drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = −5 mA	V _{DD} − 0.5	—	V	1
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = −1.5 mA	V _{DD} − 0.5	—	V	
V _{OH}	Output high voltage — High drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = −18 mA	V _{DD} − 0.5	—	V	1
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = −6 mA	V _{DD} − 0.5	—	V	
I _{OHT}	Output high current total for all ports	—	100	mA	
V _{OL}	Output low voltage — Normal drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA	—	0.5	V	1
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 1.5 mA	—	0.5	V	
V _{OL}	Output low voltage — High drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 18 mA	—	0.5	V	1
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 6 mA	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	

Table continues on the next page...

Table 10. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	μA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R_{PU}	Internal pullup resistors	20	50	$k\Omega$	3

1. PTA12, PTA13, PTB0 and PTB1 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at $V_{DD} = 3.6 V$
3. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

6.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

Table 11. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs
	• $VLLS0 \rightarrow RUN$	—	95	115	μs
	• $VLLS1 \rightarrow RUN$	—	93	115	μs
	• $VLLS3 \rightarrow RUN$	—	42	53	μs
	• $VLPS \rightarrow RUN$	—	4	4.4	μs
	• $STOP \rightarrow RUN$	—	4	4.4	μs

6.2.5 Power consumption operating behaviors

Table 12. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note 1	mA	1
I _{DD_RUNCO}	Run mode current in compute operation—48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V	—	3.6	4.7	mA	2
I _{DD_RUN}	Run mode current—48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V	—	4.26	5.3	mA	2
I _{DD_RUN}	Run mode current—48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash - at 3.0 V - at 25 °C - at 95 °C	— —	4.2 4.3	6.4 7.0	mA mA	2, 3
I _{DD_WAIT}	Wait mode current—core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	—	3.18	4.1	mA	2
I _{DD_WAIT}	Wait mode current—core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	—	2.62	2.9	mA	2
I _{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option—core and system disabled / 10.5 MHz bus at 3.0 V	—	2.18	3.27	mA	2
I _{DD_VLPRCO}	Very-low-power run mode current in compute operation—4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V	—	144.7	434.7	μA	4
I _{DD_VLPR}	Very-low-power run mode current—4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V	—	165.2	314.0	μA	4
I _{DD_VLPR}	Very-low-power run mode current—4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V	—	184.8	351.2	μA	3, 4

Table continues on the next page...

Table 12. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPW}	Very-low-power wait mode current—core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V	—	93.4	334.4	μA	4
I _{DD_STOP}	Stop mode current - at 3.0 V - at 25 °C - at 50 °C - at 70 °C - at 85 °C	— — — —	255 259.8 273.2 292.0	427.5 551.0 589.0 684.0	μA	—
I _{DD_VLPS}	Very-low-power stop mode current - at 3.0 V - at 25 °C - at 50 °C - at 70 °C - at 85 °C	— — — —	1.86 3.69 7.6 13.9	10.5 13.0 26.8 46.0	μA	—
I _{DD_VLLS3}	Very-low-leakage stop mode 3 current - at 3.0 V - at 25 °C - at 50 °C - at 70 °C - at 85 °C	— — — —	1.24 1.44 2.32 3.89	2.9 3.6 8.0 9.9	μA	—
I _{DD_VLLS1}	Very-low-leakage stop mode 1 current - at 3.0 V - at 25 °C - at 50 °C - at 70 °C - at 85 °C	— — — —	0.6 0.797 1.41 2.54	1.38 2.3 10.5 10.7	μA	—
I _{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) - at 3.0 V - at 25 °C - at 50 °C - at 70 °C - at 85 °C	— — — —	346 486.1 1090 2230	928.5 1227 2250 4020	nA	—
I _{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	—	160.3	837.9		5

Table 12. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	- at 25 °C - at 50 °C - at 70 °C - at 85 °C	—	304.3	1166.6	nA	
		—	906.3	2470		
		—	2030	4883		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode.
3. Incremental current consumption from peripheral activity is not included.
4. MCG configured for BLPI mode.
5. No brownout

Table 13. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. - VLLS1 - VLLS3 - VLPS - STOP	440	490	540	560	570	nA
		440	490	540	560	570	
		510	560	560	560	610	
		510	560	560	560	610	
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	μA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	μA
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the						

Table continues on the next page...

Table 13. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)					Unit
		-40	25	50	70	85	
	clock signal. Includes selected clock source and I/O switching currents. • MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	μA
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, or VLLSx mode.	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low-power mode using the internal clock and continuous conversions.	366	366	366	366	366	μA

6.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

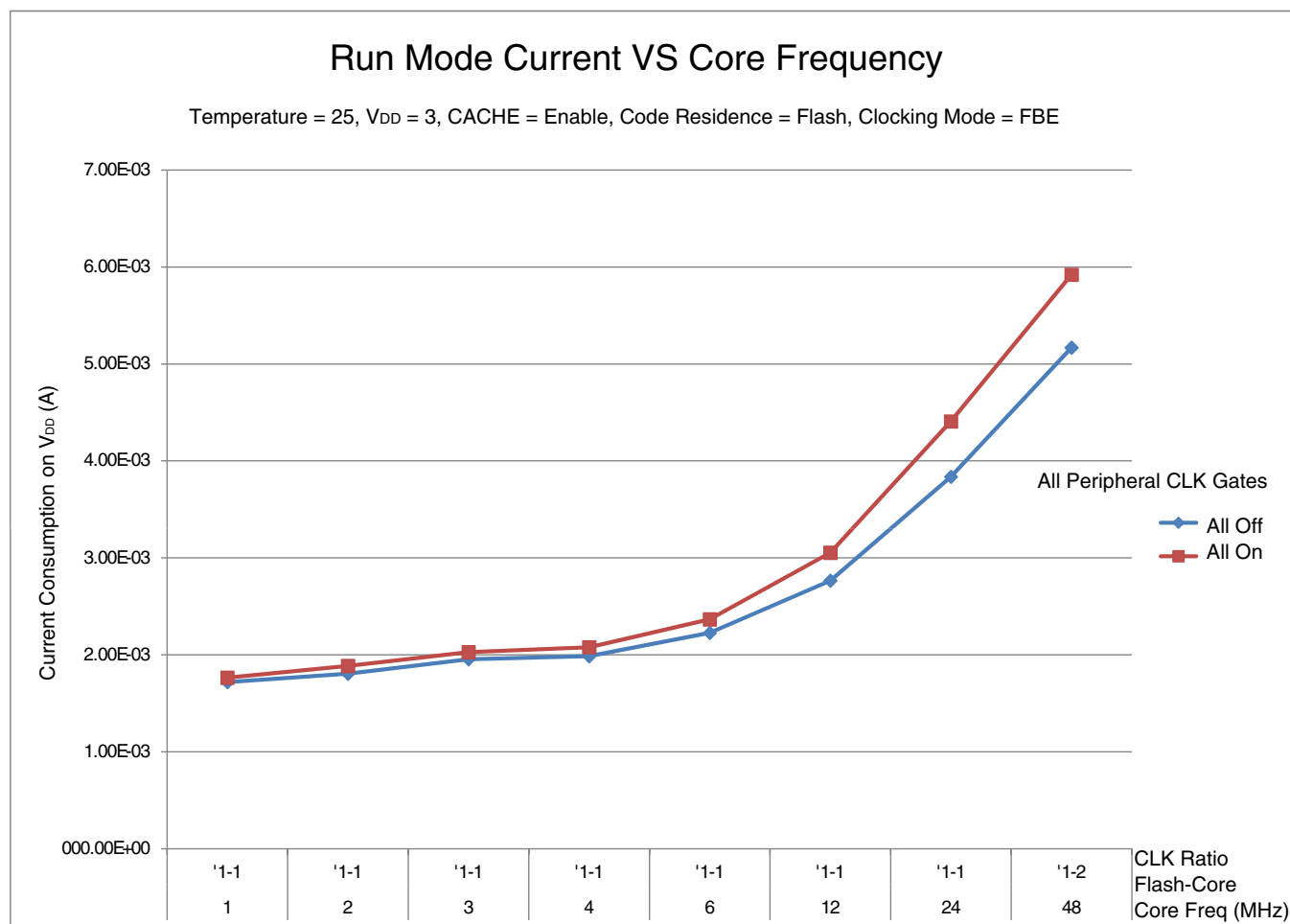


Figure 2. Run mode supply current vs. core frequency

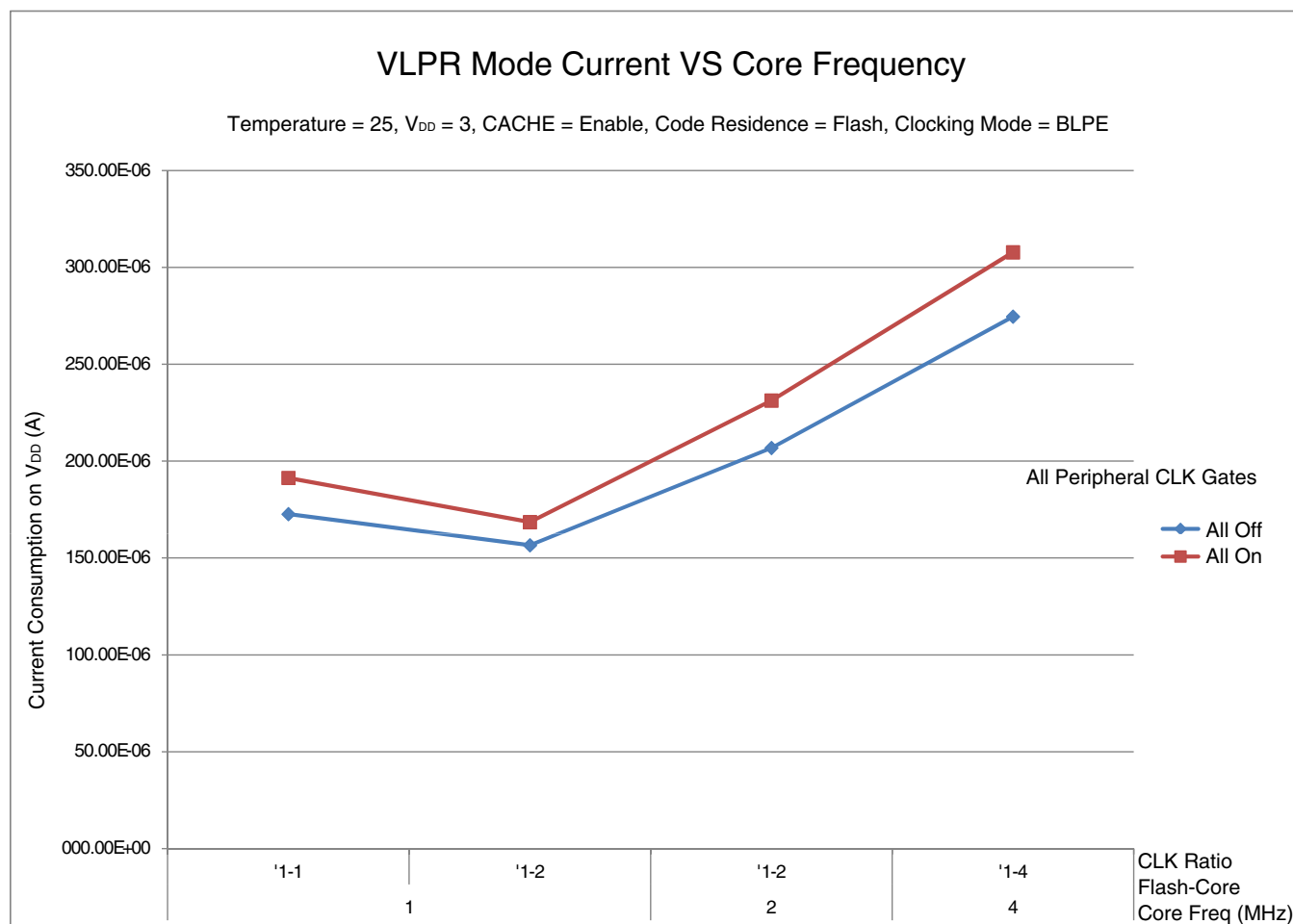


Figure 3. VLPR mode current vs. core frequency

6.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

6.2.7 Capacitance attributes

Table 14. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

6.3 Switching specifications

6.3.1 Device clock specifications

Table 15. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR mode ¹				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
f_{ERCLK}	External reference clock	—	32.768	kHz
$f_{\text{LPTMR_pin}}$	LPTMR clock	—	24	MHz
$f_{\text{LPTMR_ERCLK}}$	LPTMR external reference clock	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
f_{UART0}	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, UART, and I²C signals.

Table 16. Device clock specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
 2. This is the shortest pulse that is guaranteed to be recognized.

3. 75 pF load

6.4 Thermal specifications

6.4.1 Thermal operating requirements

Table 17. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	95	°C
T_A	Ambient temperature	−40	85	°C

6.4.2 Thermal attributes

Table 18. Thermal attributes

Board type	Symbol	Description	20 WLCSP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	69.8	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	57.5	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	62.03	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	54.3	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	51.64	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	0.73	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions — Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions — Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions — Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions — Natural Convection (Still Air)*.

7 Peripheral operating requirements and behaviors

7.1 Core modules

7.1.1 SWD electricals

Table 19. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

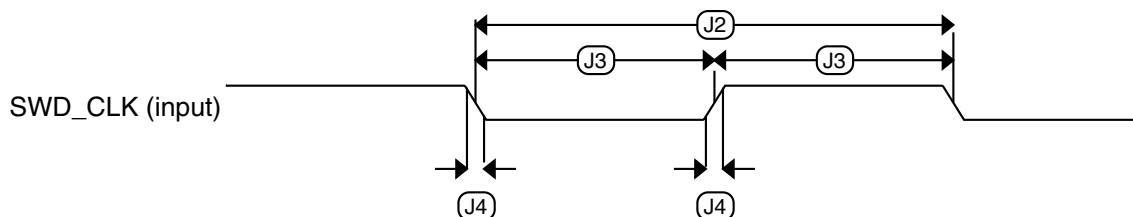


Figure 4. Serial wire clock input timing

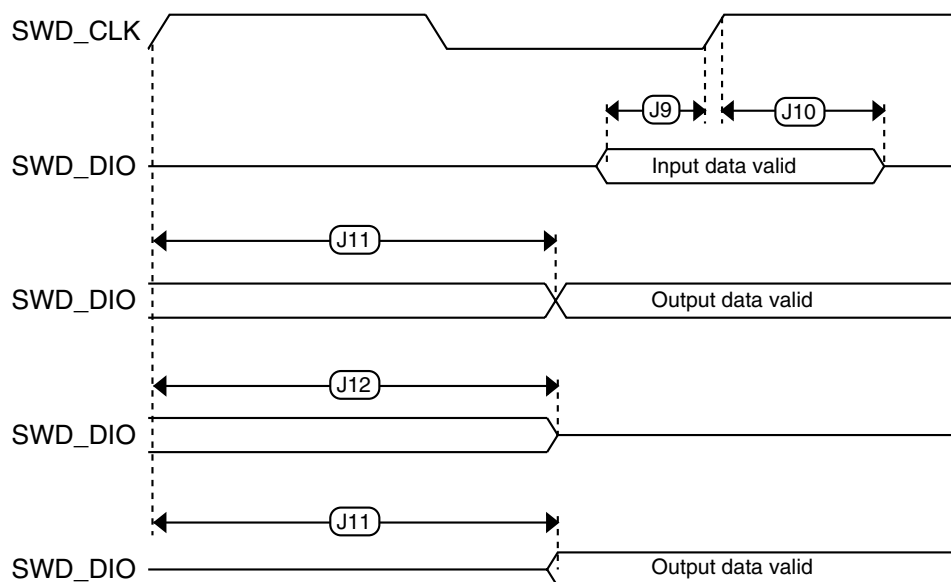


Figure 5. Serial wire data timing

7.2 System modules

There are no specifications necessary for the device's system modules.

7.3 Clock modules

7.3.1 MCG specifications

Table 20. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM]	—	± 0.3	± 0.6	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 3	$\%f_{\text{dco}}$	1, 2

Table continues on the next page...

Table 20. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C		—	± 0.4	± 1.5	% f_{dco}	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	% f_{intf_ft}	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00) $640 \times f_{fll_ref}$	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) $1280 \times f_{fll_ref}$	40	41.94	48	MHz	
$f_{dco_t_DMX32}$	DCO output frequency	Low range (DRS = 00) $732 \times f_{fll_ref}$	—	23.99	—	MHz	5, 6
		Mid range (DRS = 01) $1464 \times f_{fll_ref}$	—	47.97	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz		—	180	—	ps	7
$t_{fll_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft} .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

7.3.2 Oscillator electrical specifications

7.3.2.1 Oscillator DC electrical specifications

Table 21. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0) • 32 kHz	—	500	—	nA	1
I_{DDOSC}	Supply current — high gain mode (HGO=1) • 32 kHz	—	25	—	μ A	1
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M Ω	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M Ω	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k Ω	
V_{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD} =3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

7.3.2.2 Oscillator frequency specifications

Table 22. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—		—	ms	1, 2
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—		—	ms	

1. Proper PC board layout procedures must be followed to achieve specifications.
2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

7.4 Memories and memory interfaces

7.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

7.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

7.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{sec}1\text{k}}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.5	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	61	500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

7.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

7.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years	
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125°C.

7.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

7.6 Analog

7.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

7.6.1.1 12-bit ADC operating conditions

Table 27. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} – V _{SSA})	-100	0	+100	mV	2

Table continues on the next page...

Table 27. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	3
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	3
V _{ADIN}	Input voltage		V _{REFL}	—	V _{REFH}	V	
C _{ADIN}	Input capacitance	• 8-bit / 10-bit / 12-bit modes	—	4	5	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	4
f _{ADCK}	ADC conversion clock frequency	≤ -bit mode	1.0	—	18.0	MHz	5
C _{rate}	ADC conversion rate	≤ -bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

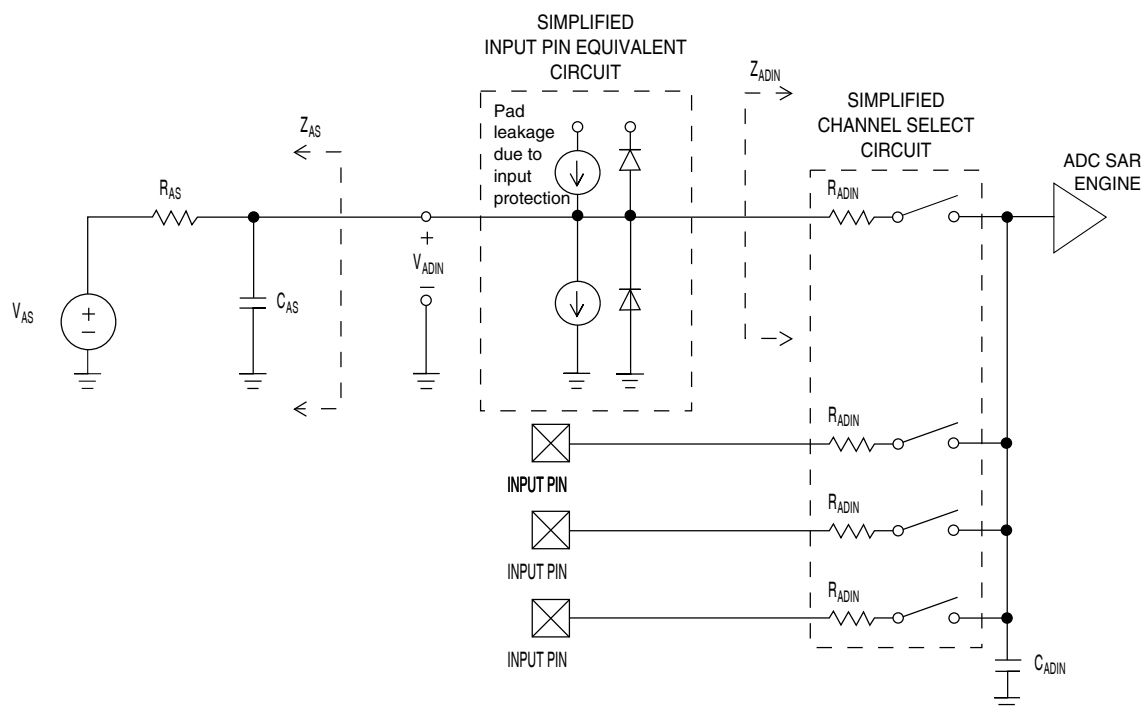


Figure 6. ADC input impedance equivalency diagram

7.6.1.2 12-bit ADC electrical characteristics

Table 28. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

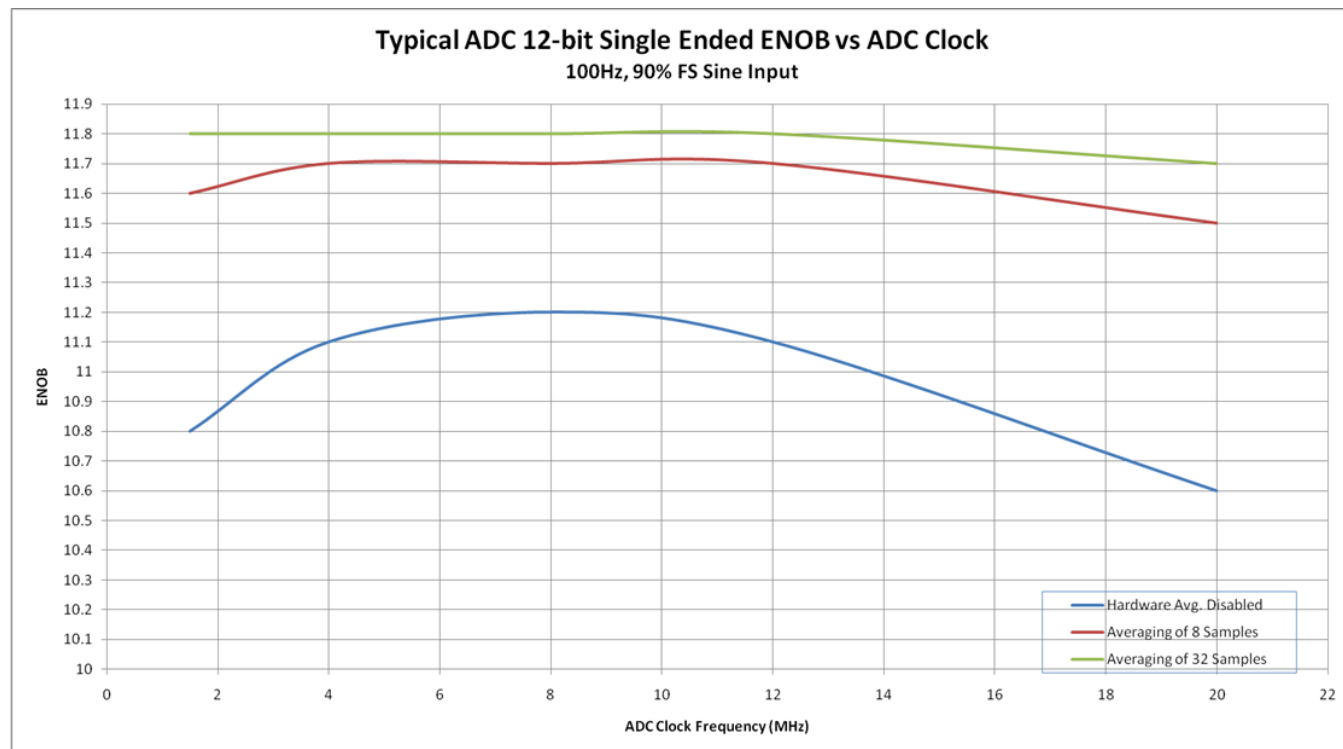
Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5

Table continues on the next page...

Table 28. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
E_Q	Quantization error	• -bit modes	—	—	± 0.5	LSB ⁴	
E_{IL}	Input leakage error		$I_{IN} \times R_{AS}$			mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	6
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	6

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. ADC conversion clock < 3 MHz

**Figure 7. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode**

7.6.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μ A
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μ A
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	−0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	−0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

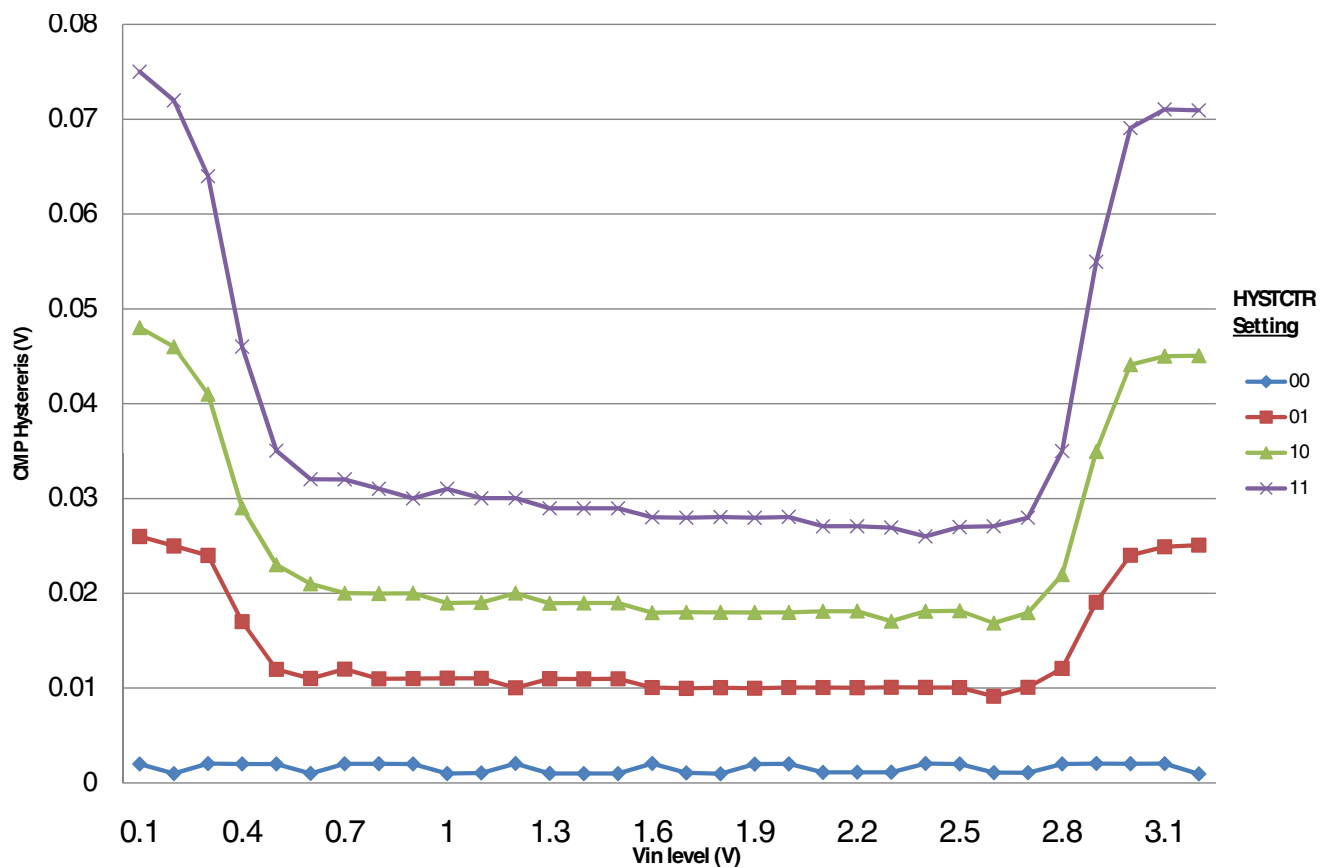


Figure 8. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

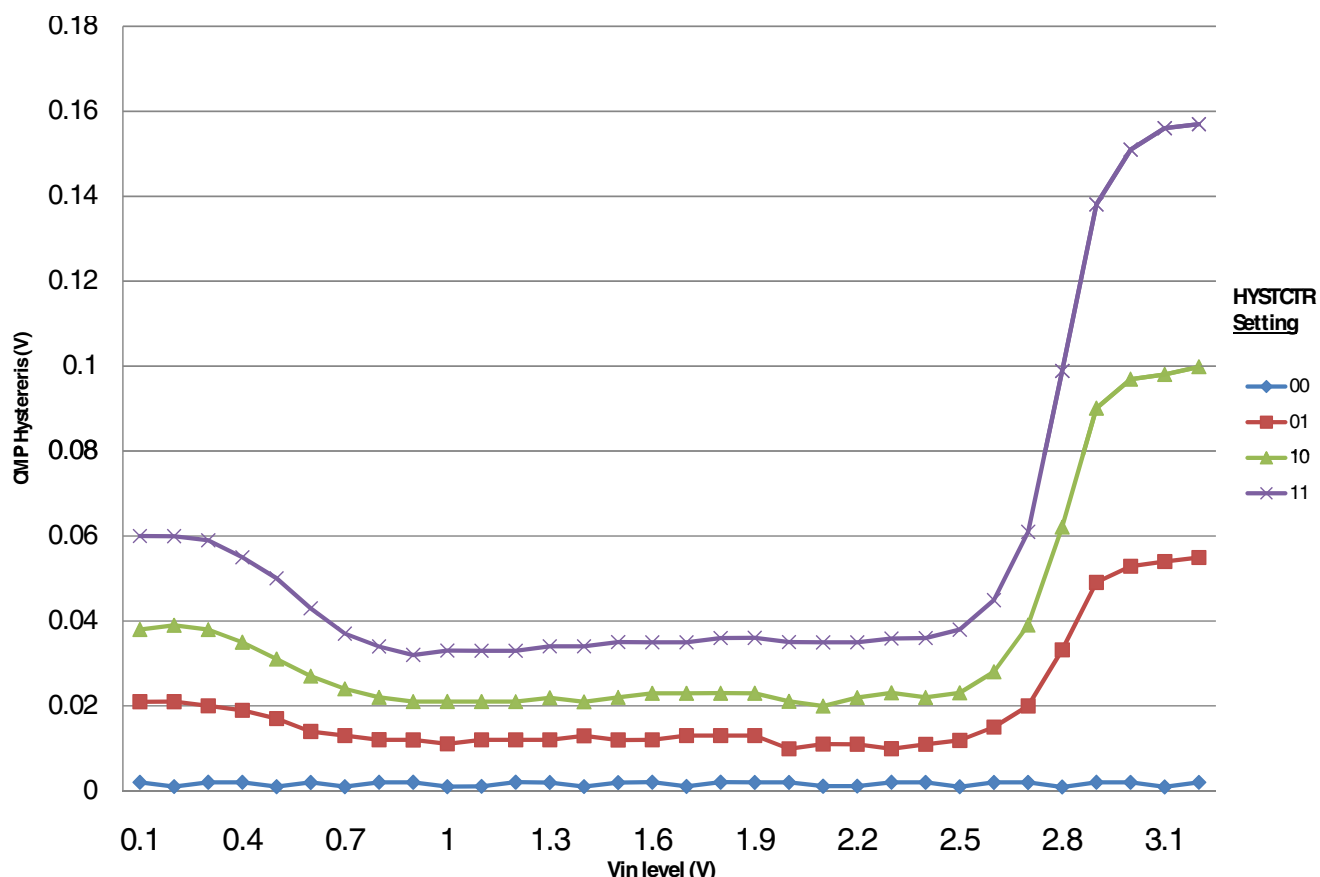


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

7.7 Timers

See [General switching specifications](#).

7.8 Communication interfaces

7.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

Peripheral operating requirements and behaviors

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 30. SPI master mode timing on slew rate disabled pads

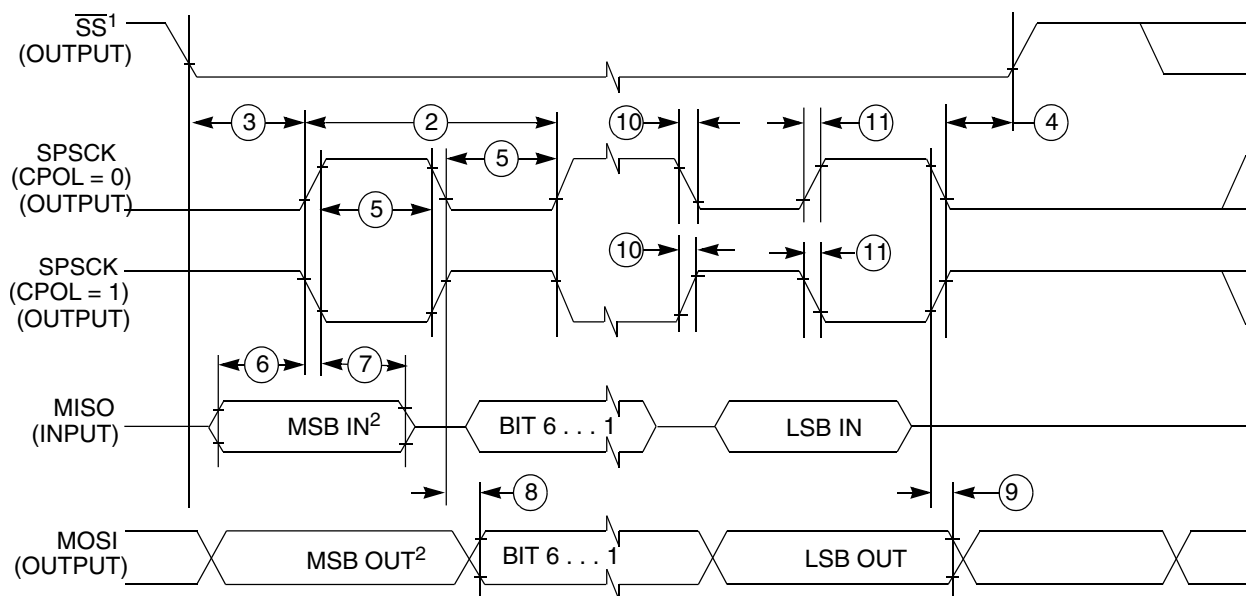
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	10	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$

Table 31. SPI master mode timing on slew rate enabled pads

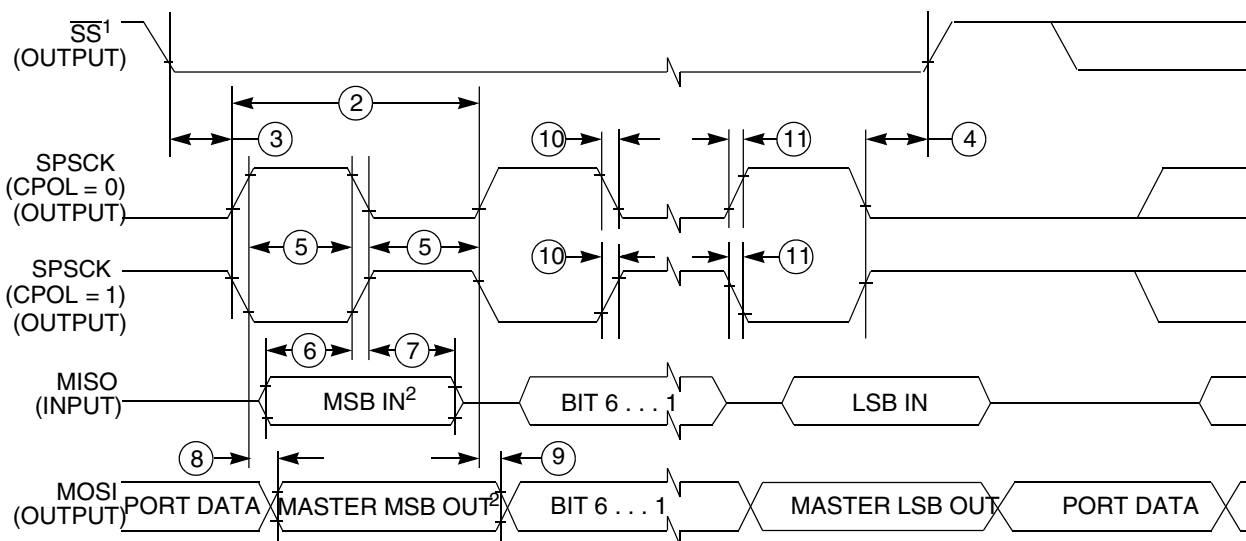
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 10. SPI master mode timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 11. SPI master mode timing (CPHA = 1)

Table 32. SPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCCK}	SPSCCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{periph} - 30$	—	ns	—

Table continues on the next page...

Table 32. SPI slave mode timing on slew rate disabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 33. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCCK}	SPSCCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

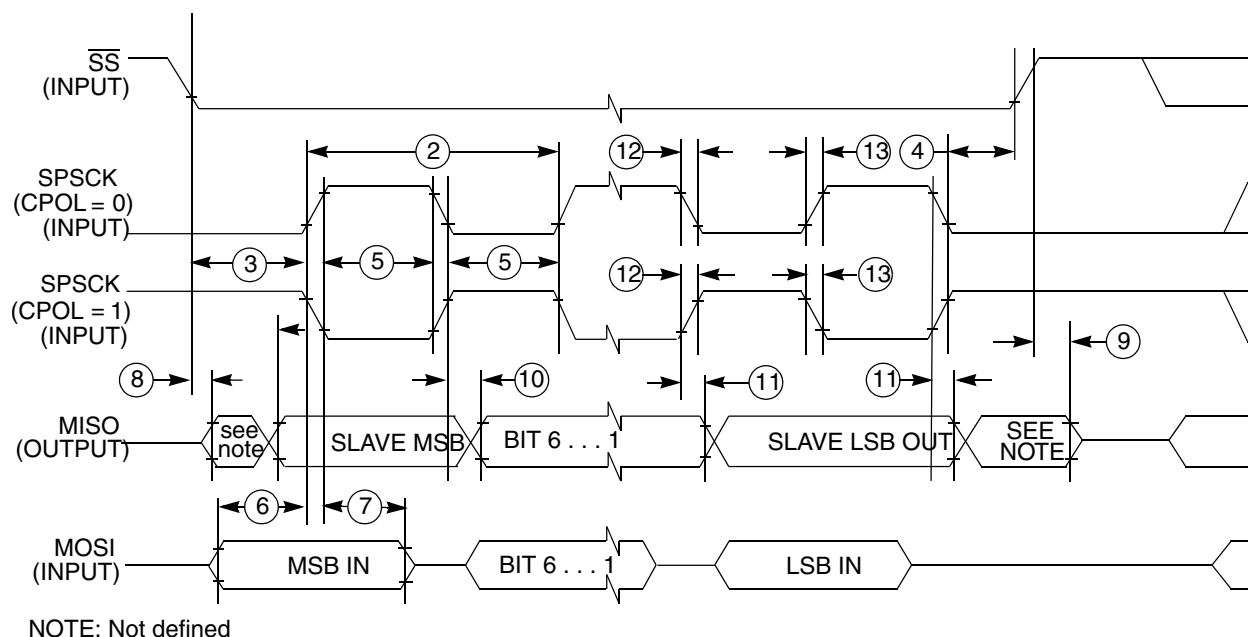


Figure 12. SPI slave mode timing (CPHA = 0)

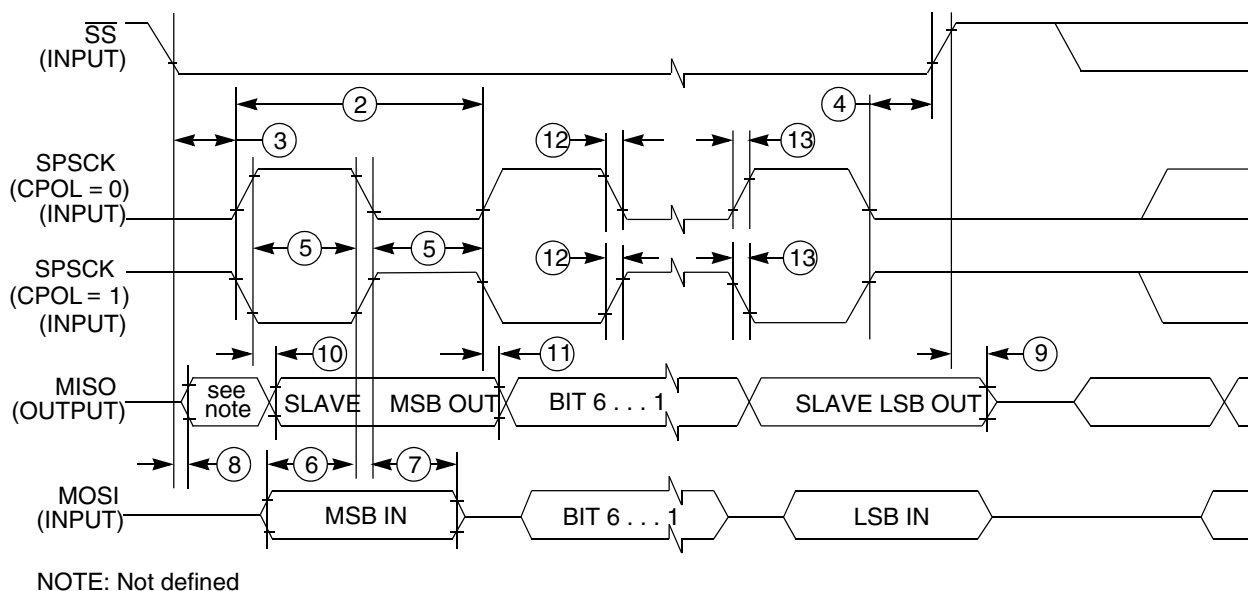


Figure 13. SPI slave mode timing (CPHA = 1)

7.8.2 I²C

See [General switching specifications](#).

7.8.3 UART

See [General switching specifications](#).

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
20-pin WLCSP	98ASA00539D

9 Pinout

9.1 KL02 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

PTB3 and PTB4 are true open drain pins. The external pullup resistor must be added to make them output correct values in using I2C, GPIO, and UART0.

20 WLC SP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
B4	VDD	VDD	VDD			
B4	VREFH	VREFH	VREFH			
C3	VREFL	VREFL	VREFL			
C3	VSS	VSS	VSS			
C4	PTA3	EXTAL0	EXTAL0	PTA3	I2C0_SCL	I2C1_SDA
D4	PTA4	XTAL0	XTAL0	PTA4	I2C0_SDA	I2C1_SCL
E3	PTA5	DISABLED		PTA5	TPM0_CH1	SPI0_SS_b
E4	PTA6	DISABLED		PTA6	TPM0_CH0	SPI0_MISO
E1	PTA7/ IRQ_4	ADC0_SE7	ADC0_SE7	PTA7/ IRQ_4	SPI0_MISO	SPI0_MOSI

20 WLC SP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
E2	PTB0/ IRQ_5	ADC0_SE6	ADC0_SE6	PTB0/ IRQ_5	EXTRG_IN	SPI0_SCK
D3	PTB1/ IRQ_6	ADC0_SE5/ CMP0_IN3	ADC0_SE5/ CMP0_IN3	PTB1/ IRQ_6	UART0_TX	UART0_RX
D2	PTB2/ IRQ_7	ADC0_SE4	ADC0_SE4	PTB2/ IRQ_7	UART0_RX	UART0_TX
D1	PTA8	ADC0_SE3	ADC0_SE3	PTA8	I2C1_SCL	
C1	PTA9	ADC0_SE2	ADC0_SE2	PTA9	I2C1_SDA	
B1	PTB3/ IRQ_10	DISABLED		PTB3/ IRQ_10	I2C0_SCL	UART0_TX
C2	PTB4/ IRQ_11	DISABLED		PTB4/ IRQ_11	I2C0_SDA	UART0_RX
B2	PTB5/ IRQ_12	NMI_b	ADC0_SE1/ CMP0_IN1	PTB5/ IRQ_12	TPM1_CH1	NMI_b
A1	PTA12/ IRQ_13/ LPTMR0_ALT2	ADC0_SE0/ CMP0_IN0	ADC0_SE0/ CMP0_IN0	PTA12/ IRQ_13/ LPTMR0_ALT2	TPM1_CH0	TPM_CLKIN0
A2	PTB13	ADC0_SE13	ADC0_SE13	PTB13	TPM1_CH1	
A3	PTA0/ IRQ_0	SWD_CLK	ADC0_SE12/ CMP0_IN2	PTA0/ IRQ_0	TPM1_CH0	SWD_CLK
A4	PTA1/ IRQ_1/ LPTMR0_ALT1	RESET_b		PTA1/ IRQ_1/ LPTMR0_ALT1	TPM_CLKIN0	RESET_b
B3	PTA2	SWD_DIO		PTA2	CMP0_OUT	SWD_DIO

9.2 KL02 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL02 signal multiplexing and pin assignments](#).

	1	2	3	4	
A	PTA12	PTB13	PTA0	PTA1	A
B	PTB3	PTB5	PTA2	VDD VREFH	B
C	PTA9	PTB4	VSS VREFL	PTA3	C
D	PTA8	PTB2	PTB1	PTA4	D
E	PTA7	PTB0	PTA5	PTA6	E
	1	2	3	4	

Figure 14. KL02 20-pin WLCSP pinout diagram

10 Revision history

The following table provides a revision history for this document.

Table 34. Revision history

Rev. No.	Date	Substantial Changes
2	05/2013	Public release.
2.1	07/2013	- Removed the specification on OSCERCLK (4 MHz external crystal) because KL02 does not support it. - Added KKL02Z32CAF4R information.



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