Features

- Supports Lattice ECP2 family
- Available in three versions:
  - Base Enhanced Video Controller modue
  - Base plus 2D Graphic Accelerator module
  - Base plus 2D and Video Input module
- Supports video controller module
- Supports touch controller module
- Supports backlight dimming control
- Supports memory controller module
- Supports USB control
- Supports SPI slave interface
- Supports DMA access
- On full version also Video input module is supported
- System-on-chip architecture based on the AMBA® 3 AHB-Lite™ interconnect and AMBA® 3 APB™ interconnect.

Table 1: Core Facts

Implementation data	
Documentation	Datasheet, User's Manual
Design File Formats	EDIF netlist
Constraint Files	LPF file
Reference Designs & Application Notes	Implementation examples
Design Tool	IspLEVER 7.2
FPGA Devices	ECP2 Family
Support	
Support provided by Exor International	

Application

- Industrial and Automated Control Markets
- Automotive graphics and Video Systems
- Medical Monitors and Instrumentation
- Household consumer products
- Building Automation HMI
- Marine Systems
- Consumer Automation (kiosks, vending machines, ATMs)

Table 2: Core Performance Data[1]

LCD-Pro IP version	Example Device	Slices	LUT-4s	Registers	EBRs	PLLs/ DLLs	External Pins	DSP Sites	Multipliers
Base Enhanced Video Controller module	ECP2-20-5	8358	13288	9326	4	1/1	118	4	4
Base plus 2D Graphic Accelerator module	ECP2-35-5	13553	21370	14994	7	1/1	118	34	25
Base plus 2D and Video Input module	ECP2-50-5	16334	25057	18156	12	1/1	146	72	49

[1] Performance and utilization characteristics are in Lattice's ispLEVER® v.7.2 SP1 software. When using this IP core in a different density, speed, or grade within a Lattice FPGA family or in a different software version, performance may vary.

General Description

The LCD-Pro modules are multipurpose Video controller, targeted for TFT displays.
The module's functionality is implemented using an FPGA-based system-on-chip implemented in the Lattice ECP2 family FPGA. The system-on-chip is based on the AMBA 3 AHB-Lite interconnect and the AMBA 3 APB interconnect. The SoC architecture enables simplified FPGA design integration and IP-block oriented design for the FPGA.
One of the features of the LCD-Pro modules is the ability to operate as a standalone USB peripheral.
All LCD-Pro versions support the 8051-based high speed USB peripheral controller, Cypress EZ-USB FX2 (CY7C68013A), used for interfacing the LCD-Pro module to a device with USB host functionality, such as PCs and USB-OTG compliant devices.

The customer can choose the best version fitting the proper features required on the final system.

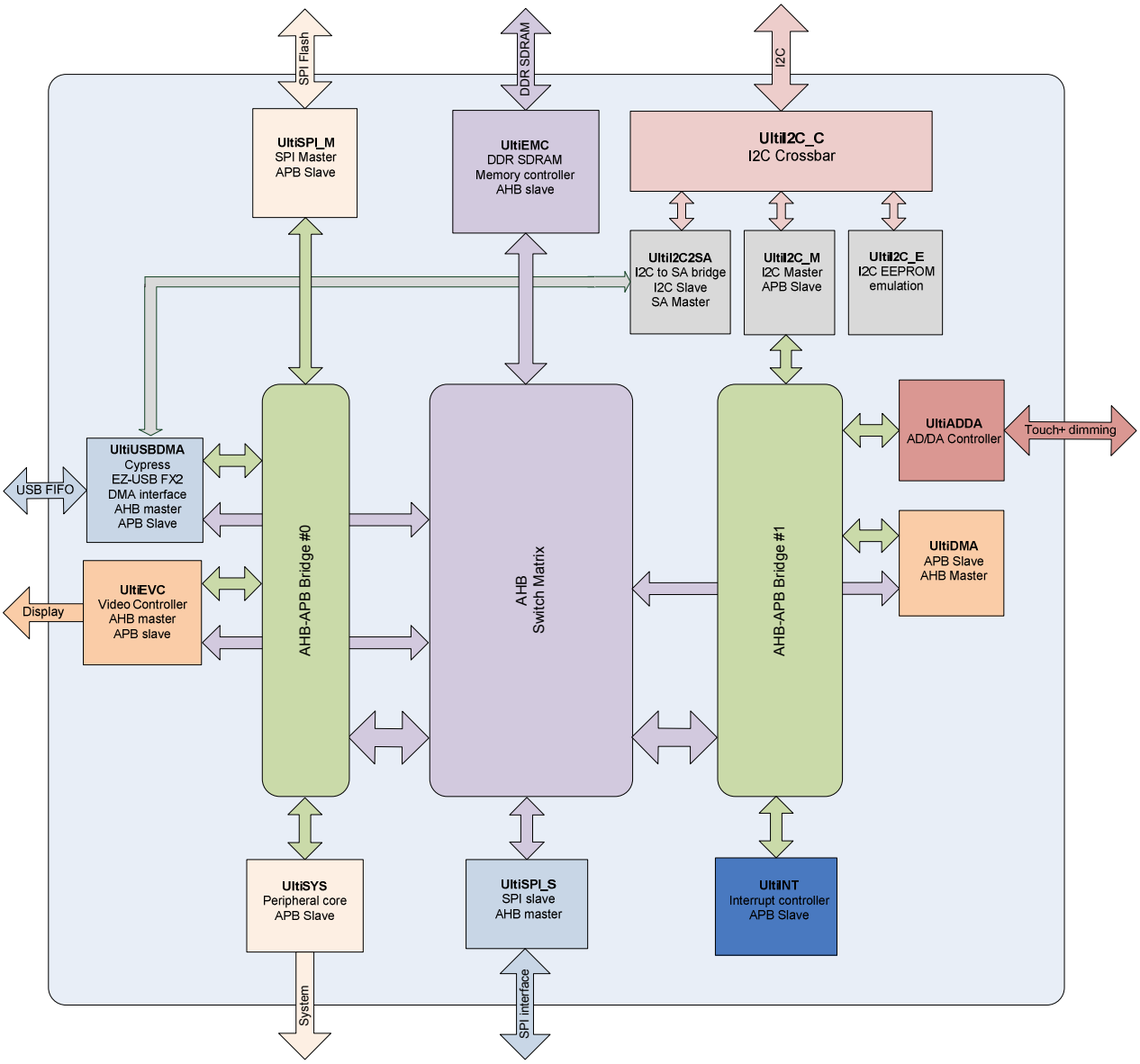

Figure 1: Base Enhanced Video Controller version

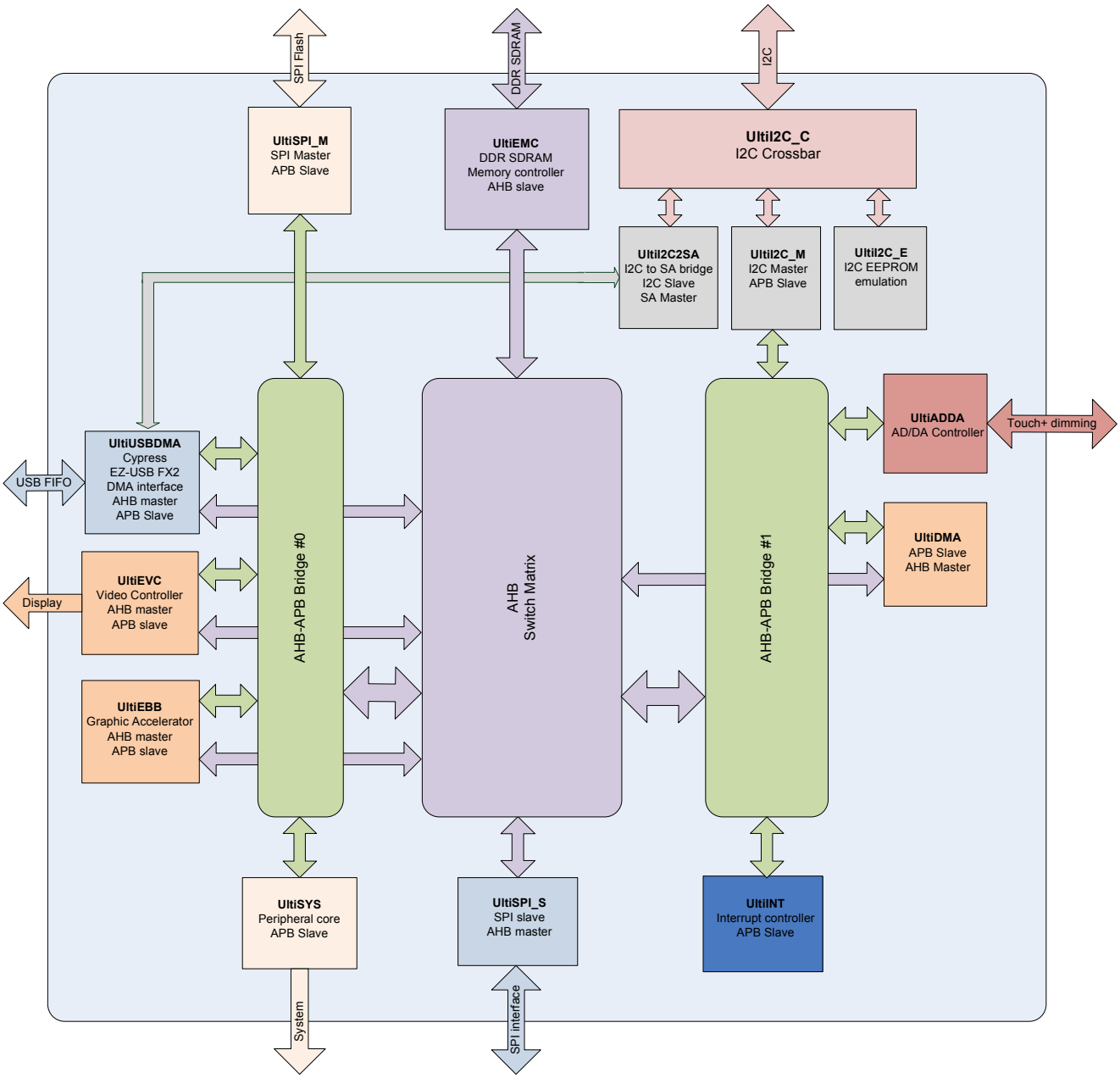

Figure 2: Base plus Graphic Accelerator module version.

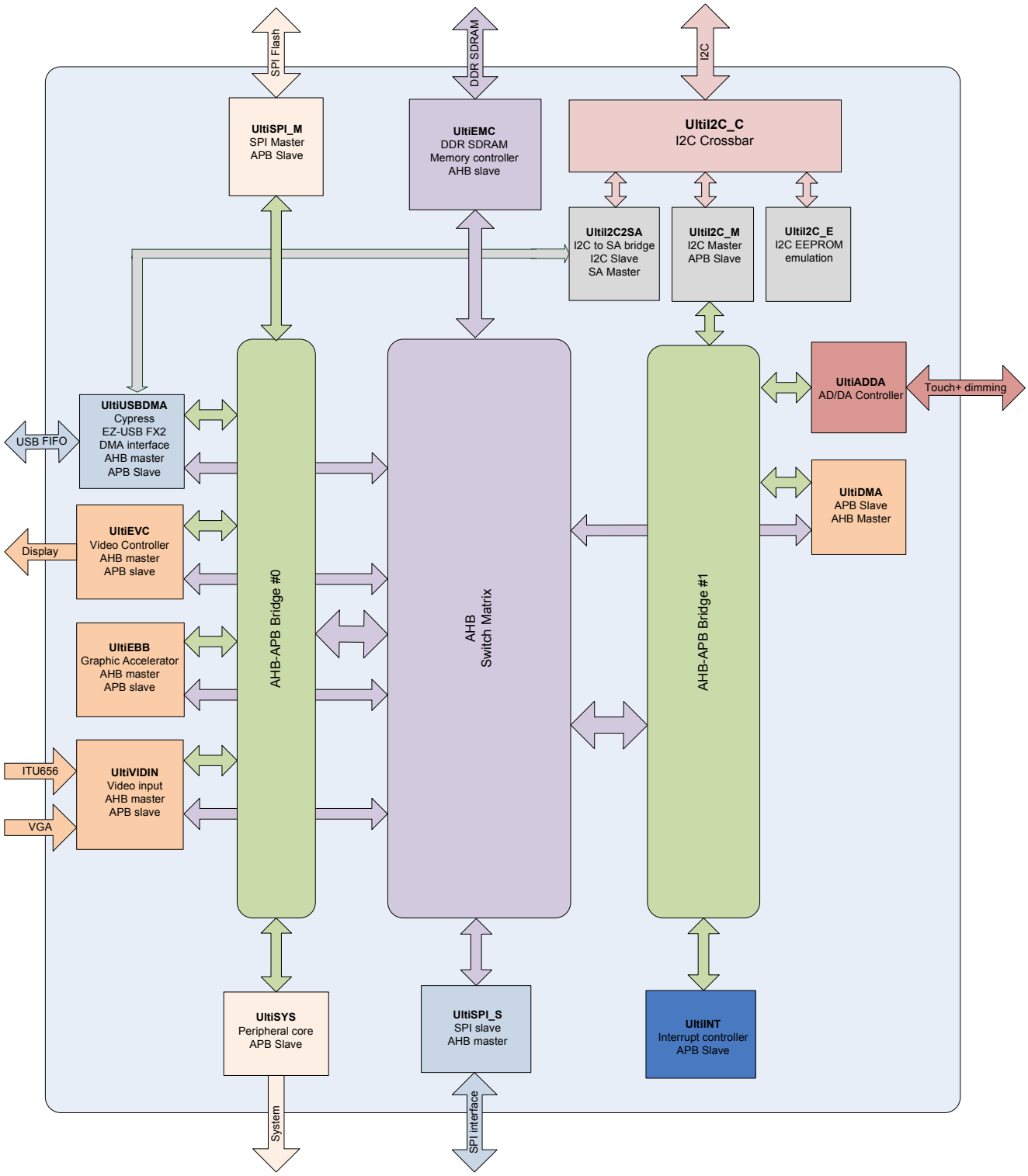

Figure 3: LCD-Pro Block Diagram. Base plus 2D and Video module version.

Functional Description

The LCD-Pro modules consist of:

- UltiUSBDMA interface, enabling high speed transfers from the USB directly to the AMBA 3 AHB-Lite interconnect.
- UltiI2C2SA – I2C to AMBA 3 AHB-Lite interface single access (SA) bridge, used to connect for control access
- UltiI2C_C – I2C crossbar used to connect and decouple multiple I2C buses
- UltiI2C_E – EEPROM emulation used for boot-up initialization of the Cypress EZ-USB FX2, containing hardcoded USB vendor and product ID
- UltiI2C_M – I2C master
- UltiEMC – DDR memory controller
- UltiSPI_M – SPI master for accessing the SPI flash
- UltiEVC– high performance modular embedded graphic display controller, targeted for driving active matrix flat panel displays
- UltiSYS – System diagnostic led interface
- UltiSPI_S – SPI slave interface
- UltiDMA – Direct memory access interface
- UltiADDA – AD/DA interface, for resistive touch and dimming control
- UltiINT – Interrupt interface
- UltiEBB – designed for acceleration of graphics when driving active matrix flat panel displays. Not available in Base version.
- UltiVIDIN – modular embedded video input controller, supporting ITU656 (PAL) and VGA inputs, deinterlacing and image scaling. Not included in Base version and in Enhanced version.
- AHB switch matrix
- AHB-APB Bridge#0 and AHB-APB Bridge#1

The internal structure is shown in the block diagram - Figure 1 (Base version); Figure 2 (Base plus Graphic Accelerator version); Figure 3 (Base plus 2D and Video module version).

System interconnect

The system interconnect in the LCD-Pro modules is based on AMBA 3 architecture. AMBA 3 (Advanced Microcontroller Bus Architecture) is an open bus specification widely accepted in the IP industry as the standard for system-on-chip interconnect.

The LCD-Pro modules implement AMBA 3 AHB-Lite specification and AMBA 3 APB specification for system interconnection.

Core modifications

Source Code customizing is available through Exor International design service.

Please contact Exor International for any required modifications.

Verification methods

Provided automated VHDL test-bench can be used for the basic functionality test, i.e. simple frame exchange. It is primarily aimed for an integration and software initialization check up.

Recommended design experience

The users should have an experience in the following areas:

- ModelSim
- IspLEVER 7.2
- Synchronous digital circuit design

Pinout

The next table includes the LCD-Pro pinout for Full version for example: signal names are described in Table 3.

Table 3: LCD-Pro Base plus 2D and Video module signal pinout

Signal	Direction	Description
Global control signals		
OSC_IN	In	Oscillator
UltiADDA control signals		
AD_START	In	
AD_IN	In	
DTOUCH	out	
DTOUCH_D_N	out	
RAMP_STOP	out	
AD_SAMPLE	out	
AMUX[2:0]	out	
EN_MUX	out	
UltiEMC memory control signals		
MEM_CLK_P	out	Memory clock
MEM_CLK_N	out	Memory clock inverted
MEM_ADDR[12:0]	out	Row/Column memory address
MEM_BA[1:0]	out	Memory bank address
MEM_CKE	out	Clock enable
MEM_CS_N	out	Chip select
MEM_RAS_N	out	Memory RAS control signal
MEM_CAS_N	out	Memory CAS control signal
MEM_WE_N	out	Memory WE control signal
MEM_DQM[1:0]	out	Memory data mask
MEM_DQS[1:0]	in, out	Memory data strobe input/output
MEM_DATA[15:0]	in, out	Memory data bus input/output
UltiEVC video control signals		
DISP_CLK	out	Display clock
DISP_DATA[23:0]	out	Video display data bus
DISP_VSYNC	out	Vertical sync
DISP_HSYNC	out	Horizontal sync
DISPL_BLANK	out	Blank
DISP_EN_VDD	out	VDD enable
DISP_EN_VEE	out	VEE enable
DISP_EN_BLIGHT	out	Backlight enable
UltiVIDIN video input control signals		
VGA_INPUT.CLK	in	Data clock from AD9882
VGA_INPUT.VSYNC	in	VSYNC pulse from VGA input
VGA_INPUT.HSYNC	in	HSYNC pulse from VGA input
VGA_INPUT.R[4:0]	in	R data from AD9882
VGA.INPUT.G[5:0]	in	G data from AD9882
VGA_INPUT.B[4:0]	in	B data from AD9882
ITU656_INPUT.CLK	in	ITU-656 clock input
ITU656_INPUT.DATA[7:0]	in	ITU-656 video data bus input
UltiI2C_C I2C signals		
SCL	in, out	I2C clock
SDA	in, out	I2C data

UltiUSBDMA USB slave FIFO interface signals		
USB_RST_N	out	Chip reset
FX2_IFCLK	out	Slave FIFO interface clock
FX2_INT0_N	out	Interrupt output
FX2_INT1_N	out	Interrupt output
FX2_SLOE	out	SLOE
FX2_FIFOADR[1:0]	out	FIFO_ADR[1:0]
FX2_PKTEND	out	PKTEND
FX2_PROG	in	FLAGA
FX2_FULL	in	FLAGB
FX2_EMPTY	in	FLAGC
FX2_SLRD	out	SLRD out
FX2_SLWR	out	SLWR out
FX2_FDATA[7:0]	in, out	Data
UltiSYS System outputs		
PWM_OUT	out	PWM output
ERROR	out	Red LED
RUN	out	Green LED
UltiSPI_M SPI master		
SPIM_CLK	out	Clock
SPIM_CS	out	Chip select
SPIM_MISO	in	Master Input Slave Output
SPIM_MOSI	out	Master Output Slave Input
UltiSPI_S SPI interface		
SPI_CS	in	Clock
SPI_SCK	in	Chip select
SPI_MISO	in	Master Input Slave Output
SPI_MOSI	out	Master Output Slave Input