LXT98xx Multi-Port 10/100 Repeaters

Specification Update

November 2001

Notice: The LXT98xx Multi-Port 10/100 Repeaters may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 249355-006

Contents

Revision History

Date	Version	Page #	Description
November 6, 2001	006	10	Clarify Stepping / Revision information.
		10	Add “WFL8” trace code information and provide additional description to “Notes” section of table.
August 13, 2001	005	14	Doc. change: Absolute Max. Rating for Max. Supply Voltage = 4.0V.
June 28, 2001	004	15	Clarify first sentence of Addenda No. 1 description.
June 1st, 2001	003	12	Specification changes added.
March 20, 2001	002	-	Removed pre-production Stepping Errata.
		10	Updated “Markings” table with Manufacturer’s Revision Code information.
January 15, 2001	001	-	Converted to Intel format (no technical or material changes).

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
LXT9860/9880 — Advanced 10/100 Repeater with Integrated Management Datasheet	248987-001
LXT9863/9883 — Advanced 10/100 Unmanaged Repeater Datasheet	249115-001
LXT988X/986X Advanced Repeater - Design and Layout Guide Application Note	249351-001
High-Speed Serial Management Interface for LXT9XX Application Note	249006-001
LXT98xx — LXT98x-to-LXT98xx Migration Application Note	249017-001
Intel® Repeaters IRB Design and Layout Guide Application Note	249018-001
SCC Test Program Sample Source Code Listing Application Note	249358-001
LXD9880 DV Board Kit for 10/100 Applications Developer Manual	249116-001

Nomenclature

Errata are design defects or errors. These may cause the LXT98xx Multi-Port 10/100 Repeaters' behaviors to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the LXT98xx Multi-Port 10/100 Repeaters product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Specification Clarification applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in stepping indicated. Specification Change or Specification Clarification does not apply to this stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings†		Page	Status	ERRATA
	4	5			
1	X	X	11	NoFix	"Data Misplacement in Extended Packets"
2	X	X	11	NoFix	"100M Packet Loss"

† Refer to "Markings" on page 10 for codes to identify various silicon steppings.

Specification Changes

No.	Steppings		Page	SPECIFICATION CHANGES
	4	5		
3	X	X	12	"IR10ENA Asserted to TPOP/N Active Timing"
4	X	X	12	"TPIP/N-to-IR100DV Low Timing"

Specification Clarifications

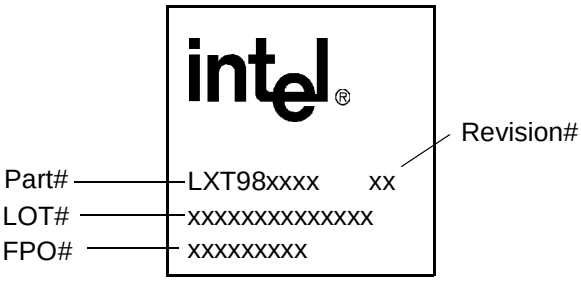
No.	Steppings			Page	SPECIFICATION CLARIFICATIONS
	#	#	#		
					None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	DOCUMENTATION CHANGES
1	003	75	LXT9860/9880 Datasheet: Test Specifications / Absolute Max. Ratings / Supply Voltage Max value is 4.0V.
		44	LXT9863/9883 Datasheet: Test Specifications / Absolute Max. Ratings / Supply Voltage Max value is 4.0V.

Identification Information

Markings

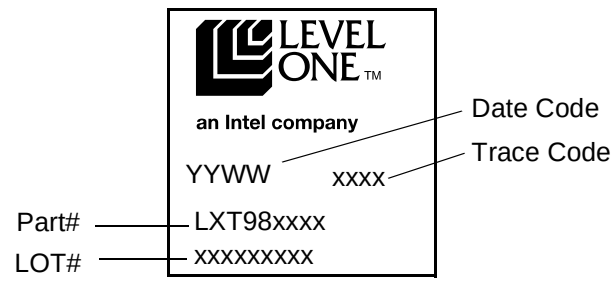


Stepping / Revision Numbers

A “Stepping Number” is assigned when any product design update is released that changes the device errata or specification. A “Revision Number” is assigned to each device tapeout, regardless of impact to device errata or specification. The “Manufacturer’s Revision Number” may be read by software from Register 13C, bits 31:28 in the LXT98xx repeaters.

Stepping	Revision Number[1]	Trace Codes	Manufacturer’s Revision Number[2]	Notes
4	A4, B3	HSD8, WSC6, WSL8	0011	Refers to the Intel part numbers LXT98xxHC
5	B4	WFL8, WFM8, HFF8	0100	Refers to Intel part numbers LXT98xxAHC and LXT9880AGE

1. Revision numbers listed on the same line are the same product stepping, but are produced at different fabrication facilities.
2. This value is from register Register 13C, bits 31:28. Please see the LXT98xx data sheets for more information.



Errata

1. Data Misplacement in Extended Packets

Problem: When extending a packet length to 96 bits, the TP_IDL pulse will be found in extended data field.

Implication: Since the packet extension is seen as a fragment, this issue is benign in networks.

Status: No Fix.

2. 100M Packet Loss

Problem: In a unique network configuration involving stacked repeaters with mixed cable lengths, short IFGs (less than 9 BT) on the 100M IRB causes internal state machines to lose synchronization. The short IFG is caused when 2 ports (using short cables) experience a collision while one port's transmission (using a long cable) reaches the repeater within 9 BT after the end of the collision.

Implication: When the next packet is sent, error codes (Hs) are substituted throughout, resulting in packet loss and re-synchronization of the state machines by EOP. The errored packet is retransmitted.

Status: No Fix. (This is a network configuration issue; therefore, no plans to fix.)

Specification Changes

1. $\overline{\text{IR10ENA}}$ Asserted to TPOP/N Active Timing

Description: The minimum bit time for $\overline{\text{IR10ENA}}$ asserted to TPOP/N is reduced from 5BT to 4BT in Table 42: 10 Mbps IRB-to-TP Port Timing Parameter.

Implication: IEEE 802.3 Standard specifies a maximum BT (Bit) time for twisted-pair timing. Reducing the minimum bit time does not impact performance or IEEE compliance.

Status: No Fix.

2. TPIP/N-to-$\overline{\text{IR100DV}}$ Low Timing

Description: The minimum bit time for TPIP/N-to-$\overline{\text{IR100DV}}$ Low is reduced from 18BT to 17BT in Table 40: 100 Mbps TP-to-IRB Timing parameters.

Implication: IEEE 802.3 Standard specifies a 46 Bit time maximum for twisted-pair port to port timing. Reducing the minimum bit time for twisted-pair port to IRB will not impact performance or IEEE compliance.

Status: No Fix.

Specification Clarifications

There are no specification clarifications.

Documentation Changes

Under “Test Specification” section for both the LXT9880/9860 and LXT9883/9863, the Absolute Maximum Ratings Supply Voltage “Max” is changed to 4.0V.

Addenda

1. 100BASE-TX Receive Jitter Tolerance

Description: If a receive-link partner operating in 100BASE-TX generates transmit jitter greater than the IEEE standard, the LXT9860/63/80/83 devices may produce errors within the Reconciliation Sublayer, which can result in failure to link or to sustain link. The LXT9860/63/80/83 devices will be enhanced to allow greater margin to the IEEE standard. The identified change should allow greater design flexibility; however, customers are advised that reliance on such out-of-margin performance is at their own risk.

Status: Implemented in Stepping 5.

2. 10BASE-T Jitter Tolerance

Description: In some 10BASE-T input jitter applications, the LXT9860/63/80/83 device margin may be close to the IEEE standard for input jitter tolerance. The LXT9860/63/80/83 devices will be enhanced to be optimally centered for 10BASE-T input jitter tolerance. The identified change should allow greater design flexibility; however, customers are advised that reliance on such out-of-margin performance is at their own risk.

Status: Implemented in Stepping 5.