Lattice Diamond

Leading-edge design and implementation tools optimized for Lattice FPGA architectures

Lattice Diamond® design software offers leading-edge design and implementation tools optimized for cost-sensitive, low-power Lattice FPGA architectures. Diamond is the next generation replacement for ispLEVER® featuring design exploration, ease of use, improved design flow, and numerous other enhancements. This combination of new and enhanced features allows users to complete designs faster, easier, and with better results than ever before.

Diamond software is available as a download from the Lattice website for both Windows and Linux. Once downloaded and installed, it can be used with either a free license or a subscription license.

Diamond Software Free License

A free license can be requested from the Lattice website. This license provides immediate access to many popular Lattice devices such as MachXO2™, MachXO™, LatticeXP2™ and LatticeECP2™ at no cost. It includes Synopsys® Synplify Pro™ for Lattice synthesis and Aldec® Active-HDL™ Lattice Edition II mixed language simulator.*

Diamond Software Subscription License

A subscription license can be purchased which adds support for all Lattice FPGAs including the latest LatticeECP3™ devices. It also includes Synopsys Synplify Pro for Lattice synthesis and Aldec Active-HDL Lattice Edition II mixed language simulator*.

Key Features and Benefits

- **Design Exploration Features**
  - Explore design alternatives with Implementations & Strategies
  - Run Manager for accelerating exploration and utilizing multi-core processors
  - Integrated HDL code checking
  - Lattice Synthesis Engine (LSE) for additional synthesis exploration options.
- **Ease-of-Use Features**
  - Advanced next generation user interface
  - Centralized reports and messaging
  - Extensive cross-probing support
  - File list View for managing multiple constraint, preference, debug, timing analyzer, and power calculator files
  - ECO Editor for specific physical netlist-level changes
  - Programmer for improved programming support
- **Improved Design Flow**
  - New Timing Analyzer view allows updated timing analysis, including clock jitter analysis, without re-implementing the design
  - Simulation Wizard to easily export designs to multiple simulators
  - Incremental design flow for accelerating run time with small HDL changes
- **Additional Software Included with Diamond**
  - LatticeMico™ system integration for embedded microprocessor applications
  - EPIC full-featured physical netlist-level editor

✓**SUPERIOR DESIGN EXPLORATION**

✓**EASE OF USE**

✓**IMPROVED DESIGN FLOW**

**Aldec Active-HDL Lattice Edition II simulator is only available for Windows. Floating licenses require the additional ALDEC-USBKEY product.*

Diamond Key New Features

Design Exploration

Projects / Implementations/ Strategies

Diamond allows more robust projects and offers new capabilities for improved design exploration. Key features include:

- **Mixing of Verilog, VHDL, EDIF, and schematic sources**
- **Implementations allow multiple versions of a design within a single project for easy design exploration**
- **Strategies allow implementation "recipes" to be applied to any implementation within a project or shared between projects**
- **Manage and choose files for constraints, timing analysis, power calculation, and hardware debug**
- **Use Run Manager view for parallel processing of multiple implementations to explore design alternatives for the best results**

HDL Analysis Tools

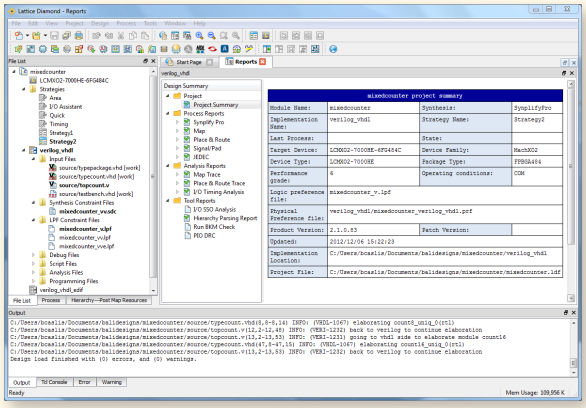
Hierarchy view automatically parses and displays the design structure and provides several features:

- **Displays post-synthesis and post-map design resources**
- **Displays and opens source files for each hierarchy level**
- **Options for hierarchy control, test bench generation, and symbol generation**

The HDL Diagram tool shows a graphical display of the design structure and provides BKM (Best Known Methods) rule checks.

Synthesis Options

In addition to Synplify Pro for all devices, for MachXO2™ and MachXO™ devices the Lattice Synthesis Engine (LSE) is also available for exploring how to achieve the best results. LSE supports both Verilog and VHDL languages and uses the Synopsys Design Compiler Constraints format for constraints.



Diamond Environment for Design Exploration

Ease of Use

GUI for a New Generation of Tools

The Diamond user interface combines leading edge features and customization while offering improved ease of use. All tools open in "Views" integrated into a common user interface. Once the operation for a single tool is learned, this knowledge can be applied to other tools.

Key GUI Elements

- **Common menu and button locations for all views**
- **Three user interface sections for tools, projects, and output**
- **Start Page – Open projects, import ispLEVER projects, online help, software updates**
- **Report View – Centralized location for all reports from implementation tools**

Speed Common Functions with ECO Editor & Programmer

- **ECO Editor provides quick access to commonly used physical netlist editing functions without using the EPIC full editor**
- **Programmer allows fast programming of FPGAs**
- **Deployment Tool creates a device programming file format for the user's deployment method**

Improved Design Flow

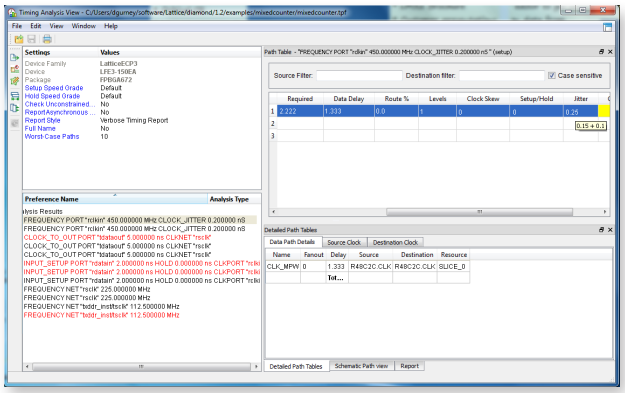
Fast, Easy Timing Analysis

Timing Analysis view offers an easy-to-use graphical environment for navigating timing information.

- **Click on a constraint and see the timing paths, detailed paths, and path schematic views instantly**
- **Easy visual cues provide instant design feedback**
- **Rapidly updated analysis when timing constraints are changed**
- **Add clock jitter analysis to improve the robustness of your design**

Scripting with Tcl

- **Tcl command dictionaries for projects, netlists, HDL code checking, power calculation, and hardware debug**
- **In addition to the Tcl console in the Diamond environment, a separate Tcl console application allows running scripts independently**



Diamond Timing Analysis View

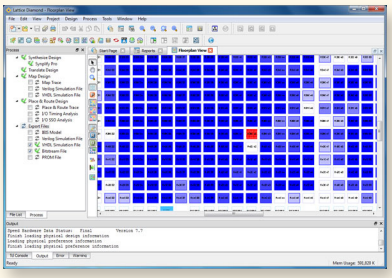
Easy Export to Simulators

The new Simulation Wizard guides you through all the necessary steps to get your design to Aldec or ModelSim simulators in the format you choose.

Improved Features

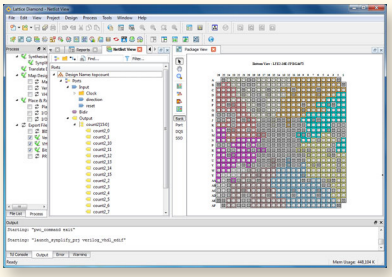
Feature	Description
Power Calculator	• Uses highly accurate data models and a data-driven power model • Provides power estimation and calculation results, graphical power displays, and reports • In addition, Power Estimator is a stand-alone tool that provides power estimation
Spreadsheet View	• Enter and view design constraints (pin assignments, clock resource usage, global preferences, timing preferences, and more) • Checks pin assignments real-time or on-demand
Package View	• Easy graphical assignment of signals to pins • Graphical representation of SSO noise analysis
Floorplanning Tasks	• Floorplan View – View design placement and edit placement constraints • Physical View – Detailed view of physical routing of paths to understand timing issues • Netlist View – Browse design ports, instances, and nets. Drag and drop into other views to set constraints. • NCD View – Detailed usage information of physical components • Device View – View device resources and edit placement constraints
Lattice Synthesis Engine (LSE)	• Supports MachXO2 and MachXO device families • Supports both Verilog and VHDL languages and uses Synopsys Design Compiler Constraints (SDC) format for constraints.
Reveal Hardware Debugger	• Easy insertion of embedded logic analyzer debug hardware for real-time analysis • New streamlined Reveal Analyzer module with multiple cursors and rubber banding for measuring events in the waveform display
IPexpress	• The interface to the catalog of modules and intellectual property (IP) optimized for Lattice devices • Import a reference file for each module or IP to easily incorporate the changes resulting from regenerating a module or IP
Programmer	• Comprehensive device programming manager • Efficiently programs Lattice devices using JEDEC and bitstream files generated by Lattice software
Deployment Tool	• Creates various device programming file formats for testers, embedded systems or external memories
Synopsys Synplify Pro for Lattice Synthesis	• Automatically produce an RTL schematic of your design • Cross-probe with RTL source code • Mixed VHDL and Verilog synthesis support • Compile points • Automatic re-timing (balancing registers across combinatorial logic) • Automatic gated-clock and generated-clock conversion for efficient implementation of RTL written for an ASIC into an FPGA
Aldec Active-HDL Simulation	• Mixed language simulation of VHDL and Verilog (Aldec Active-HDL Lattice Edition II only) • Language Assistant • Code Execution Tracing • Advanced Breakpoint Management • Memory Viewing

Floorplan View



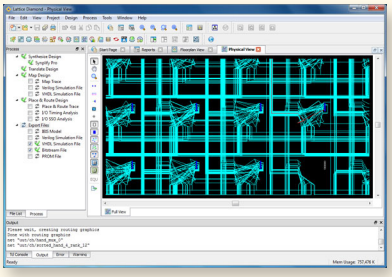
Floorplan View provides the ability to view design placement and edit placement constraints.

Package View



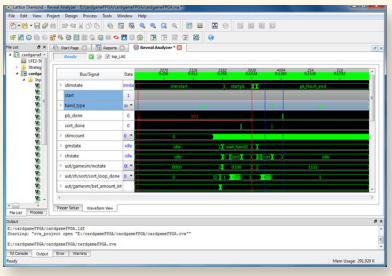
Easy graphical assignment of signals to pins and a graphical representation of SSO noise analysis.

Physical View



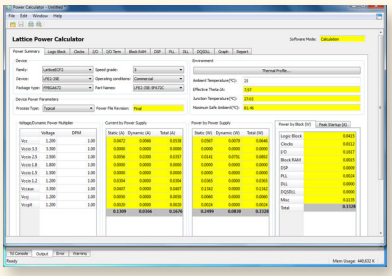
A detailed, read-only view of the physical routing of paths for a more detailed understanding of timing issues.

Reveal Hardware Debugger



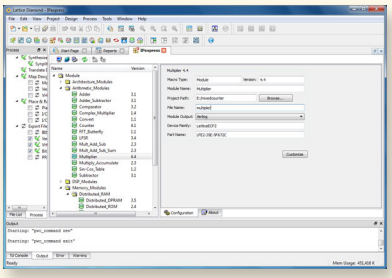
The Reveal Hardware Debugger uses a signal-centric model that allows easy insertion of embedded logic analyzer debug hardware for real-time analysis.

Power Calculator



The data driven approach of Power Calculator provides very accurate results for both power estimation and calculation.

IPexpress



An interface to the Lattice catalog of modules and IP optimized for Lattice devices.

Diamond Software Configuration Summary

	Lattice Diamond Free License	Lattice Diamond Subscription License
Lattice Device Support		
LatticeECP3, LatticeECP2M/S, LatticeSC™, LatticeSCM™, LatticeECP2/S		✔
MachXO2, MachXO, LatticeECP™, LatticeEC™, LatticeXP™, LatticeXP2, LatticeECP2	✔	✔
Key Software Features		
Complete Diamond Software Environment	✔	✔
Third-Party Software		
Synopsys Synplify Pro	✔	✔
Aldec Active-HDL Lattice Edition II	✔	✔
Operating Systems		
Windows 7 (64-bit app for 64-bit OS, 32-bit app for 32-bit OS) – Vista and XP (32-bit app for 32-bit OS)	✔	✔
Linux (64-bit app for 64-bit OS, 32-bit app for 32-bit OS) – REHL 6, 5 and 4; Novell SUSE 10	✔	✔
Licensing and Ordering		
License Terms	1 Year Nodelocked Only, Renewable	1 Year Subscription, Nodelocked or Floating
Ordering Part Number	N/A	DIAMOND-E-12M

Related Products

Product	Description	Ordering Part Number
Diamond DVD Media Backup	Diamond software on DVD media. This is media only and does not include a Diamond license.	DIAMOND-I-12M
USB Key for Aldec Simulation Floating License	Required to use Aldec simulation with a floating license. Existing USB keys from ispLEVER can also be used with Diamond software.	ALDEC-USBKEY
Download Cable (1.2V to 5V USB Programming Cable)	USB programming cable	HW-USBN-2A
Download Cable (1.8V to 5V Parallel Port Programming Cable)	Parallel port programming cable	HW-DLN-3C

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