LatticeECP3™ Serial Protocol Board – Revision D

User's Guide

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Revision: EB44_01.3

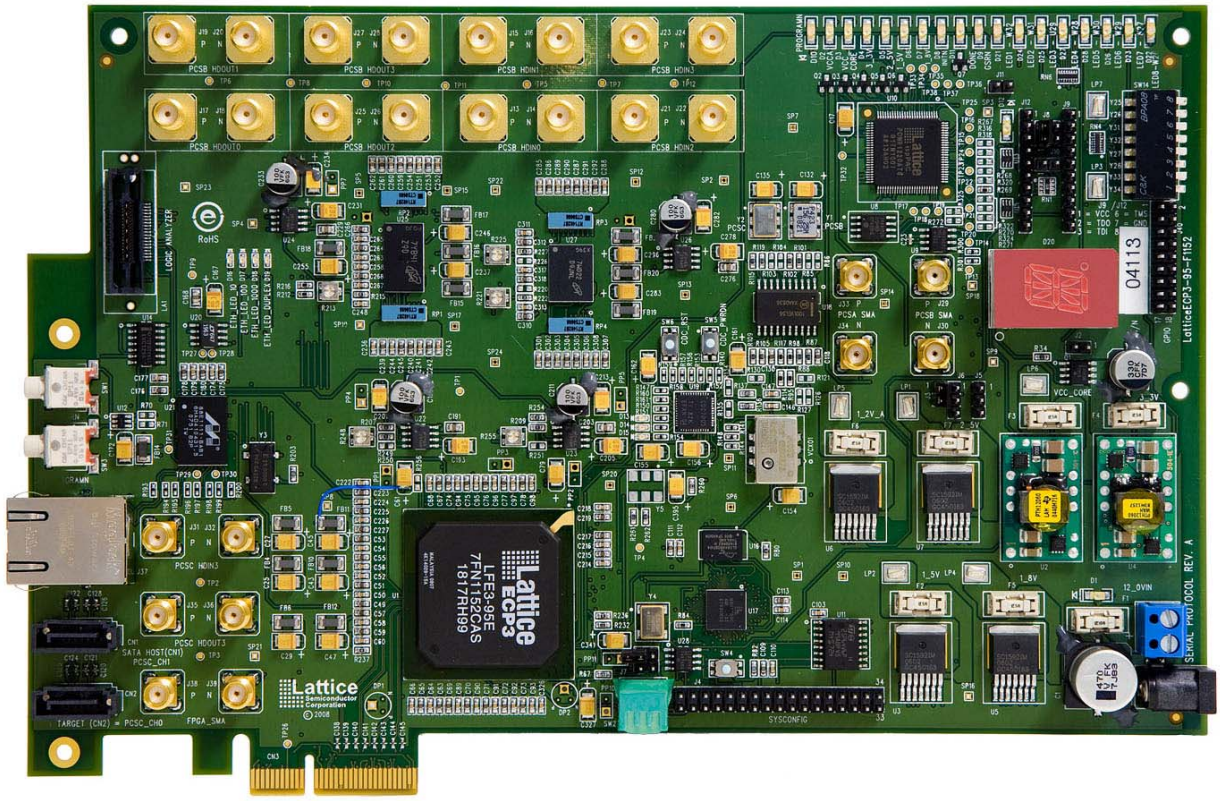
Introduction

The LatticeECP3 Serial Protocol Board (referred to in this document as "SPB") allows designers to investigate and experiment with the features of the LatticeECP3 high-speed SERDES transceivers. The SPB is available for full and detailed characterization of the high speed I/O channels and includes interfaces for some of the latest protocol interconnections.

The features of the LatticeECP3 Serial Protocol Board can assist engineers with rapid-prototyping and testing their specific designs. The board is an enhanced form-factor of the PCI Express add-in card specification. It allows for x4 PCI Express interconnection that is available for demonstration purposes with some non-standard form-factor issues. The board has several debugging and analyzing features for complete evaluation of the LatticeECP3 device. This guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeECP3 FPGA.

The evaluation board includes provisioning to connect high-speed SERDES channels via SMA connectors to test and measurement equipment. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces.

Figure 1. LatticeECP3 Serial Protocol Board



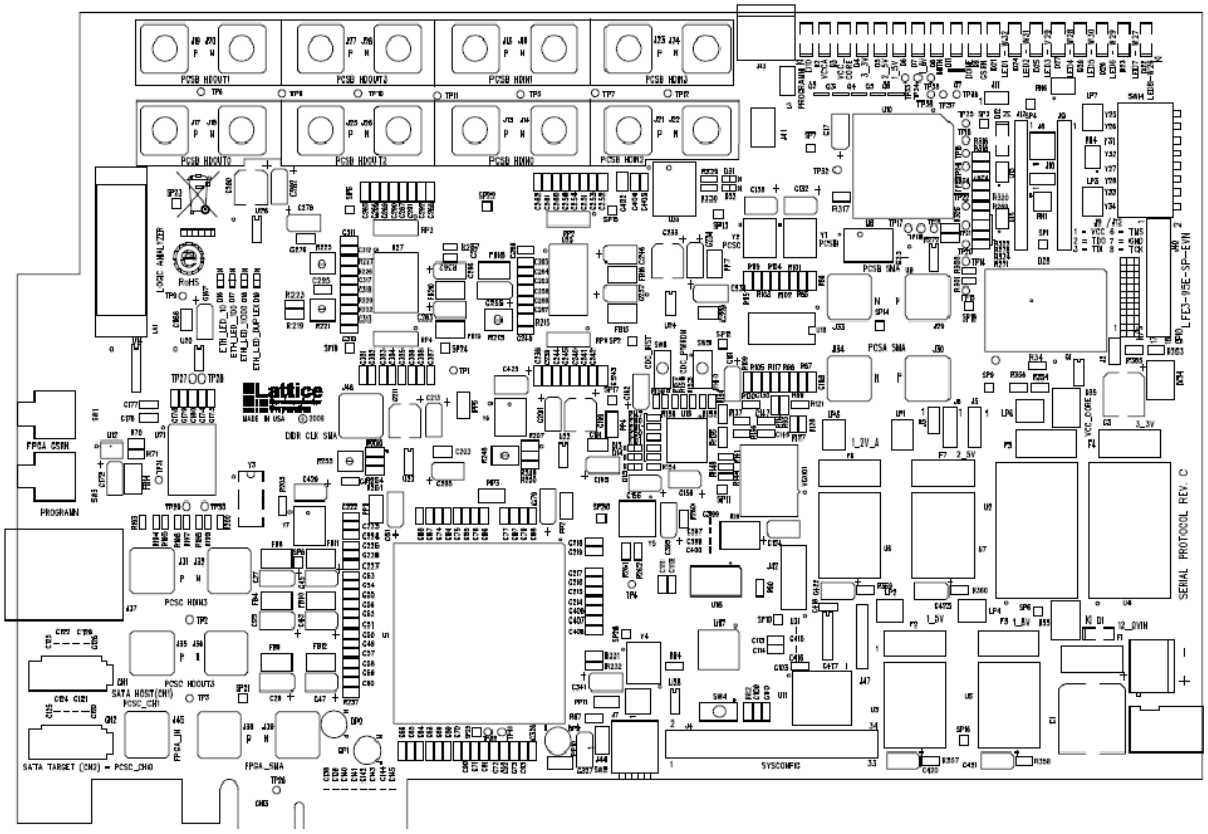
Board Features

- PCI Express x4 edge connector interfaces
  - Allow demonstration of PCI Express (x4) interfaces
  - x4 is non-compliant but will demonstrate x4 functionality with an open-frame motherboard
- Allow control of SERDES PCS registers using the Serial Client Interface (ORCAstra)
- Serial ATA interfaces for host and target configurations

- RJ45 interface to 10/100/1000 Ethernet
- On-board Boot Flash.
  - 64M Serial SPI Flash
  - Parallel Flash via MachXO™ Crossover PLD programming bridge
- Switches, LEDs, displays for demo purposes
- Several debug and analysis connections
- Input connection for lab-power supply
- Power connections and power sources
- ispVM™ programming support
- On-board and external reference clock sources

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board.

Figure 2. Serial Protocol Board Outline Drawing



LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeECP3 devices in the 1156-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP3 Family Data Sheet.

Note: The connections referenced in this document refer to the LFE3-95E-FF1156 device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeECP3 Serial Protocol Board is ready to power on. The board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or, it can be supplied from an benchtop supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J1 and plug wall-transformer into an AC wall outlet.

Power Supplies

(see Appendix A, Figure 20)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided to use with a benchtop supply adjusted to provide a nominal +12V DC. An indicator (D1) will illuminate when 12V is applied to the board.

All input power sources and on-board power supplies are fused with surface mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies.

Table 1. Board Power Supply Fuses and Indicators LEDs (see Appendix A, Figure 20)

Fuse Designator	Function	Power Good LED Designator	Function
F1	12V Input Supply Fuse	D1	12V Input Good Indicator
F2	1.5V Fuse	D6	1.5V Good Indicator
F3	1.2V Core Fuse	D3	1.2V Core Good Indicator
F4	3.3V Fuse	D4	3.3V Good Indicator
F5	1.8V Fuse	D7	1.8V Good Indicator
F6	1.2V Analog Supply	D2	1.2V VCCA Good Indicator
F7	2.5V Fuse	D5	2.5V Good Indicator

Power can be supplied with either a wall transformer pack, or another external source.

Table 2. External Board Supply Input Terminal (see Appendix A, Figure 20)

TB1	Screw terminal for 12V DC Pin 1(square PCB pad) -> +12V DC Pin 2 -> Ground

The above-mentioned supplies can be isolated from the on-board regulators by removal of the associated fuse. Surface-mounted test loops are provided to apply alternative power sources to these supplies as required for testing purposes.

Table 3. Power Supply Test Connections

Test Point Designator	Supply
LP1	2.5V
LP2	1.5V
LP3	3.3V
LP4	1.8V
LP5	1.2V VCCA
LP6	1.2V VCC Core

PCI Express Power Interface

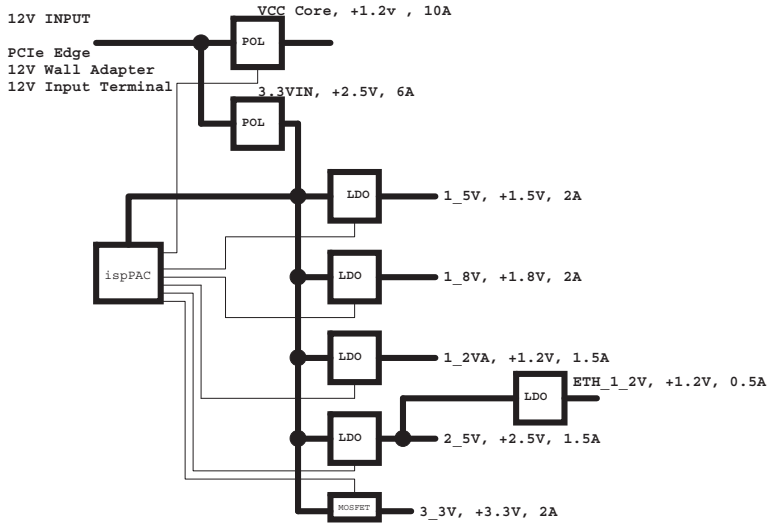
Power can be sourced to the board via the PCB edge fingers (CN1). This interface allows the user to provide power from a PCI Express host board.

Power Management

The evaluation board includes a Lattice ispPAC®-POWR1220AT8 programmable power management IC (U10). This device controls the power sequence and monitors designated board supplies. The POWER GOOD indication LEDS are controlled via this device.

The power management device is factory programmed to control the power supplies. A block diagram of the power management is shown in Figure 3.

Figure 3. Power Management Block Diagram



Programming/FPGA Configuration

(see Appendix A, Figure 23)

A programming header is provided on the evaluation board, providing access to the LatticeECP3 JTAG port.

Note: An ispDOWNLOAD™ Cable is included with each ispLEVER®-Base or ispLEVER-Advanced design tool shipment. Cables may also be purchased separately from Lattice.

ispVM Download Interface

J12 is an 10-pin JTAG connector used in conjunction with the ispVM USB download cable to program and control the device.

Table 4. Standard ispVM Programming Cable Configuration

Pin	Description
Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	PROGRAMN[1]
Pin 5	Enable used for alternate programming of the ispPAC-POWR1220AT8 device
Pin 6	TMS
Pin 7	GND
Pin 8	TCK
Pin 9	DONE[1]
Pin 10	INITN[1]

1. Denotes optional connection to programming cable.

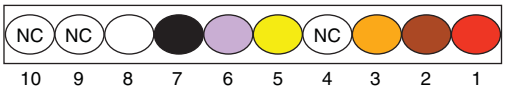
After initial board setup, use the following procedure to program the evaluation board.

Instructions assume ispVM software has been installed on a local PC.

Connect the ispDOWNLOAD cable rainbow-colored flywires to the connector J12.

Pin 1 = red, 2 = brown, 3 = orange, 4 = open, 5 = open, 6 = purple, 7 = black, 8 = white, 9 = open, 10 = open.

Table 5. ispVM JTAG Connector (see Appendix A, Figure 23)



Pin	Function	Color
1	PWR	Red
2	TDO	Brown
3	TDI	Orange
5	ISPEN	Yellow[1]
6	TMS	Purple
7	GND	Black
8	TCK	White

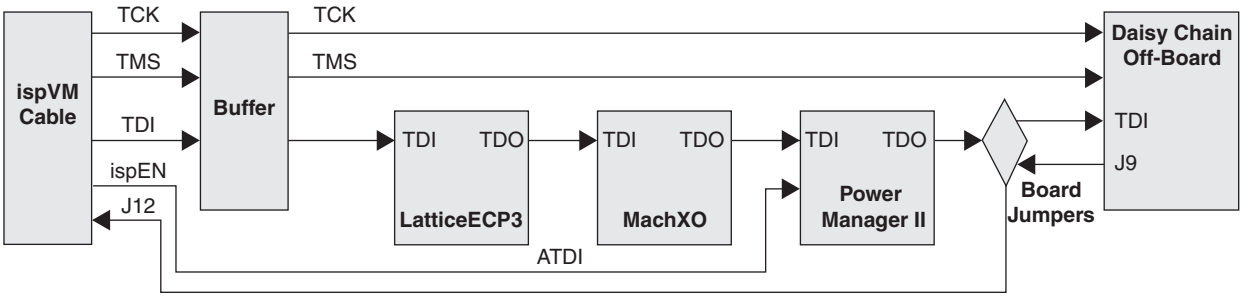
1. Only connected for programming the ispPAC-POWR1220AT8 device.

Programming the Daisy Chain

(see Appendix A, Figure 23)

This board includes three Lattice programmable (U1=LFE395, U17= LCMXO1200C, and U13 = POWR1220AT8) devices that can be programmed in a daisy chain. The board also includes a mechanism to daisy chain other Lattice evaluation boards that use the same connector standard.

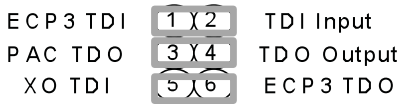
Figure 4. JTAG Chain



An alternative chain can be used when it is desired to only communicate with the ispPAC-POWR1220AT8 device. This alternative method utilizes the ispEN pin to drive the TDISEL input. A logic "1 "driven on the TDISEL of the ispPAC-POWR1220AT8 will enable the ATDI input ignoring the TDI data of the board JTAG chain and receiving TDI data directly from the ispVM input.

A 2x3 header(J41) completes the on-board JTAG chain between the LatticeECP3 FPGA, the MachXO1200 CPLD and the ispPAC-POWR1220 devices. These jumpers must be in place for proper operation with ispVM.

Figure 5. ALL Devices in Chain Selection (J41)



JTAG daisy-chaining across multiple boards is provisioned on board by jumpers. Header J8 controls the data path to and from the evaluation board TDO. The board is factory programmed with a jumper across pins 1 and 2 of J8. If the user needs to build a JTAG daisy-chain to another Lattice evaluation board the user needs to place jumpers between pins 1 and 3 and 2 and 4 respectively. This will alter the data path off-board via J9, which typically can be connected to another ispVM connector of a Lattice Semiconductor evaluation board. J10 and J11 can also be used for off-board daisy-chaining to wire AND the PROGRAMN and INITN pin respectively between the boards.

Download Procedure

Requirements:

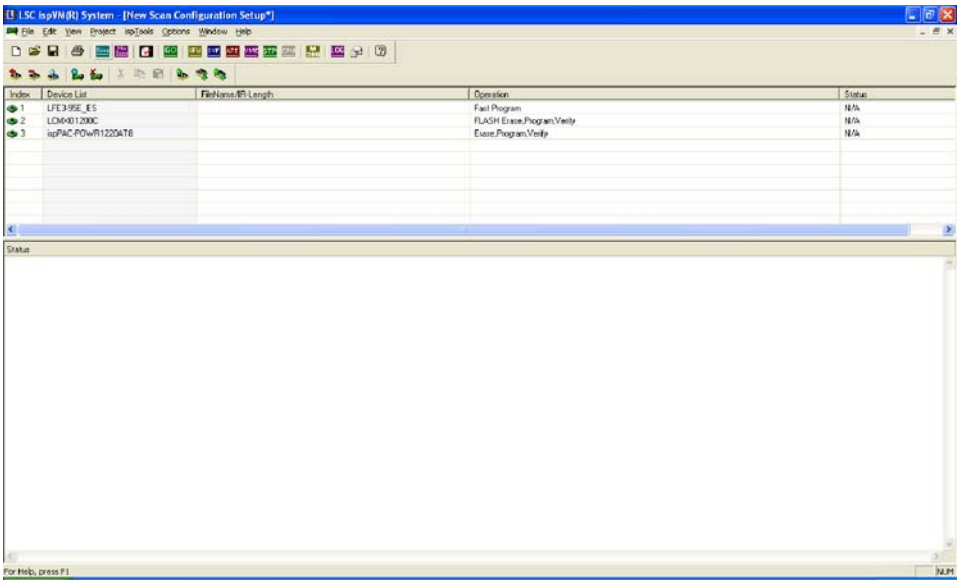
- PC with ispVM System v.17.4 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). *Note: An option to install these drivers is included as part of the ispVM System setup.*
- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

JTAG Download

The LatticeECP3 device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

1. Connect the LatticeECP3 Serial Protocol Board to the appropriate power sources and power up board.
2. Connect the ispDOWNLOAD cable to the appropriate header. J12 is used for the 1x10 cable.
3. Start the ispVM System software.
4. Press the **SCAN** button located in the toolbar. The LatticeECP3 and the MachXO1200 devices will be automatically detected.

Figure 6. Main Downloading Window



5. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.

6. Add the data file from the **Browse** dialog and select **OK** when complete.

7. To program only the LatticeECP3-95, place the LCMXO1200C and the ispPAC-POWR1220AT8 devices into BYPASS and the LFE3-95 into Erase, Program, Verify mode, as shown below.

Figure 7. Device Information Window

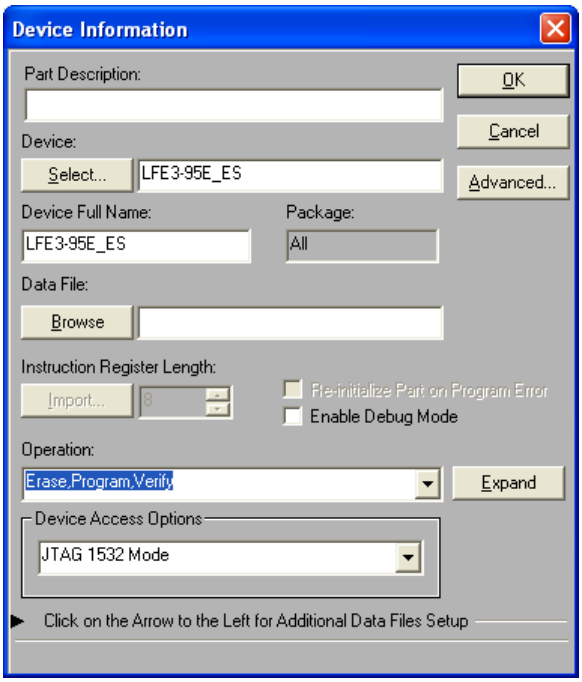
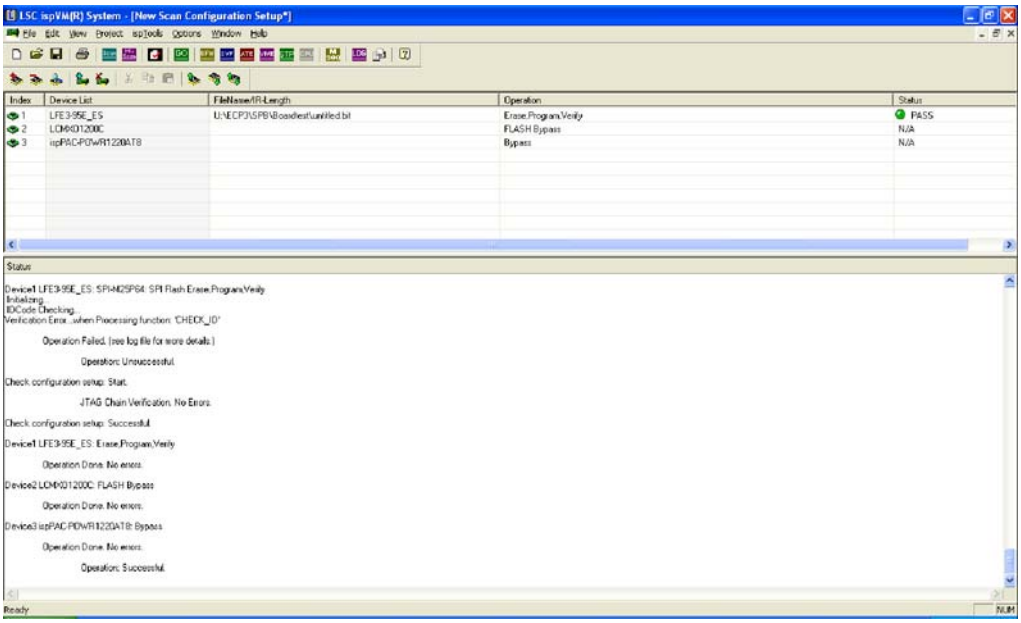


Figure 8. Successful Programming Session



8. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

Programming the Power Manager Device

The J12 header can be used to isolate and program the ispPAC-POWR1220AT8 Power Manager device. This device can be isolated from the others on the chain using the optional ispEN connection from the ispVM programming cable. Connecting ispEN to pin 5 on J12 and selecting the optional control in ispVM will isolate the Power Manager. The connection is activated from the **Options** pull-down menu of the ispVM toolbar. The Cable and I/O Port Setup dialog box is used to select the polarity of this connection to SET LOW.

Figure 9. Setup for ISPEN Usage

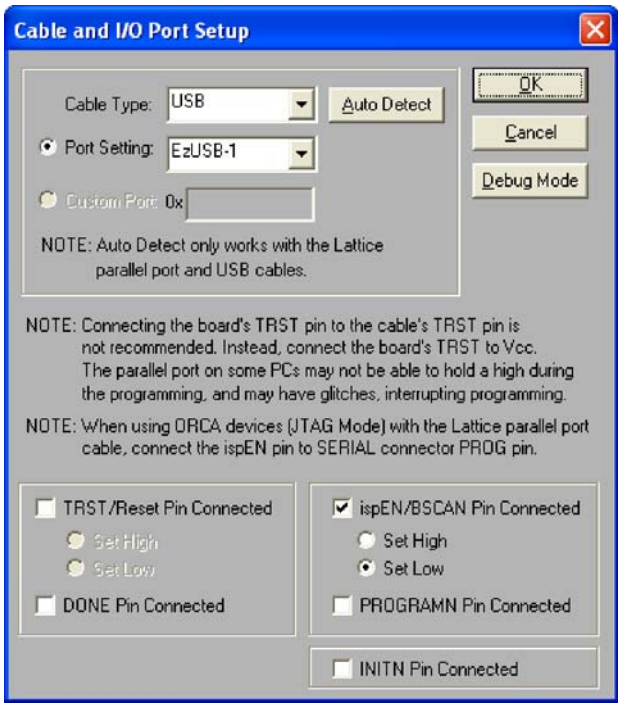
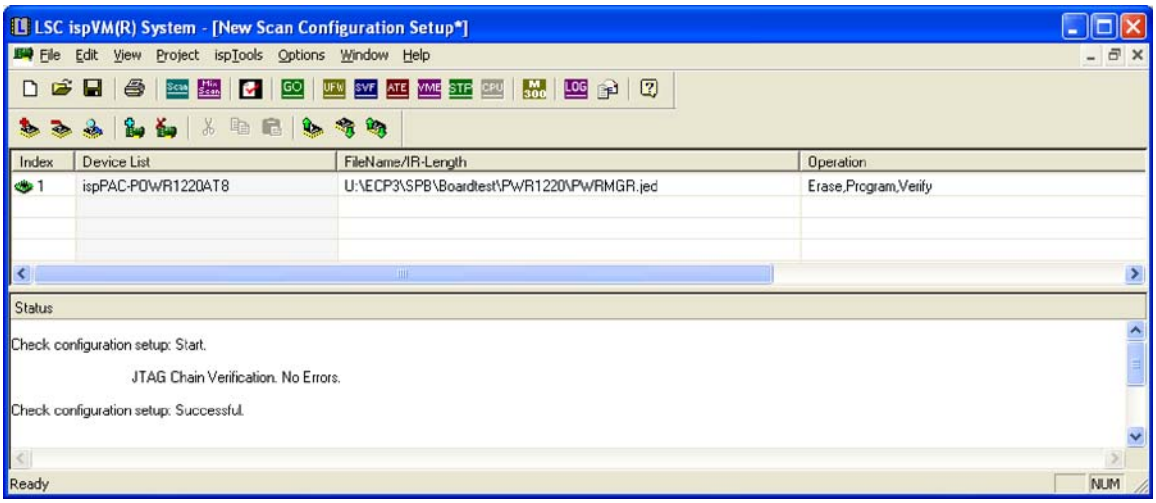


Figure 10. Programming of ispPAC-POWR1220AT8 Power Manager Device



Note: The ispEN connection must be disconnected for complete programming of the other devices on the SPB.

Configuration Status Indicators

(see Appendix A, Figure 23)

These LEDs indicate the status of configuration to the FPGA.

- D8 (red) illuminated, this indicates that the programming was aborted or reinitialized driving the INITN output low.
- D11 (green) illuminated, this indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D12 (green) will flash indicating TDI activity.

- D10 (red) illuminated, this indicates that PROGRAMN is low.
- D9 (red) illuminated, this indicates that GSRN is low.

PROGRAMN and GSRN

(see Appendix A, Figure 23)

- These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3) and GSRN (SW1). Depressing the button drives a logic level "0" to the device.

CFG [2:0]

(see Appendix A, Figure 23)

- The FPGA CFG pins are set on the board for a particular programming mode via the SW2 DIP switch.
- JTAG programming is independent of the MODE pins and is always available to the user.
- Pushing in (depressing) the switch is ON and sets the value to 0.

Table 6. CFG Mode Selections

CFG2	CFG1	CFG0	Configuration Mode
0(ON)	0(ON)	0(ON)	SPI Flash
0(ON)	1(OFF)	0(ON)	SPIm
1(OFF)	0(ON)	1(OFF)	Slave Serial
1(OFF)	1(OFF)	1(OFF)	Slave Parallel
X (don't care)	X (don't care)	X (don't care)	ispJTAG

On-Board Serial SPI Flash Memory

(see Appendix A, Figure 23)

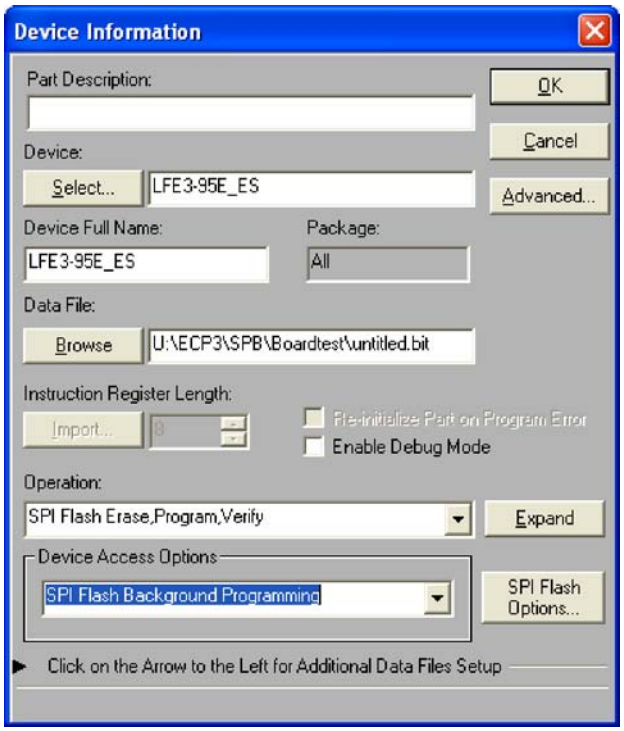
- One Serial SPI (16-pin TSSOP 64M) Flash memory devices (U11) is on-board for non-volatile configuration memory storage. Either a STMicro M25P64VMF16 or Macronix MX25L6405 device is populated on-board.
- The CFG [2:0] need to be [000] all depressed to read the Flash memory at power-up or after toggling the PROGRAMN pin.
- J11 must have a jumper between pins 1 and 2.

Programming Serial SPI Flash Memory

The Serial SPI Flash memory device can be configured easily via its JTAG port. This mode enables the FPGA to be programmed at power-up or assertion of PROGRAMN with a bitstream stored in the memory device.

1. Connect the evaluation board to the appropriate power sources and power up board.
2. Connect the ispDOWNLOAD cable to the appropriate header. J9 is used for the 1x10 cable.
3. Start the ispVM System software.
4. Press the **Scan** button located in the toolbar. The LFE3-9, LCMXO1200C and ispPOWR1220AT8 devices will be automatically detected.
5. Double-click the **Operation** column for the LFE3-95 and the Device Dialog box shown below will open.
6. In the dialog box select the **SPI Flash Programming Mode** in the Device Access Option pull-down menu. This will open the SPI Serial Flash Dialog box.

Figure 11. Device Information Dialog Screen



7. The SPI Serial Flash Device dialog box will open. In this box select **SPI Flash Erase, Program, Verify** in the **Operation** pull-down menu.

8. Select **SPI Serial Flash** in the **Device Family** pull-down menu, **STMicro** under the **Vendor** pull-down menu, **SPI-M2564** under the **Device** pull-down menu, and **16-lead SOIC** under the **Package** submenu.

Figure 12. Select Device Dialog Box

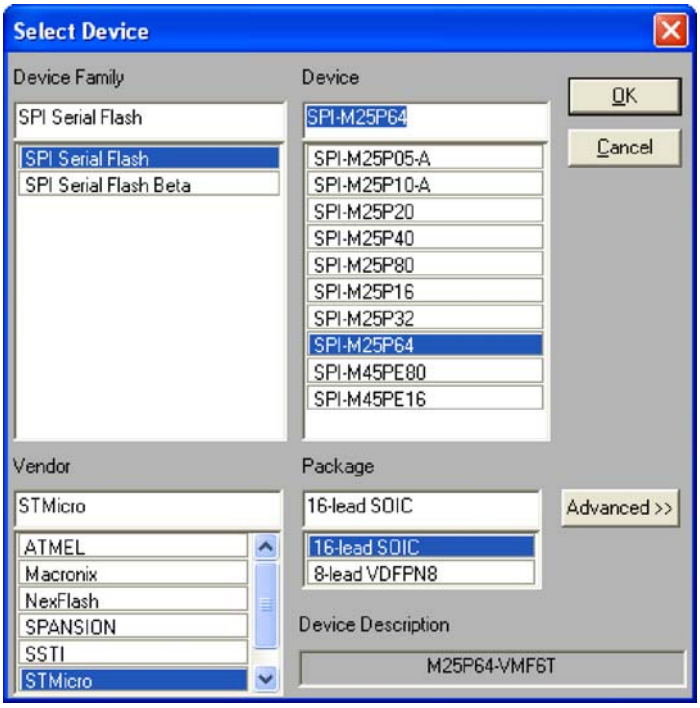
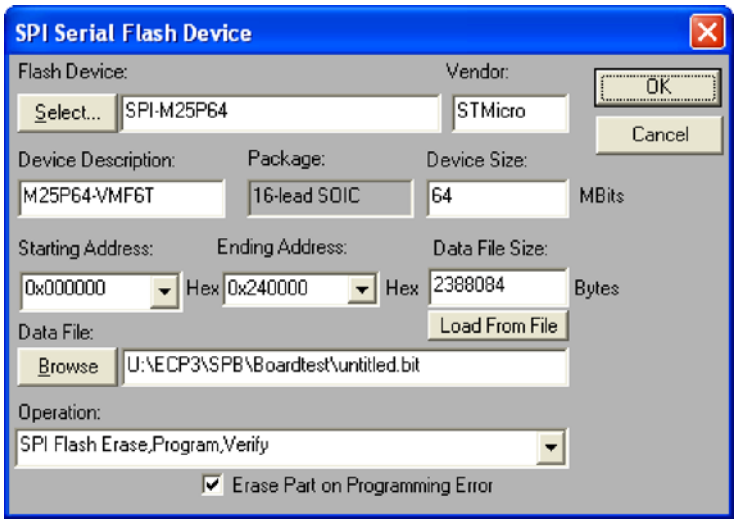
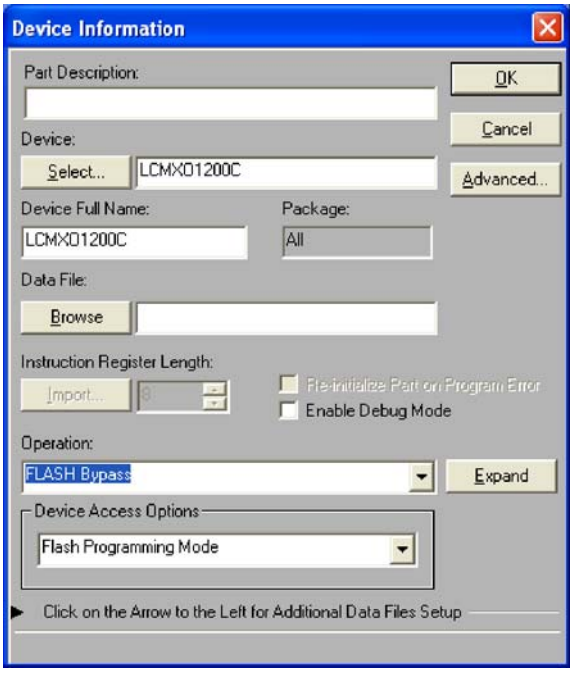


Figure 13. Sample SPI Serial Flash Device Dialog Box



9. Click **OK** in the SPI Flash Device Dialog box. Then click **OK** in Select Device dialog box. You will then return to the main configuration screen. If you do not desire to load the LCMXO1200C and the ispPOWR1220 device, these devices should be placed in Flash Bypass mode by double-clicking the **Operation** column and selecting the Bypass operation shown below.

Figure 14. Flash Bypass for LCMXO1200C Device



10. From the main programming window, Select **Go** for the top toolbar. This will begin the SPI Serial Flash programming.

Figure 15. Programming Main Window

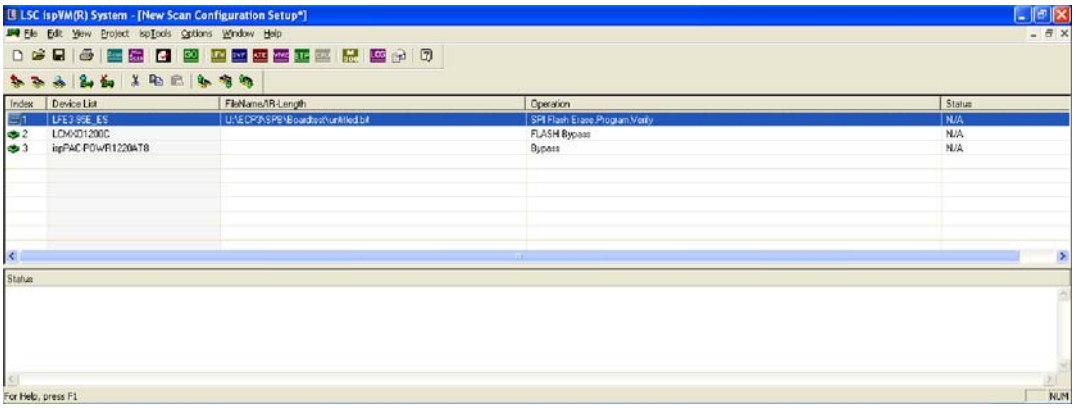
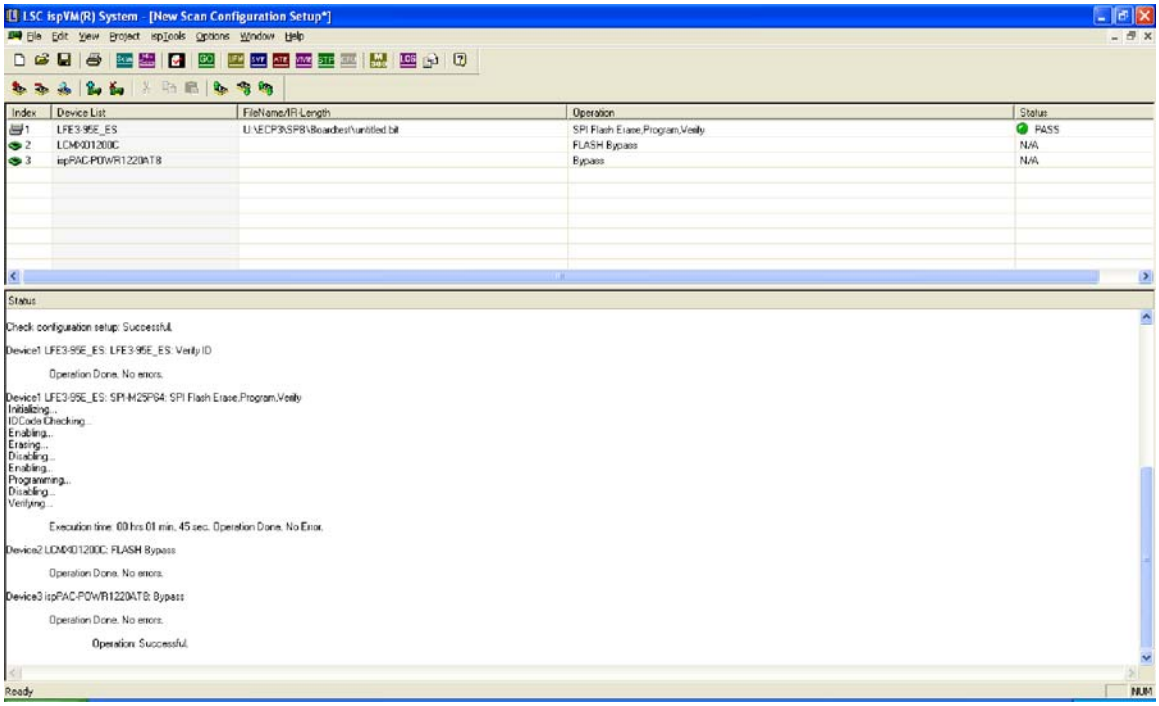


Figure 16. SPI Serial Flash Programming Status Window

Figure 17. Successful SPI Serial Flash Programming Session



On-Board Parallel SPI Flash Memory

(see Appendix A, Figure 25)

- A 16-bit parallel Flash device is also available. This board uses a Lattice MachXO Crossover PLD to act as a programming bridge from the Flash device.
- The CFG [2:0] needs to be [111] all up.
- The ispVM System programming software can be used directly to program either the serial SPI Flash or the par-

allel Flash devices. Application note AN8077, Parallel Flash Programming and FPGA Configuration, addresses the use of the parallel Flash implementation.

On-Board Clock Capabilities

Dedicated SERDES Reference Clock Inputs

(see Appendix A, Figure 26)

- A 156.25 MHz, low-jitter (5x7.5mm surface mount) oscillator is included on-board.
  - Connected via clock mux to PCSB_REFCLK
  - Clock control CLOCK_CTRL_SEL0 is connected to both the FPGA (ball #A25) or the Crossover PLD (ball #N6). Either of these sources selects the clock source of Y1 oscillator or J29 and J33 SMA inputs.
- A 125.00 MHz, low-jitter (5x7.5mm surface mount) oscillator is included on-board.
  - Connected via clock mux to PCSC_REFCLK
  - Clock control CLOCK_CTRL_SEL1 is connected to both the FPGA (ball #B25) or the Crossover PLD (ball #M14). Either of these sources selects the clock source of Y2 oscillator or J30 and J34 SMA inputs.

***SMA connections J29 and J33 can provide an external clock source to PCSB. J29 is the true and J33 is the compliment of the differential pair. The description markings on the evaluation board are incorrect.

***SMA connections J30 and J34 can provide an external clock source to PCSC. J30 is the true and J34 is the compliment of the differential pair. The description markings on the evaluation board are incorrect.

User Defined General Purpose Clock Oscillator

(see Appendix A, Figure 31)

A 100 MHz oscillator is included on the board. It is fanned-out to several destinations on the board. They include the following. This oscillator is used for general clocking and should be avoided for jitter sensitive applications.

Table 7. 100 MHz Clock Destinations

Clock Destination	Evaluation Board Designation	Destination Pin
Crossover PLD	U17	A8
FPGA	U1	B6
FPGA	U1	H17-PCLKT0
FPGA	U1	P30-RUM2_GPLLT_IN_A

(see Appendix A, Figure 33)

An auxiliary SMT oscillator area is included on the board. It includes a 5x7.5mm surface-mount pad for the addition of any user-defined oscillator. This oscillator interconnects to FPGA ball numbers AB28 and AB29 that are specifically general purpose PLL inputs to the FPGA fabric.

(see Appendix A, Figure 33)

SMA inputs J38 and J39 are provided to drive any externally generated differential clock onto the board. These 50-ohm terminated SMAs interconnect to FPGA ball numbers U28 and V28 that are specifically PCLKT3_0 and PCLKC3_0 inputs to the FPGA fabric.

SERDES

Surface Mounted SMA Connections

(see Appendix A, Figure 26)

DC coupled top-mounted SMA connectors connect to the one quad or four SERDES Tx and Rx channels. These pins are directly coupled to the designated SMA connector creating a path for both input and output differential data.

Table 8. SERDES SMA Test Connectors

Connector	SERDES Signal	FPGA Pin
J13	PCSB_HDINP0	AL17
J14	PCSB_HDINN0	AK17
J15	PCSB_HDINP1	AL16
J16	PCSB_HDINN1	AK16
J17	PCSB_HDINP2	AL15
J18	PCSB_HDINN2	AK15
J19	PCSB_HDINP3	AL14
J20	PCSB_HDINN3	AK14

Connector	SERDES Signal	FPGA Pin
J21	PCSB_HDOUTP0	AP17
J22	PCSB_HDOUTN0	AN17
J23	PCSB_HDOUTP1	AP16
J24	PCSB_HDOUTN1	AN16
J25	PCSB_HDOUTP2	AP15
J26	PCSB_HDOUTN2	AN15
J27	PCSB_HDOUTP3	AP14
J28	PCSB_HDOUTN3	AN14

Serial ATA Channels

(see Appendix A, Figure 26)

High-speed connections are included to attach SATA-type cables to SERDES channels for board-to-board or loop-back purposes. The connectors are configured using the 7-pin SATA specifications.

Figure 18. SATA Connector, Molex Part Number 67800-5050

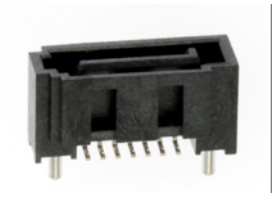


Table 9. SERDES to SATA Connections

Host		
CN1 Pin	SERDES Pin	FPGA Ball #
1	—	GND
2	PCSC_HDOUTP1	AP24
3	PCSC_HDOUTN1	AN24
4	—	GND
5	PCSC_HDINP1	AL24
6	PCSC_HDINN1	AK24
7	—	GND

Target		
CN2 Pin	SERDES Pin	FPGA Ball #
1	—	GND
2	PCSC_HDINP0	AL25
3	PCSC_HDINN0	AK25
4	—	GND
5	PCSC_HDOUTP0	AP25
6	PCSC_HDOUTN0	AN25
7	—	GND

SERDES PCI Express Channels

(see Appendix A, Figure 26)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge fingers (CN3) to fit directly into a PCI Express host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections.

Table 10. x4 PCI Express Connections

CML Pin Name	FPGA Pin	PCI Express	PCI Express Edge	Description
PCSA_HDOUTP_3	AP18	PERp0	A16	Integrated end point block transmit pair
PCSA_HDOUTN_3	AN18	PERn0	A17	
PCSA_HDINP_3	AL18	PETp0	B14	Integrated end point block receive pair
PCSA_HDINN_3	AK18	PETn0	B15	
PCSA_HDOUTP_2	AP19	PERp1	A21	Integrated end point block transmit pair
PCSA_HDOUTN_2	AN19	PERn1	A22	
PCSA_HDINP_2	AL19	PETp1	B19	Integrated end point block receive pair
PCSA_HDINN_2	AK19	PETn1	B20	
PCSA_HDOUTP_1	AP20	PERp2	A25	Integrated end point block transmit pair
PCSA_HDOUTN_1	AN20	PERn2	A26	
PCSA_HDINP_1	AL20	PETp2	B23	Integrated end point block receive pair
PCSA_HDINN_1	AK20	PETn2	B24	
PCSA_HDOUTP_0	AP21	PERp3	A29	Integrated End point block transmit pair
PCSA_HDOUTN_0	AN21	PERn3	A30	
PCSA_HDINP_0	AL21	PETp3	B27	Integrated End point block receive pair
PCSA_HDINN_0	AK21	PETn3	B28	
PCSA_REFCLKP	AH19	PCIe_CLKp	A13	Integrated End point block differential clock pair
PCSA_REFCLKN	AH20	PCIe_CLKn	A14	
PCIE_PERSETN	D23	PERSTN	A11	Fundamental PCI Express reset

External SERDES Reference Clock Cleaner

(see Appendix A, Figure 27)

The Texas Instruments CDC7005 is a high-performance, low-phase noise, and low-skew clock synthesizer and jitter cleaner that synchronizes the voltage controlled crystal oscillator (VCXO) frequency to the reference clock. It is included on the evaluation board to demonstrate the use of an external clock cleaner as a means to reuse the SERDES recovered clock for retransmitting. The interconnection from the FPGA brings a single-ended LVCMOS clock from the SERDES to the CDC7005 input. The CDC7005 has an internal prescaler, phase frequency detector, charge pump, operational amplifier, and a LVPECL clock buffer. Along with an external VCXO and loop filter, the device completes a phase locked loop (PLL). Through the PLL operation, the VCXO input clock synchronizes with the reference clock input and ultimately with all clock outputs. All LVPECL clock outputs are completely synchronized in terms of phase and frequency with the reference clock input.

Table 11. Reference Clock Interconnections

CDC7005 Outputs		1156 fpBGA Inputs		Notes
Y0/Y0b	P46/P47	PCSB_REFCLKP/N	AH15/AH16	Stuffing option R126/R127 must be fitted with 0-ohm resistors for connection to the FPGA reference clock input.
Y1/Y1b	P3/P4	RLM1_GPLLT_INA/B	Y28/Y27	
Y2/Y2b	P7/P8	RUM0_GDLLT_INA/B	AJ34/AK34	
CDC7005 Input		**1156 fpBGA Output**		
REFIN	P37	D22		LVCMOS

The jitter cleaning action depends on the PLL loop bandwidth. Up to the loop bandwidth, all noise (jitter) passes through and above the loop bandwidth, all signal noise is cleaned. The ideal loop bandwidth is chosen such that the reference clock source starts exceeding the VCXO noise floor. If the input has lot of jitter, then selecting a low

loop bandwidth, jitter can be cleaned. For the CDC7005, a low loop (sub 10 Hz) bandwidth can be selected easily. The CDC7005 itself adds a low noise to its outputs. For jitter cleaning operation, the noise performance of VCXO is critical. So, with a proper loop bandwidth and applicable VCXO, the CDC7005 acts as a jitter cleaner. The evaluation board is equipped with an Epson-Toyocom TCO2111-245.76MHZ VCXO that is packaged in a 13.9x9.8mm SMT form-factor.

Table 12. CDC7005 Control and Status Signals

CDC7005 Pin		Board Feature	Description
1	NPD	SW5	Push-button that asserts LOW when depressed to power-down CDC7005.
14	NRESET	SW6	Push-button that asserts LOW when depressed to RESET CDC7005.
22	STATUS_VCXO	D13	Amber LED - CDC7005 PLL locked when lit.
23	STATUS REF	D14	Amber LED - CDC7005 valid clock on REF_IN when lit. > 3.5 MHz.
25	STATUS LOCK	D15	Amber LED - CDC7005 valid VCXO clock on VCXO_IN when lit. > 10 MHz

The serial interface of the CDC7005 is a simple SPI-compatible interface for writing to the registers of the device. It consists of three control lines: CTRL_CLK, CTRL_DATA, and CTRL_LE. These pins from the CDC7005 are interconnected to the FPGA to allow for a controller to be built inside the FPGA.

Table 13. CDC7005 Serial Interconnections

CDC7005		1156 fpBGA Ball Number
CTRL_CLK	35	E23
CTRL_DATA	33	C23
CTRL_LE	36	E22

The TI CDC7005 can also be controlled via an interface to header J47. This header can be used in conjunction with the TI programming software required for programming the internal control register of the CDC7005. TI. The software package provides real-time GUI control to the device. The software runs under Windows98, NT, and 2000. Info can be found at www.ti.com/lit/zip/scac037.

Table 14. External Programming Interface for TI CDC7005 Clock Cleaner (See Appendix A, Figure 27)

J47 Pin	DB-25 Parallel Cable	Description
1	2	Data
2	3	CLK
3	4	LE
4	18	Enable
5	19	GND

FPGA Test Pins

(see Appendix A, Figure 31)

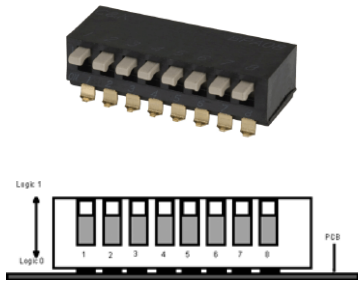
General Purpose DIP Switch

(see Appendix A, Figure 31, SW14)

General-purpose FPGA pins are available for user applications. FPGA pins are connected to a switch (SW15) that is a SPST-side actuated DIP switch. The switch is physically located on the secondary side of the board along the back-panel edge. The switches are connected to logic level 0 when depressed toward the board and a 1 when away from the board. The designated pins are connected according to the following table.

Table 15. FPGA Test Pins (See Appendix A, Figure 33)

1156 fpBGA Ball Number	SW14 Switch Position
Y34	1
Y33	2
Y30	3
AA29	4
Y32	5
Y31	6
Y26	7
Y25	8



General-Purpose LEDs

(see Appendix A, Figure 31)

The LEDs on the evaluation board are connected to general-purpose FPGA I/O. The purpose of these LEDs is to provide status for user designs. The LEDs must be included in the FPGA design.

Table 16. LED Definitions (See Appendix A, Figure 33)

Name	1156 fpBGA Ball Number	PCB Designator	LED Color
LED1	W32	D21	Red
LED2	W31	D24	Yellow
LED3	V29	D25	Green
LED4	W28	D27	Blue
LED5	W30	D28	Blue
LED6	W29	D26	Green
LED7	W27	D23	Yellow
LED8	W26	D22	Red

General-Purpose Header

(see Appendix A, Figure 31, J40)

A 2x9 header (J10) provides a general-purpose connection to communicate with general purpose FPGA I/Os.

Table 17. General Purpose Header Connections (See Appendix A, Figure 33)

Header Pin	1156 fpBGA Ball Number	Header Pin	1156 fpBGA Ball Number
1	GND	2	GND
3	A6	4	E11
5	A8	6	J13
7	A9	8	K13
9	A10	10	B11
11	B10	12	A11
13	J12	14	G12
15	K12	16	G11
17	C11	18	D11

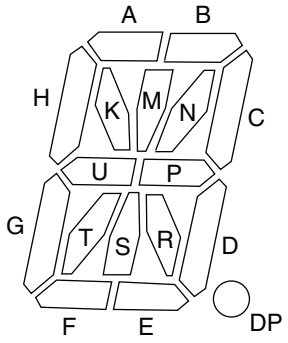
17-Segment LED Display

(see Appendix A, Figure 33, D20)

General-purpose FPGA pins are connected to a 17-segment display according to Table 18. These pins can be driven low to illuminate the display segments.

Table 18. 17-Segment LED Display

Segment	1156 fpBGA Ball Number
A	C30
B	C29
C	B31
D	A31
E	H25
F	H26
G	A30
H	A29
K	A27
M	A26
N	A28
P	B28
R	G25
S	G26
T	D25
U	C25
DP	D28



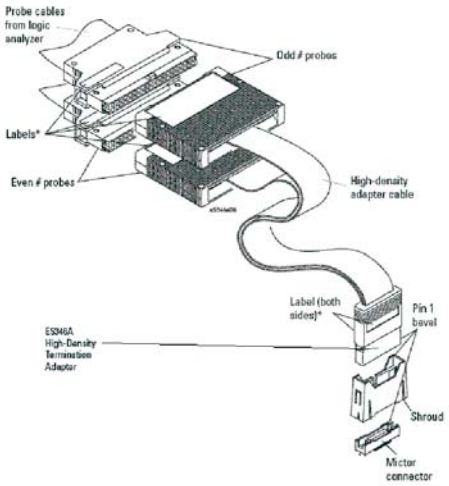
Logic Analyzer Probe

(see Appendix A, Figure 31, LA1)

An AMP/TYCO 767004 38-position .025 VERT SMD logic analyzer probe connection is provided for the user to utilize for test points. This connection provides 34 general I/O signals to be observed on Logic Analyzer probes using Mictor connections such as the Agilent 5346A.

Table 19. Logic Analyzer To FPGA Pin Reference (See Appendix A, Figure 33)

Signal	1156 fpBGA Ball #	Signal	1156 fpBGA Ball #
LA1	G13	LA2	H14
LA3	A13	LA4	B13
LA5	D10	LA6	C10
LA7	C13	LA8	D13
LA9	J15	LA10	H15
LA11	D3	LA12	C2
LA13	C14	LA14	D14
LA15	A14	LA16	B14
LA17	G16	LA18	G17
LA19	D15	LA20	E15
LA21	J16	LA22	H16
LA23	A15	LA24	B15
LA25	E17	LA26	F28
LA27	C16	LA28	D16
LA29	K16	LA30	L16
LA31	A16	LA32	B16
LA33	G18	LA34	F19



10/100/1000Base Ethernet Interface

(see Appendix A, Figure 28, U21)

The Marvell 88E1111 Gigabit Ethernet transceiver device (U21) is included on the board. This physical layer device supports 1000BASE-T, 100BASE-TX, and 10BASE-T applications via a standard Media interface to an RJ-45 (Bel Stewart "MAGJACK" p/n L829-1J1T-43) connection. The RJ-45 connection includes network magnetics providing the proper signal conditioning, electro-magnetic interference suppression and signal isolation. This connector includes two LEDs and the board includes four status LEDs from the Marvell device. The LEDs are register-programmed and detailed descriptions are included in the Marvell data sheet.

Table 20. PHY Status Indicators

LED	Status Description
RJ45- Yellow	LED RX
RJ45- Orange	LED TX
PCB Amber (D16)	LINK 10
PCB Amber (D17)	LINK 100
PCB Green (D18)	LINK 100
PCB Amber (D19)	DUPLEX

The Marvell 88E1111 device communicates via a MAC interface to the LatticeECP3 device via GMII, SGMII, and a standard 10-bit interface. The evaluation board includes the means to setup the required hardware configuration for the PHY to operate in all the supported modes. Hardware configuration options such as PHY address, PHY operating mode, auto-negotiation, and physical connection type must be set up using the configuration switches SW7 to SW13 on the back side of the board. These switches tie the CONFIG[6:0] pins to the control LED output pins. The encoded values of the LED outputs that are tied to the CONFIG[6:0] pins are latched at the de-assertion of the PHY RESETn control.

The switch matrix of the PHY CONFIG pins are described below. DIP switches control the hardware settings. *Note: Only one switch position per DIP pack should be on for any configuration.*

Table 21. PHY Hardware Configuration Switch Control (see Appendix A, Figure 29)

Switch Position	88E1111 LED Output	Bit[2:0]
1	VDDO	111
2	LED_10	110
3	LED_100	101
4	LED_1000	100
5	LED_DUPLEX	011
6	LED_RX	010
7	LED_TX	001
8	VSS	000

88E1111 Hardware Register Map				
DIP	88E1111 Pin	Bit[2]	Bit[1]	Bit[0]
SW7	CONFIG0	PHYADDR[2]	PHYADDR[1]	PHYADDR[0]
SW8	CONFIG1	ENE_PAUSE	PHYADDR[4]	PHYADDR[3]
SW9	CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
SW10	CONFIG3	ANEG[0]	ENA_XC	DIS_125
SW11	CONFIG4	MODE[2]	MODE[1]	MODE[0]
SW12	CONFIG5	DIS_FC	DIS_SLEEP	MODE[3]
SW13	CONFIG6	SEL_BDT	INT_POL	75/50 Ohm

Note: DIP switches SW[7:13] utilize same position mapping.

Table 22. Board DIP Switch Designations for Marvell Transceiver Configuration Pins

Switch	PHY Configuration Pin
SW7	CONFIG0
SW8	CONFIG1
SW9	CONFIG2
SW10	CONFIG3
SW11	CONFIG4
SW12	CONFIG5
SW13	CONFIG6

Figure 19. DIP Switch Positions for CONFIG Pins

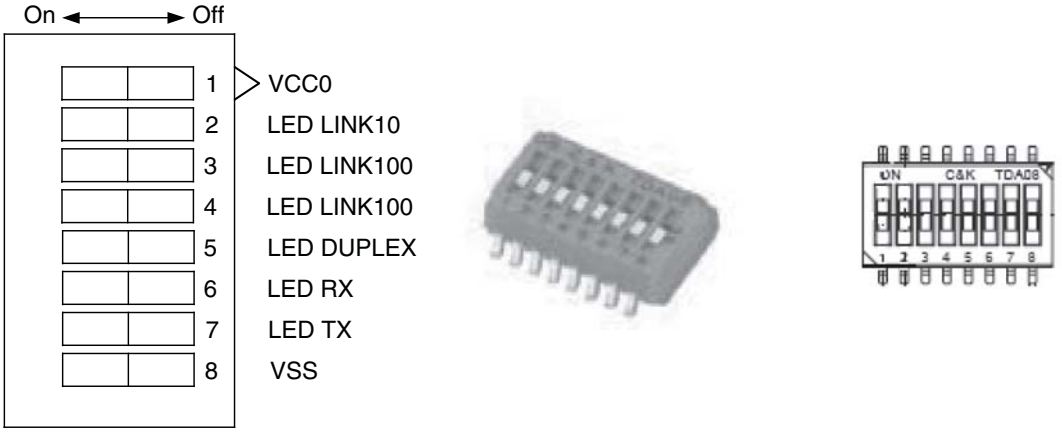


Table 23. Marvel Transceiver Configuration Defaults

DIP Switch	PHY Config Pin	Position ON	Encoded Output Pin	Encoded Value	Description
SW7	CONFIG0	7	LED TX	001	PHY ADDR[2:0] = 001
SW8	CONFIG1	4	LED LINK1000	100	ENABLE PAUSE, PHY ADDR[4:3] = 00
SW9	CONFIG2	1	VCCO	111	Auto Neg., Advertise All, Prefer Slave
SW10	CONFIG3	1	VCCO	111	Enable MDI Crossover, Disable 125 CLK
SW11	CONFIG4	8	VSS	000	1000 Base-X without clock 1000 Base-X Auto Neg. to copper (GBIC)
SW12	CONFIG5	2	LED LINK10	110	Disable fiber/copper, Auto-detect, Enable Sleep
SW13	CONFIG6	8	VSS	000	Select MDC/MDIO, INTn Active High, 50-ohm termination

Table 24. FPGA/MAC to 88E1111 PHY Interconnections (see Appendix A, Figure 33)

MAC Netname	88E1111 Pin	1156 fpBGA Ball Number
GTXCLK	E2	A18
TX_CLK	D1	J17/PCLKT0_0
TX_ER	F2	K20
TX_EN	E1	B19
TXD7	J2	A19
TXD6	J1	H19
TXD5	H3	G19
TXD4	H1	F18
TXD3	H2	D18
TXD2	G3	H18
TXD1	G2	J18
TXD0	F1	B18
RX_CLK	C1	E19/PCLKT1_0
RX_ER	D2	L19
RX_DV	B1	C19
RXD7	C5	C20
RXD6	A2	G21
RXD5	A1	G20
RXD4	C4	B20
RXD3	B3	A20
RXD2	C3	K19
RXD1	D3	J19
RXD0	B2	D19
CRS	B5	A17
COL	B6	B17
S_IN+	A3	AP23
S_IN-	A4	AN23
S_CLK+	A5	nc
S_CLK-	A6	nc
S_OUT+	A7	AL23
S_OUT-	A8	AK23

Table 25. 88E1111 Control and Status Interconnections to FPGA (see Appendix A, Figure 33)

PHY Control/Status	88E1111 Pin	1156 fpBGA Ball Number
MDIO	M1	D20
MDC	L3	F21
RESETn	K3	F22
INTn	L1	A21
FREQ_SEL	H8	B21
CLK25	H9	D21

Crossover PLD Device

(see Appendix A, Figure 25, U17)

The board includes a Lattice LCMXO-1200C Crossover PLD which is used in conjunction with the parallel Flash device for loading the configuration memory of the FPGA. It is also used for general-purpose board management functions. It has several connections to the FPGA and other devices on the board and includes an active high, push-button (SW4) if needed for user designs.

Generic user-defined interconnections are defined in Table 26.

Table 26. MachXO to FPGA Interconnections

MachXO csBGA Ball Number	FPGA fpBGA Ball Number
M1	C3
P13	C4
P10	B1
N7	B2
N8	E4
P11	D4
N13	B3
N1	A2
N3	D5
N4	C6
P1	B4
M12	A3
M2	D6
M3	C5
M4	A4
M6	A5

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP3 Serial Protocol Board	LFE3-95EA-SP-EVN	

Known Issues

SATA Target interface(CN2) channel – Transmit data must be polarity-inverted in FPGA design for correct connection.

SATA Host interface(CN1) channel – Receive data must be polarity-inverted in FPGA design for correct connection.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
August 2009	01.0	Initial release.
September 2009	01.1	Updated Programming the Daisy Chain text section.
May 2010	01.2	Added Known Issues section.
July 2010	01.3	Updated Ordering Part Number in the Ordering Information table.

Appendix A. Schematic

Figure 20. Cover Page

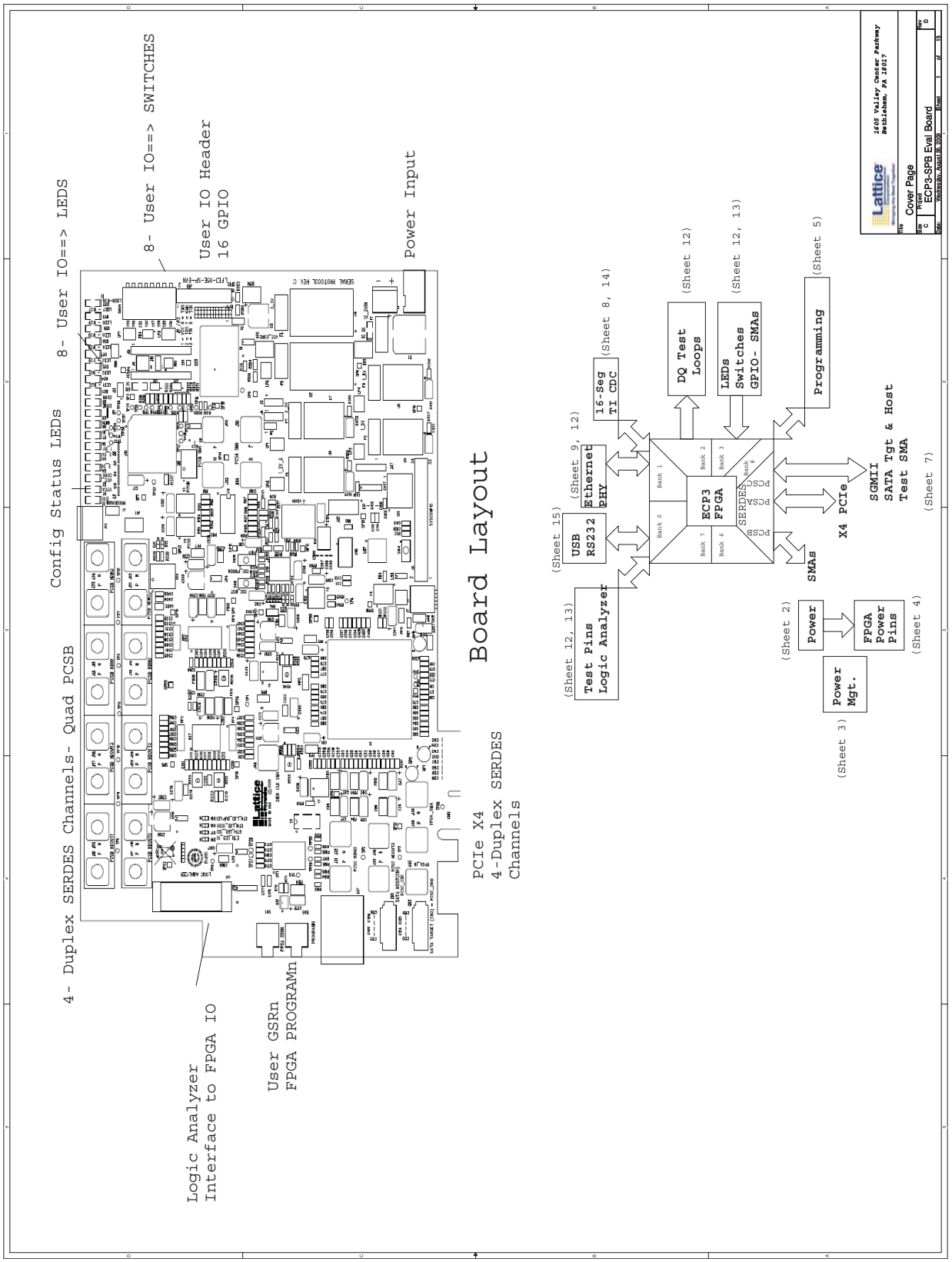


Figure 21. Power Generation

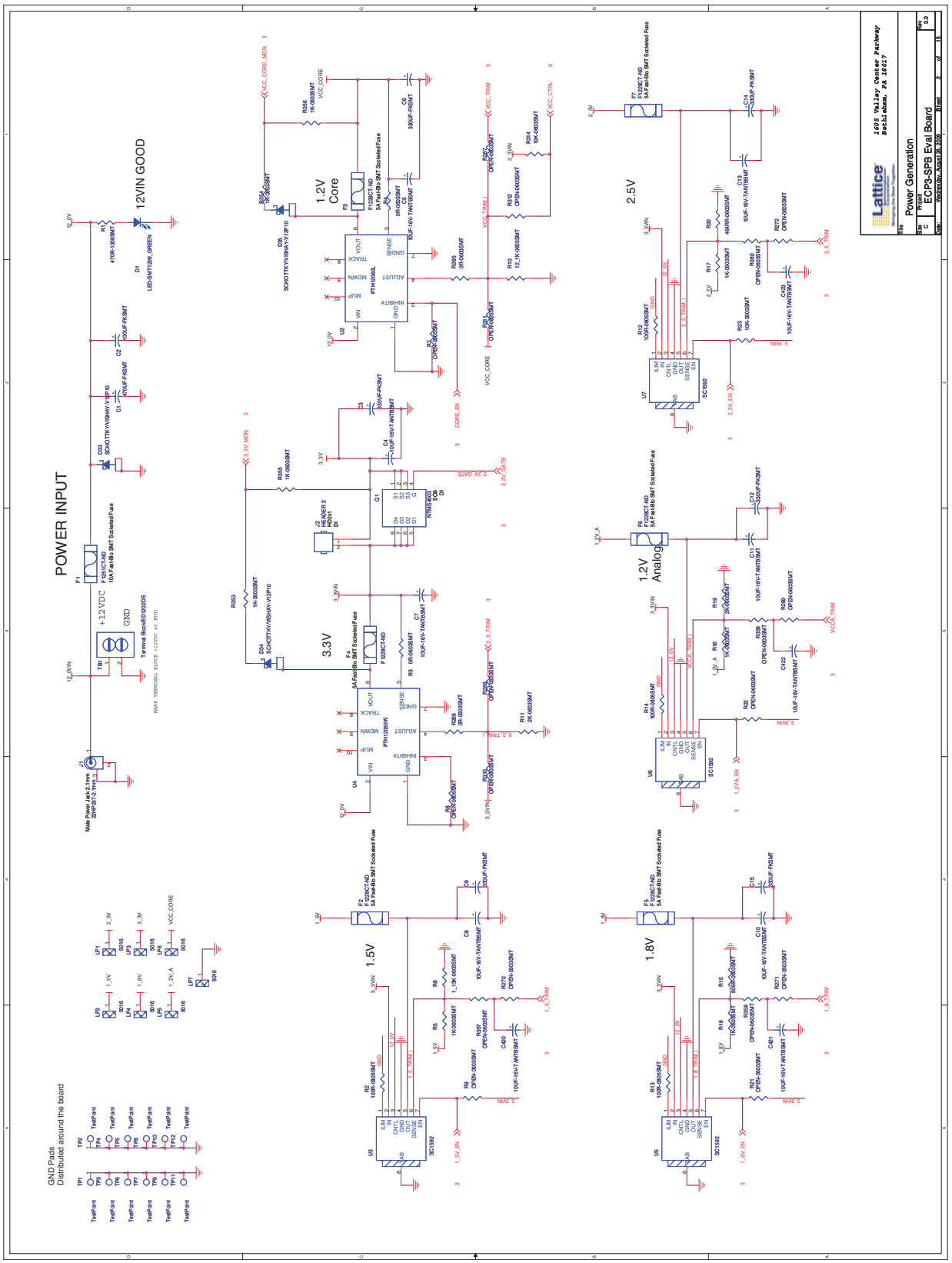


Figure 22. Power Management

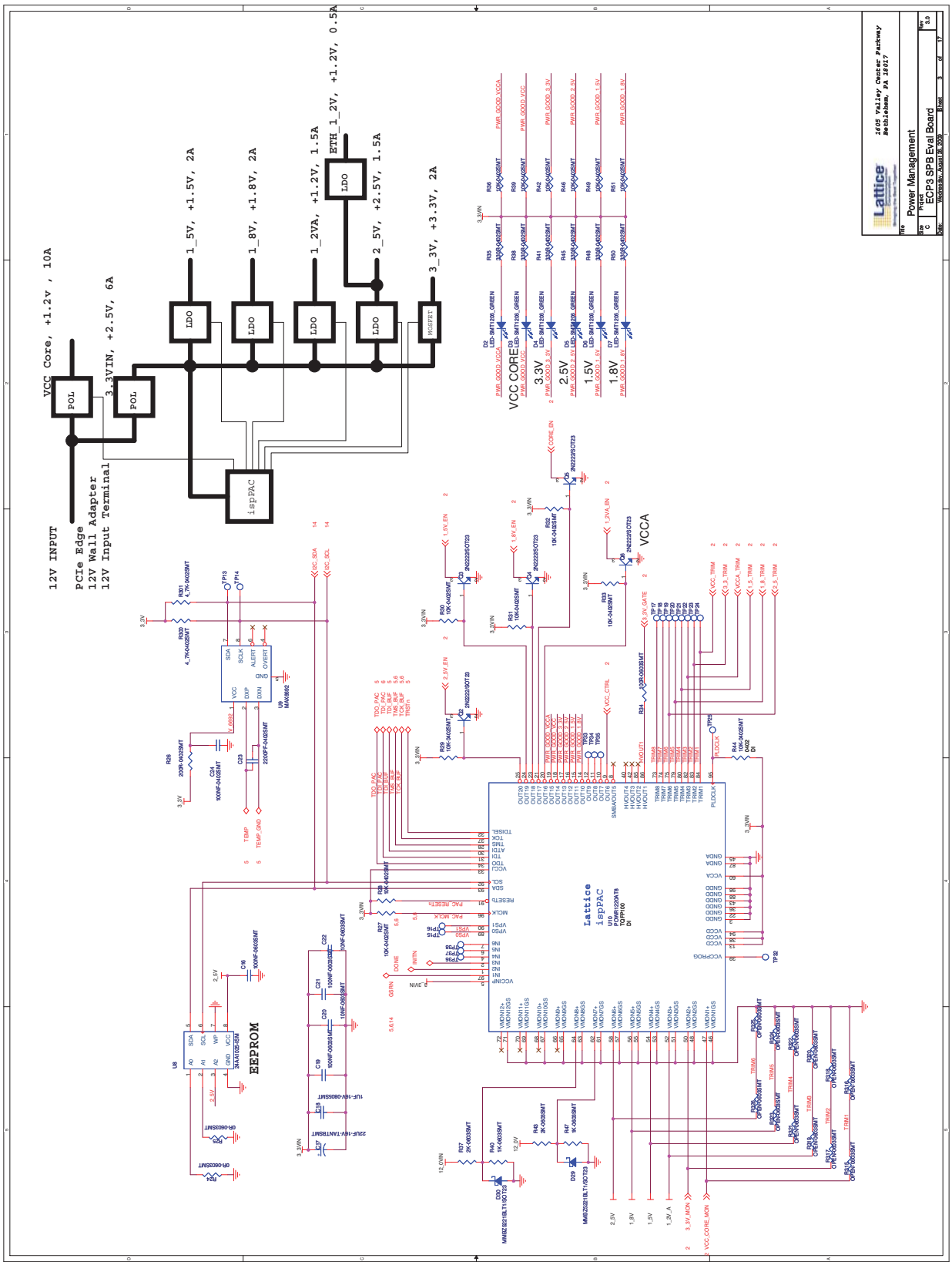


Figure 23. Power Supplies

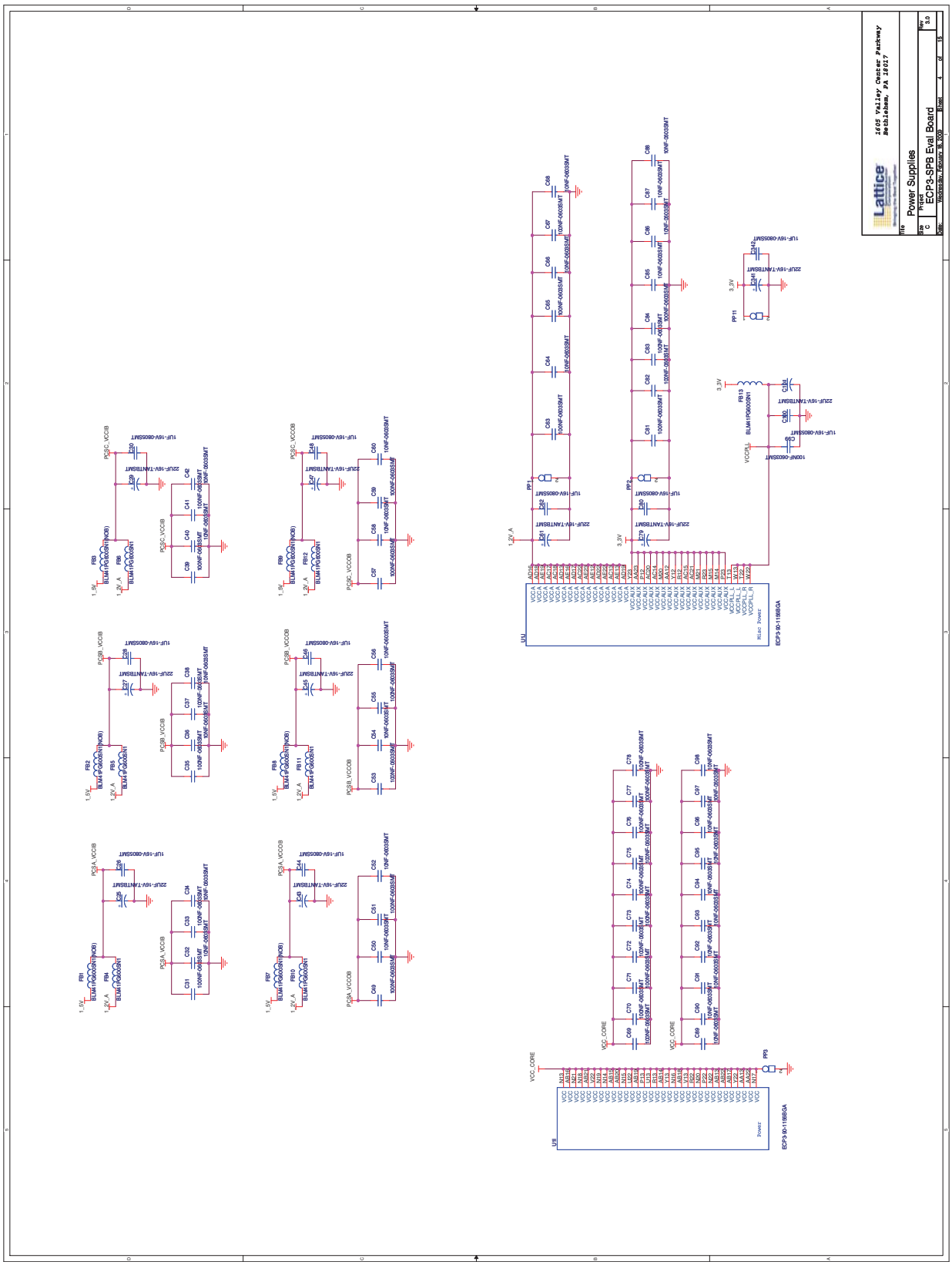


Figure 24. Programming

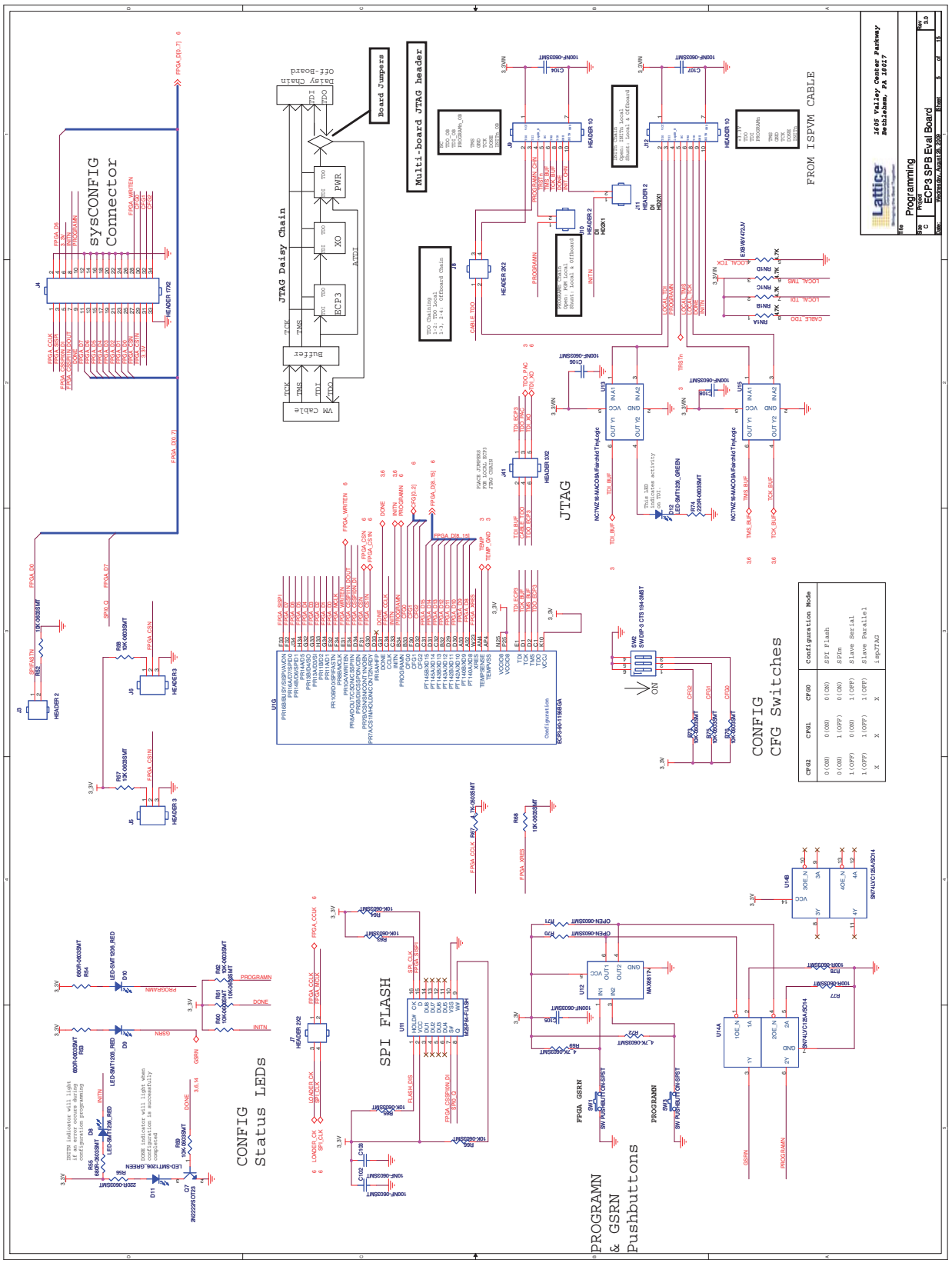


Figure 25. Parallel FPGA Loader

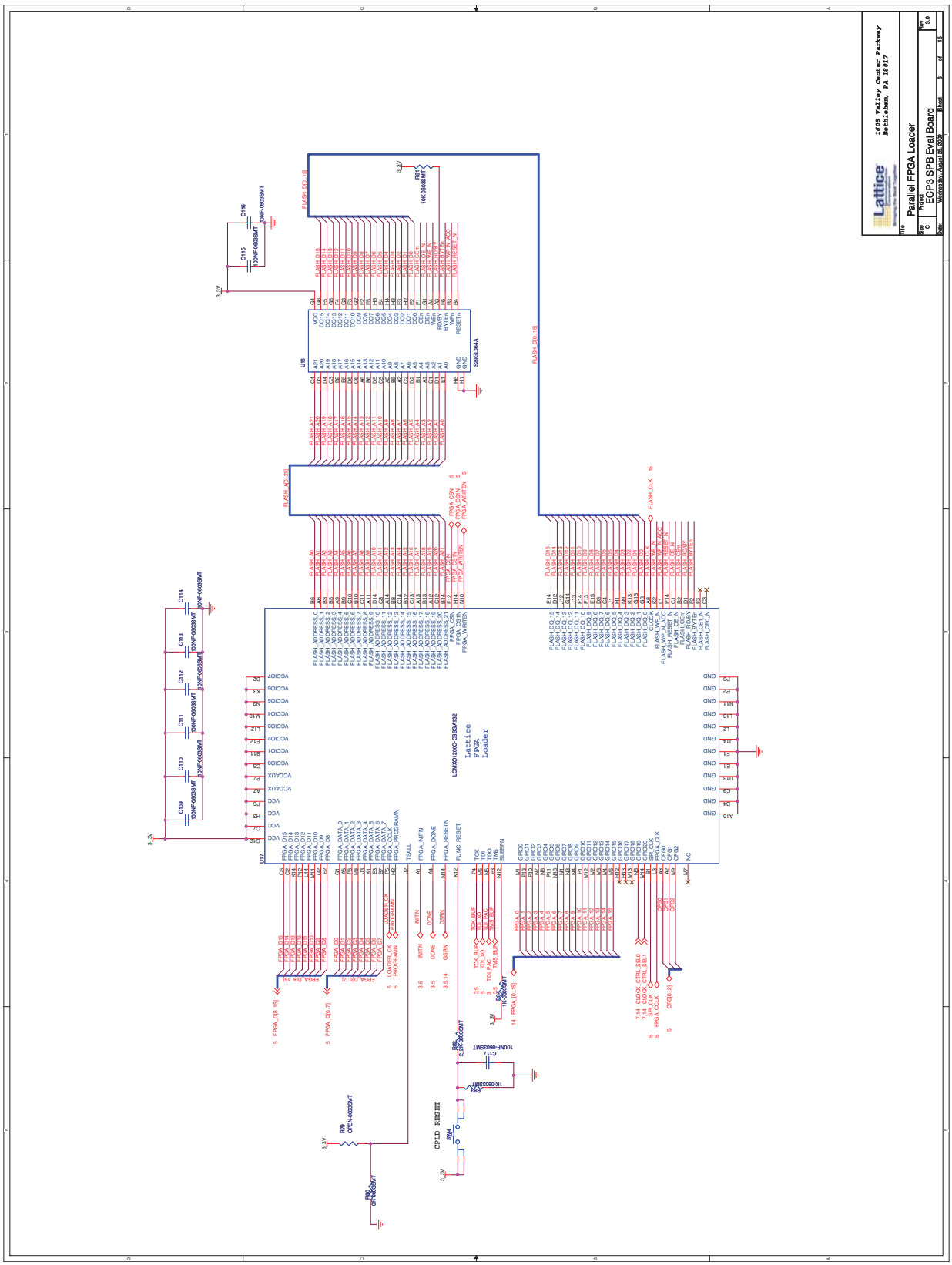


Figure 26. SERDES

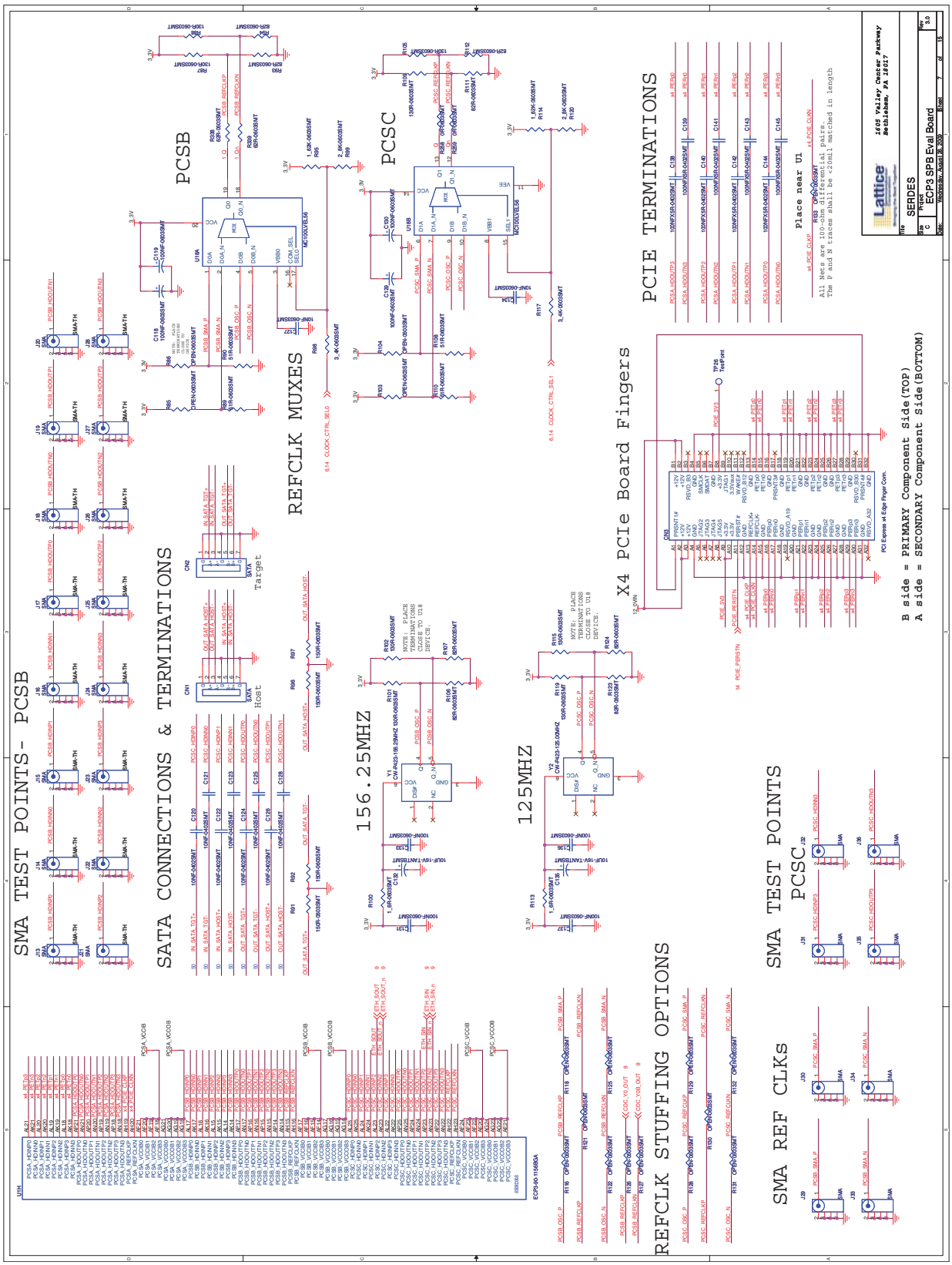


Figure 27. Clock Cleaner

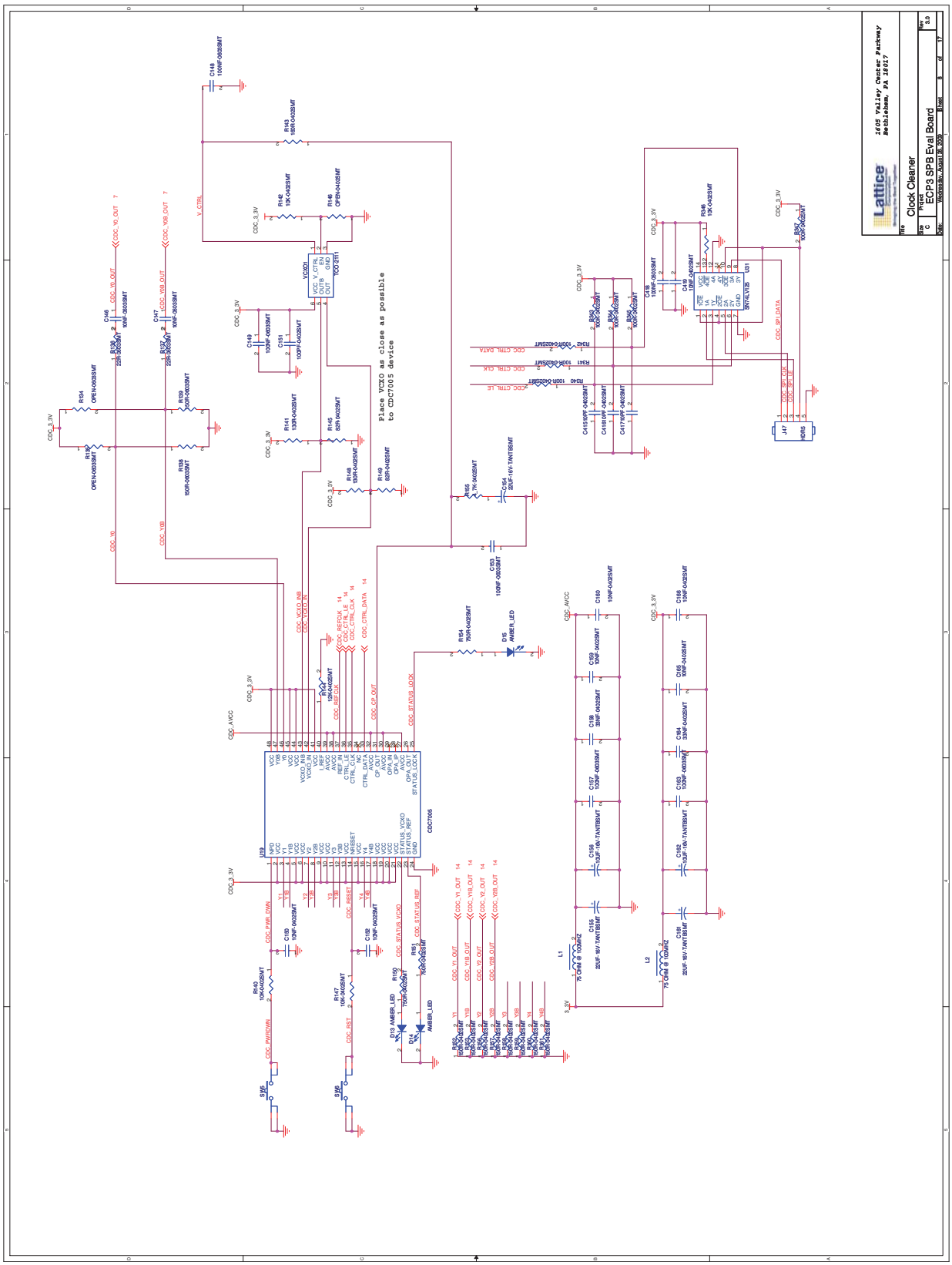


Figure 28. 1000BASE-T PHY/RJ45

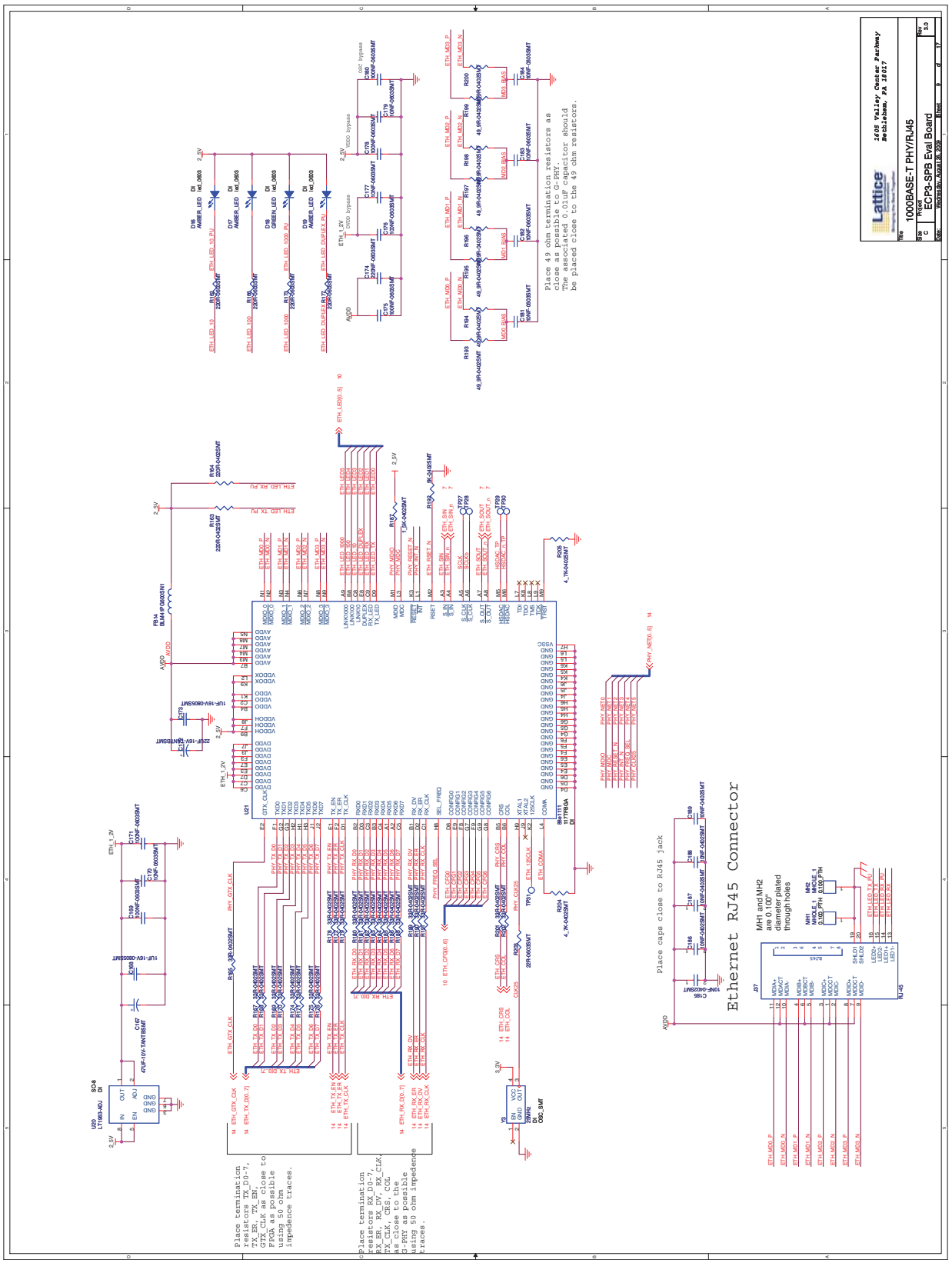


Figure 29. PHY Configuration

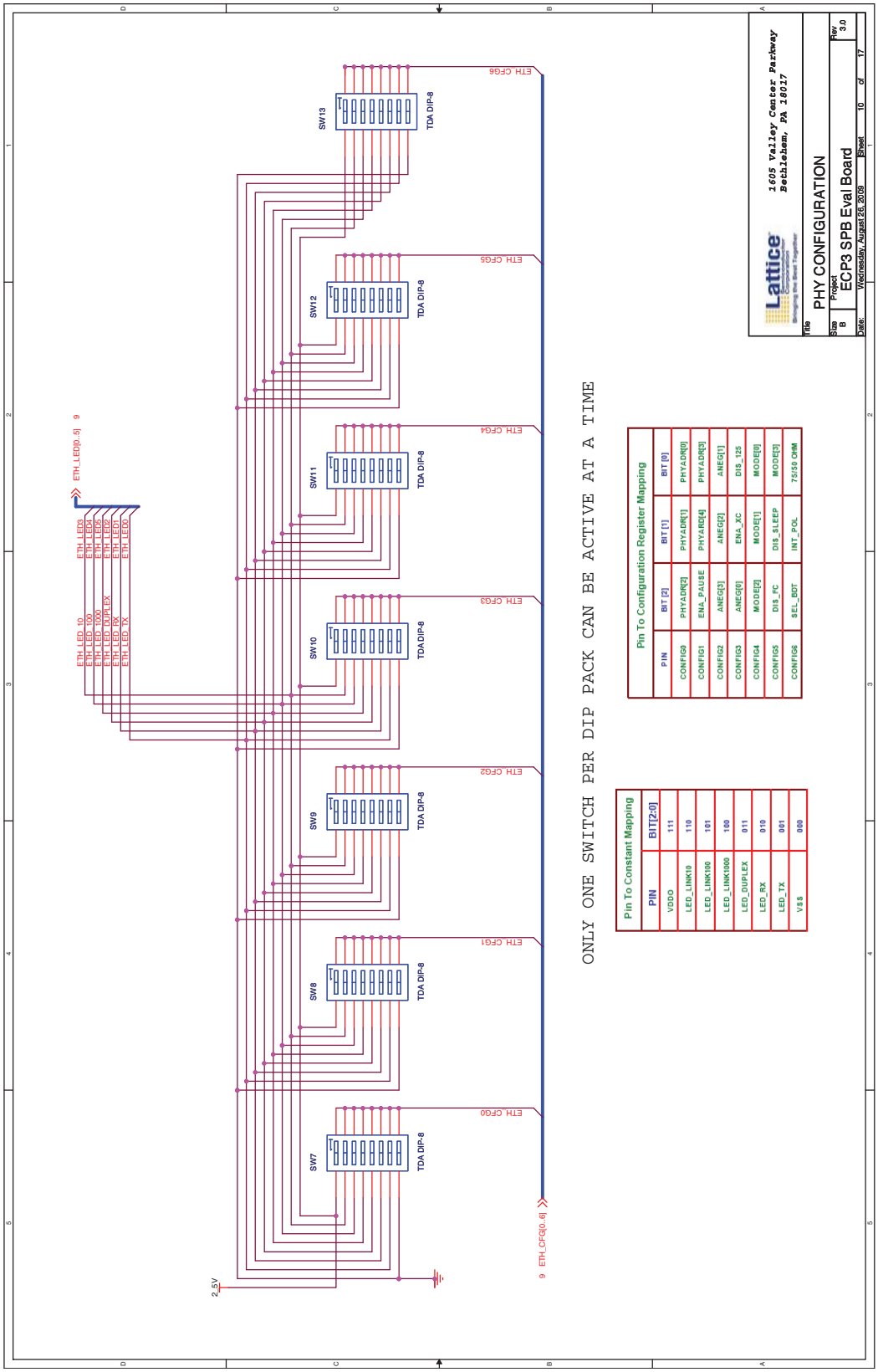


Figure 30. Bank 6 and Bank 7

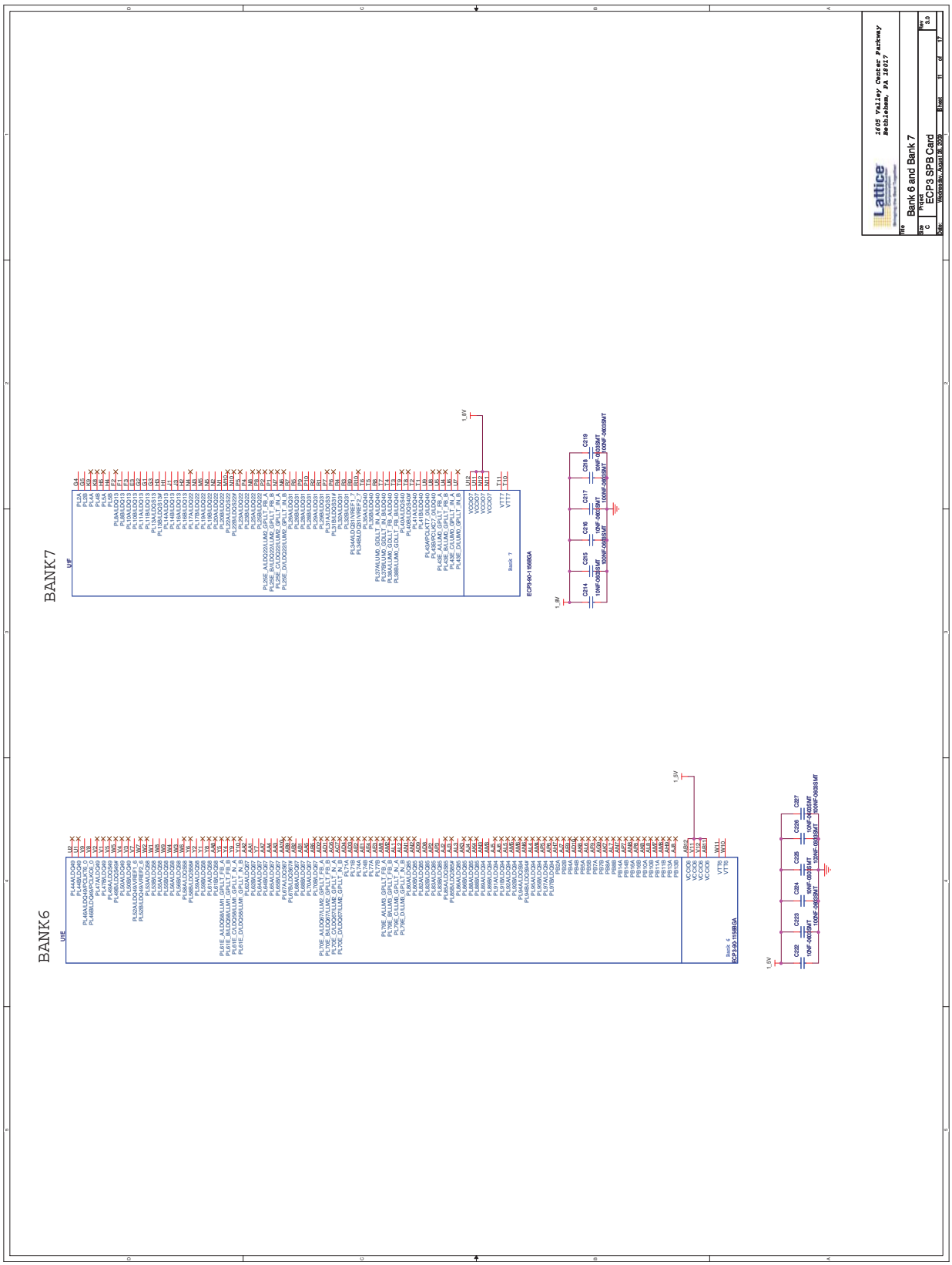


Figure 31. FPGA Test

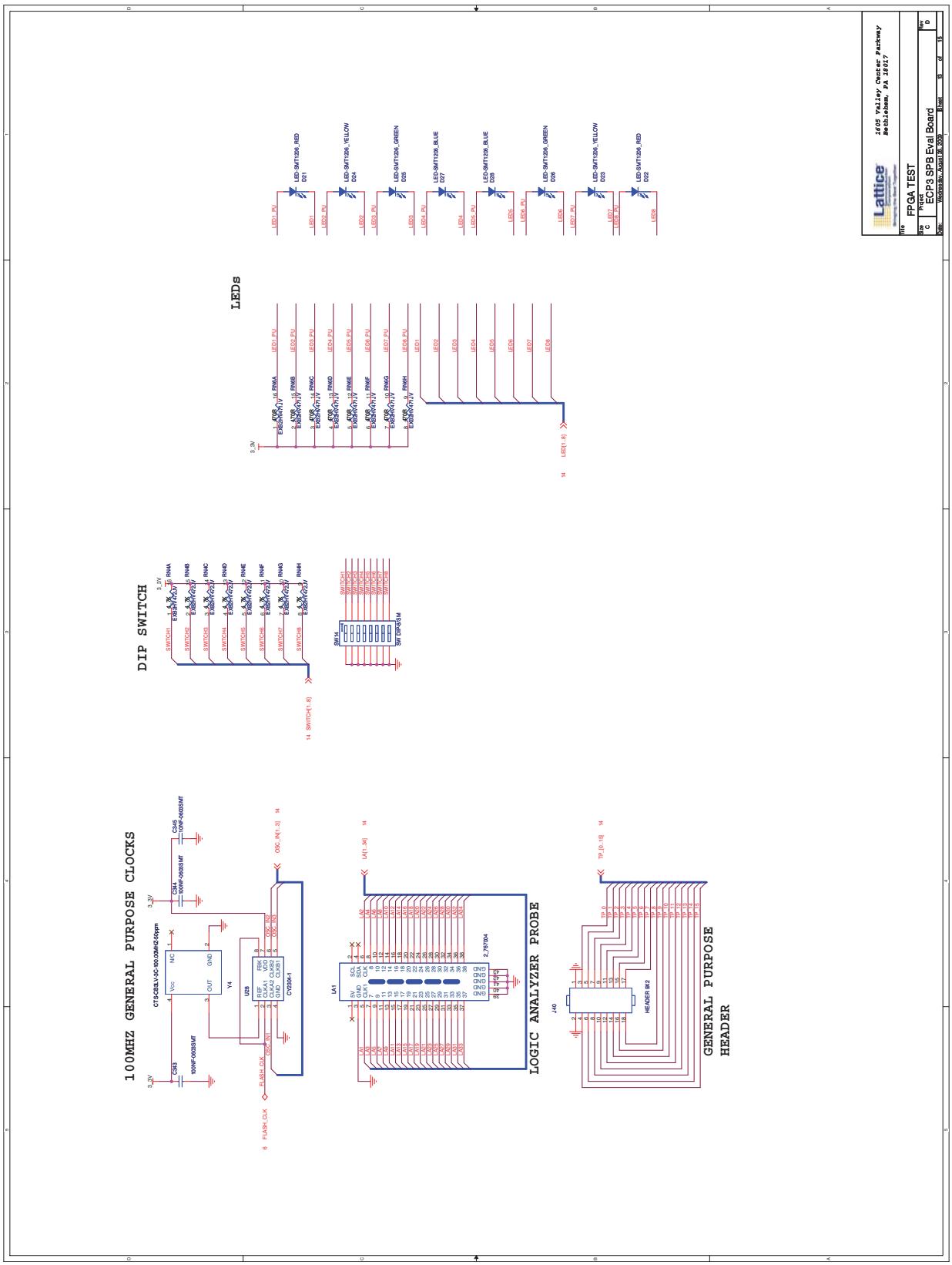


Figure 32. VSS/Decoupling

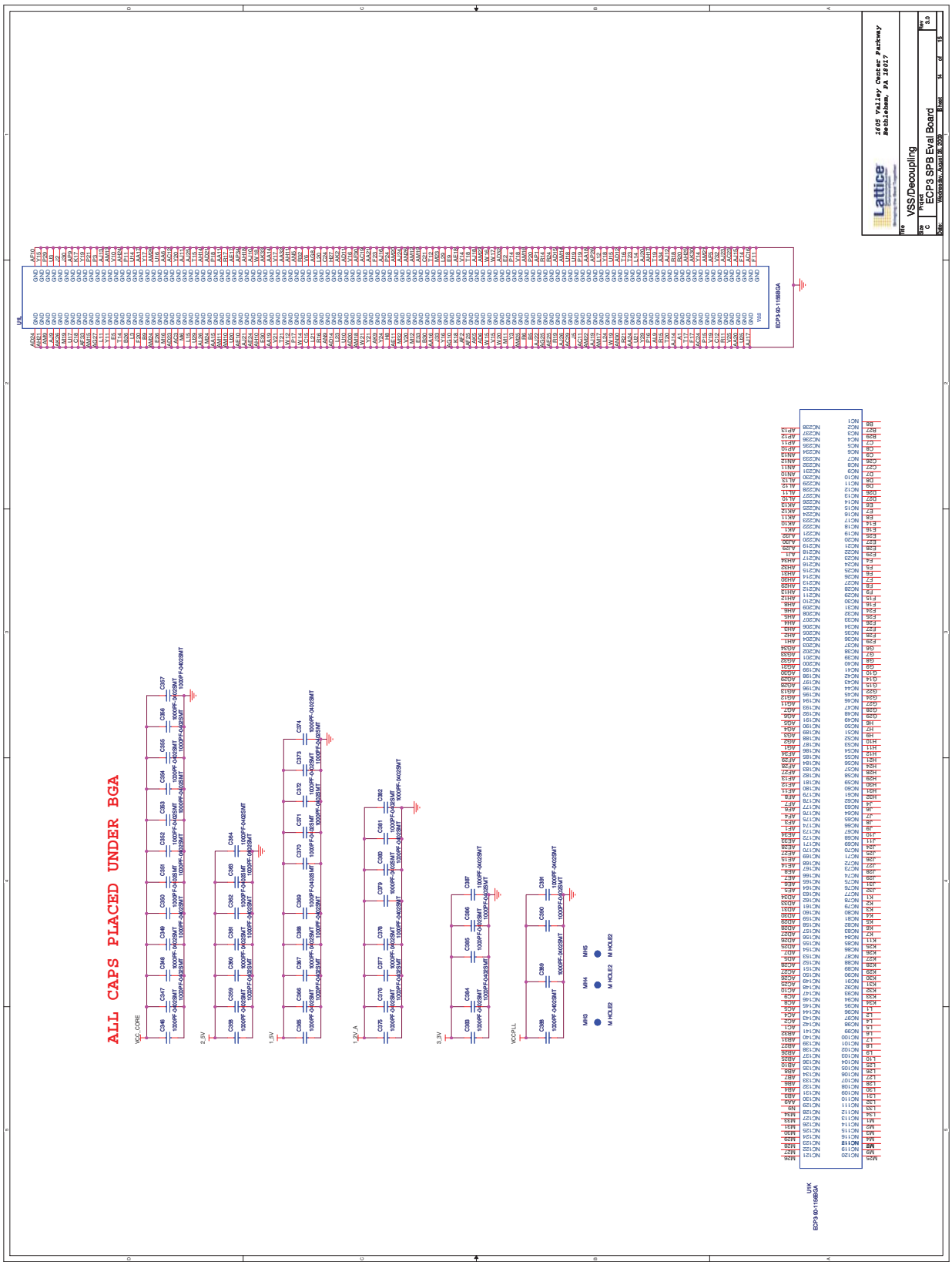


Figure 33. FPGA Pins

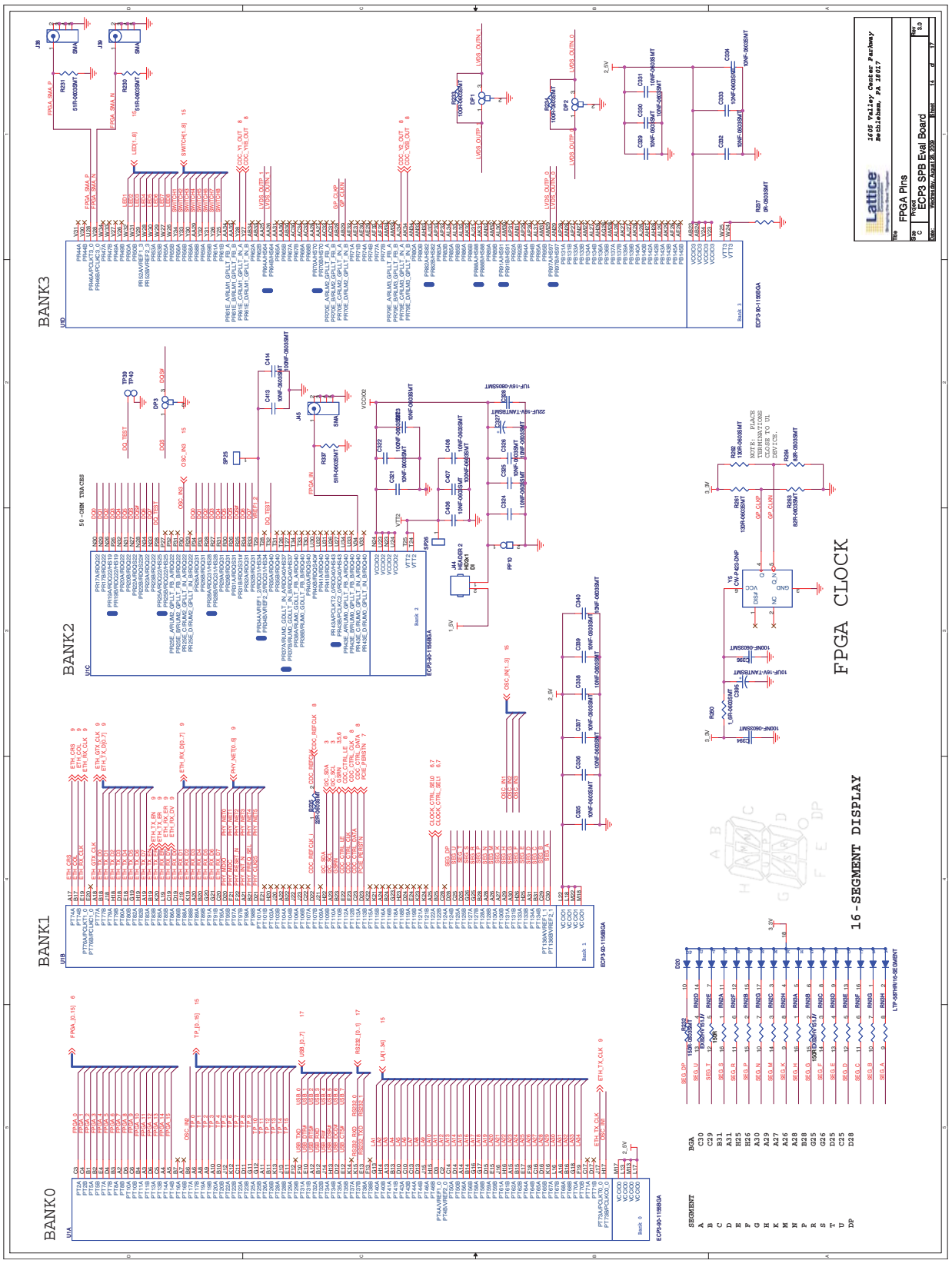
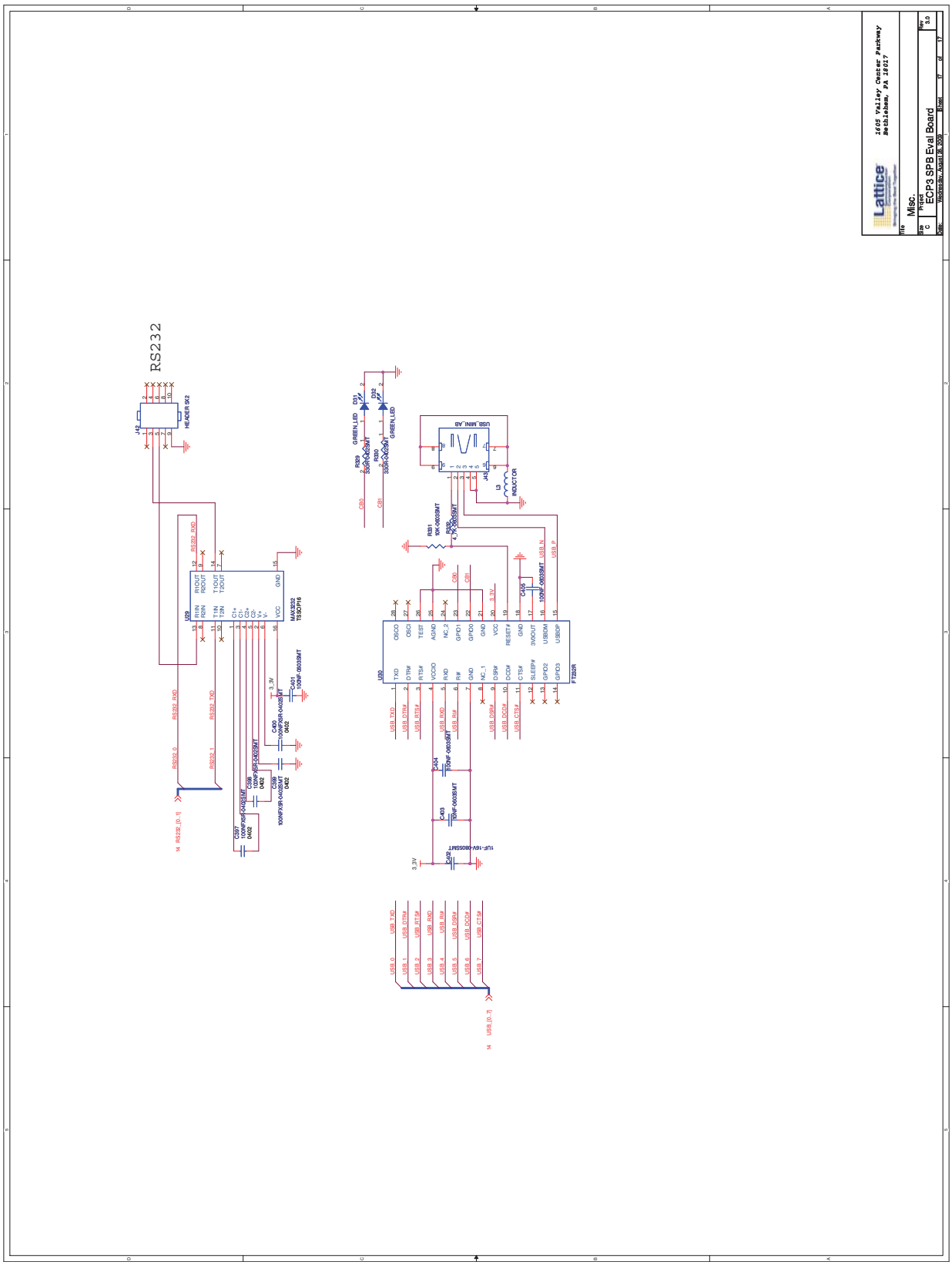


Figure 34. Miscellaneous



Appendix B. Bill of Materials

Table 27. Bill of Materials

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
1	2	CN1,CN2	SATA	Molex	67800-1005/ DK#WM19023-ND	CONN HEADER 7POS VERT SMD 15GOLD
2	1	CN3	PCI Express x4 Edge Finger Conn.			PCB Edge finger
3	1	C1	470UF-FKSMT	Panasonic	EEV-FK1V471Q	CAP 470UF 35V ELECT FK SMD
4	5	C2,C199,C211,C233,C280	100UF-FKSMT	Panasonic	EEE-FK1V101XP	CAP 100UF 35V ELECT FK SMD
5	6	C3,C6,C9,C12,C14,C15	330UF-FKSMT	Panasonic	EEE-FK1C331P	CAP 330UF 16V ELECT FK SMD
6	16	C4,C5,C7,C8,C10,C11,C13,C132,C135,C156,C162,C201,C213,C234,C282,C395	10UF-16V-TANTBSMT	AVX	TAJB106K016R	CAP TANTALUM 10UF 16V 10% SMD
7	121	C16,C19,C21,C31,C33,C35,C37,C39,C41,C49,C51,C53,C55,C57,C59,C63,C65,C67,C69,C70,C71,C72,C73,C74,C75,C76,C77,C78,C81,C82,C83,C84,C99,C102,C104,C105,C106,C107,C108,C109,C111,C113,C115,C117,C118,C119,C129,C130,C131,C133,C136,C137,C148,C149,C153,C157,C163,C169,C171,C175,C176,C178,C180,C190,C192,C194,C196,C198,C202,C204,C206,C208,C210,C215,C217,C219,C223,C225,C227,C228,C230,C232,C239,C240,C242,C245,C250,C253,C254,C257,C259,C261,C264,C266,C268,C270,C272,C274,C275,C277,C279,C286,C287,C290,C292,C294,C300,C302,C304,C305,C307,C310,C312,C314,C316,C318,C320,C343,C344,C394,C396	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603
8	21	C17,C25,C27,C29,C43,C45,C47,C61,C79,C101,C154,C155,C161,C172,C237,C246,C255,C283,C296,C327,C341	22UF-16V-TANTBSMT	Kemet	T491B226M016AT	
9	27	C18,C26,C28,C30,C44,C46,C48,C62,C80,C100,C168,C173,C191,C200,C203,C212,C229,C235,C238,C247,C256,C276,C281,C284,C297,C328,C342	1UF-16V-0805SMT	Panasonic	ECJ-2FB1C105K	CAP 1UF 16V CERAMIC 0805 X5R
10	113	C20,C22,C32,C34,C36,C38,C40,C42,C50,C52,C54,C56,C58,C60,C64,C66,C68,C85,C86,C87,C88,C89,C90,C91,C92,C93,C94,C95,C96,C97,C98,C103,C110,C112,C114,C116,C127,C134,C146,C147,C170,C177,C179,C181,C182,C183,C184,C195,C197,C207,C209,C214,C216,C218,C222,C224,C226,C236,C241,C243,C244,C248,C249,C251,C252,C258,C260,C262,C263,C265,C267,C269,C271,C273,C285,C288,C289,C291,C293,C295,C298,C299,C301,C303,C306,C308,C309,C311,C313,C315,C317,C319,C321,C322,C323,C324,C325,C326,C329,C330,C331,C332,C333,C334,C335,C336,C337,C338,C339,C340,C345,C392,C393	10NF-0603SMT	Kemet	C0603C103K5RACTU	CAP .01UF 50V CERAMIC X7R 0603
11	1	C23	2200PF-0402SMT	AVX	0402YC223KAT2A	CAP CERM .022UF 10% 16V X7R 0402
12	1	C24	100NF-0402SMT	Yageo	04022F104Z7B20D	CAP .10UF 16V CERAMIC Y5V 0402
		Alt: CC0402ZRY5V7BB104				
13	19	C120,C121,C122,C123,C124,C125,C126,C128,C150,C152,C159,C160,C165,C166,C185,C186,C187,C188,C189	10NF-0402SMT	Panasonic	ECJ0EB1E103K	CAP .01UF 25V CERAMIC X7R 0402
14	8	C138,C139,C140,C141,C142,C143,C144,C145	100NFX5R-0402SMT	Kemet	C0402C104K8PACTU	CAP .10UF 10V CERAMIC X5R 0402
15	1	C151	100PF-0402SMT	AVX	04026C101KAT2A	CAP CER 100PF 6.3V X7R 0402
		Alt: ECJ-0EB1E101K				
16	2	C158,C164	33NF-0402SMT	AVX	0402YD333KAT2A	CAP CERM .033UF 10% 16V X5R 0402
17	5	C167,C193,C205,C231,C278	47UF-10V-TANTBSMT	Kemet	B45196H2476K209	CAP TANTALUM 47UF 10V 10% SMD
18	1	C174	220NF-0603SMT	AVX	06036C224KAT2A	CAP CER .22UF 6.3V X7R 0603
		Alt: 0603ZC224KAT2A				
19	46	C346,C347,C348,C349,C350,C351,C352,C353,C354,C355,C356,C357,C358,C359,C360,C361,C362,C363,C364,C365,C366,C367,C368,C369,C370,C371,C372,C373,C374,C375,C376,C377,C378,C379,C380,C381,C382,C383,C384,C385,C386,C387,C388,C389,C390,C391	1000PF-0402SMT	Panasonic	ECJ-0EB1E102K	CAP 1000PF 25V CERAMIC X7R 0402
20	2	DP1,DP2	DIFFTESTPOINT			
21	11	D1,D2,D3,D4,D5,D6,D7,D11,D12,D25,D26	LED-SMT1206_GREEN	Panasonic	LNJ316C83RA	LED GREEN (UP) W/LENS 1206

Table 27. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
22	5	D8,D9,D10,D21,D22	LED-SMT1206_RED	Panasonic	LNJ211R82RA	LED RED (UP) W/LENS 1206
23	6	D13,D14,D15,D16,D17,D19	AMBER_LED	Lite-On	LTST-C190AKT	LED AMBER CLEAR 0603 SMD
24	1	D18	GREEN_LED	Lite-On	LTST-C190GKT	LED GREEN CLEAR 0603 SMD
25	1	D20	LTP-587HR/16-SEGMENT	Lite-On	LTP-587HR	16-segment array
26	2	D23,D24	LED-SMT1206_YELLOW	Panasonic	LNJ411K84RA	LED YELLOW (UP) W/LENS 1206
27	2	D27,D28	LED-SMT1206_BLUE	Panasonic	LNJ916C8BRA	LED BLUE (UP) W/LENS 1206
28	6	FB1,FB2,FB3,FB7,FB8,FB9	BLM41PG600SN1(NOB)			
29	13	FB4,FB5,FB6,FB10,FB11,FB12,FB13,FB14 ,FB15,FB16,,FB18,FB19,FB20,	BLM41PG600SN1	Murata	BLM41PG600SN1L	FERRITE CHIP 60 OHM 6000MA 1806
30	2	F1, F3	F1251CT-ND	Littlefuse	þ	FUSEBLOCK WITH 10A FUSE SMD
31	5	F2,F4,F5,F6,F7	F1228CT-ND	Littlefuse	0154005.DR	FUSEBLOCK WITH 5A FUSE SMD
32	1	J1	22HP037-2.1mm	Condor	22HP037A	power input
33	4	J2,J3,J10,J11	HEADER 2	Samtec	TSW-102-07-T-S	2x1-0.25 Header
34	1	J4 (SEE ECN FOR Placement)	HEADER 17X2	Samtec	TSW-117-07-T-D	17x2-0.25 Header
35	2	J5,J6	HEADER 3	Samtec	TSW-103-07-T-S	3x1-0.25 Header
36	2	J7,J8	HEADER 2X2	Samtec	TSW-102-07-T-D	2x2-0.25 Header
37	2	J9,J12	HEADER 10	Samtec	TSW-110-07-T-S	10x1-0.25 Header
38	16	J13,J14,J15,J16,J17,J18,J19,J20,J21,J22,J 23,J24,J25,J26,J27,J28	Rosenberger 32K153-400E3	Rosenberger	32K153-400E3	TH- SMA connector
	Alt		32K153-400L5			
39	10	J29,J30,J31,J32,J33,J34,J35,J36,J38,J39	SMA	Molex	73391-0060	CONN JACK SMA STR 50 OHM PCB
40	1	J37	RJ-45	Bel Fuse	L-829-1J1T-43	Integrated RJ45 Connector
41	1	J40	HEADER 9X2	Samtec	TSW-109-07-T-D	9x2-0.25 Header
42	1	LA1	2_767004	Amp	2-767004-2	CONN RECEPT 38POS .025 VERT SMD
43	7	LP1,LP2,LP3,LP4,LP5,LP6,LP7	5016	Keystone Electronics	5016	TEST POINT PC COMPACT SMT
44	2	L1,L2	75 OHM @ 100MHZ	Murata	BLM18BA750SN1D	
45	2	MH1,MH2	MHOLE_1			
46	3	MH3,MH4,MH5	M HOLE2			
47	10	PP1,PP2,PP3,PP4,PP5,PP7,PP8,PP9,PP1 0,PP11	PROBEPOINT			
48	1	Q1	NTMS4503	ON Semiconductor	NTMS4503NR2G	MOSFET N-CH 28V 14A 8-SOIC
49	6	Q2,Q3,Q4,Q5,Q6,Q7	2N2222/SOT23	Diodes Inc	MMBT2222A-7	TRANS NPN 40V 350MW SMD SOT-23
50	1	RN1	EXBV8V472JV	Panasonic	EXBV8V472JV	RES ARRAY 4.7K OHM 5% 4 RES SMD
51	2	RN2,RN3	EXB2HV151JV	Panasonic	EXB2HV151JV	RES ARRAY 150 OHM 5% 8 RES SMD
52	1	RN4	EXB2HV472JV	Panasonic	EXB2HV472JV	RES ARRAY 4.7K OHM 5% 8 RES SMD
53						
54	1	RN6	EXB2HV471JV	Panasonic	EXB2HV471JV	RES ARRAY 470 OHM 5% 8 RES SMD
55	4	RP1,RP2,RP3,RP4	CTS-RT1402B7	CTS Corporation Resistor/ Electrocomponents	RT2402B7	RES NET DDR SDRAM 50 OHM 3X9 BGA
56	1	R1	470R-1206SMT	Panasonic	ERJ-8GEYJ471V	RES 470 OHM 1/4W 5% 1206 SMD
57	4	R2,R12,R13,R14	100R-0805SMT	Panasonic	ERJ-6GEYJ101V	RES 100 OHM 1/8W 5% 0805 SMD
58	20	R3,R4,R24,R25,R80,R207,R209,R211,R21 5,R217,R222,R227,R236,R237,R249,R254, R258,R259,R265,R266	0R-0603SMT	Panasonic	ERJ-3GEY0R00V	RES ZERO OHM 1/10W 5% 0603 SMD
59	1	R6	1_13K-0603SMT	Panasonic	ERJ-3EKF1131V	RES 1.13K OHM 1/10W 1% 0603 SMD
60	0		50R-0603SMT	Vishay	FC0603E50R0BTBT1	RES 50 OHM 125MW .1% 0603 SMD
61	2	R7,R8	OPEN-0805SMT			

Table 27. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
62	47	R70,R71,R79,R85,R86,R103,R104,R116,R118,R121,R122,R125,R126,R127,R128,R129,R130,R131,R132,R133,R134,R135,R214,R220,R226,R250,R251,R267,R268,R270,R271,R272,R310.R311,R312,R315,R316,R317,R318,R319,R320,R321,R322,R323,R324,R325,R326	OPEN-0603SMT			
63	1	R10	12_1K-0603SMT	Susumu Co Ltd	RG1608P-1212-B-T5	RES 12.1K OHM 1/10W .1% 0603 SMD
64	4	R11,R19,R37,R43	2K-0603SMT	Panasonic	ERJ-3EKF2001V	RES 2.00K OHM 1/10W 1% 0603 SMD
65	1	R15	806R-0603SMT	Panasonic	ERJ-3EKF8060V	RES 806 OHM 1/10W 1% 0603 SMD
66	0	R16	49_9R-0603SMT	Yageo	RC0603FR-0749R9L	RES 49.9 OHM 1/10W 1% 0603 SMD
		Alt: RC0603FR-0749R9L				
67	5	R34,R77,R78,R233,R234	100R-0603SMT	Panasonic	ERA-3YEB101V	RES 100 OHM 1/16W .1% 0603 SMD
68	0	R18	66_5R-0603SMT	Vishay	CRCW060366R5FKEA	RES 66.5 OHM 1/10W 1% 0603 SMD
69	21	R9,R21,R22,R23,R52,R57,R58,R59,R60,R61,R62,R63,R64,R65,R66,R68,R73,R75,R76,R81,R314	10K-0603SMT	Panasonic	ERJ-3GEYJ103V	RES 10K OHM 1/10W 5% 0603 SMD
70	1	R26	200R-0402SMT	Panasonic	ERJ-2RKF2000X	RES 200 OHM 1/16W 1% 0402 SMD
71	17	R27,R28,R29,R30,R31,R32,R33,R36,R39,R42,R44,R46,R49,R51,R140,R142,R147	10K-0402SMT	Panasonic	ERJ-2RKF1002X	RES 10.0K OHM 1/16W 1% 0402 SMD
72	6	R35,R38,R41,R45,R48,R50	330R-0402SMT	Panasonic	ERJ-2GEJ331X	RES 330 OHM 1/16W 5% 0402 SMD
73	19	R5,R18,R16,R17,R40,R47,R83,R84,R212,R216,R219,R223,R224,R228,R229,R246,R247,R252,R253	1K-0603SMT	Panasonic	ERJ-3EKF1001V	RES 1.00K OHM 1/16W 1% 0603 SMD
74	3	R53,R54,R55	680R-0603SMT	Panasonic	ERJ-3GEYJ681V	RES 680 OHM 1/10W 5% 0603 SMD
75	6	R56,R74,R162,R166,R173,R177	220R-0603SMT	Panasonic	ERJ-3GEYJ221V	RES 220 OHM 1/10W 5% 0603 SMD
76	7	R67,R69,R72,R206,R208,R210,R218	4_7K-0603SMT	Panasonic	ERJ-3GEYJ472V	RES 4.7K OHM 1/10W 5% 0603 SMD
77	1	R82	2_2K-0603SMT	Panasonic	ERJ-3GEYJ222V	RES 2.2K OHM 1/10W 5% 0603 SMD
78	10	R87,R88,R101,R102,R105,R109,R115,R119,R261,R262	130R-0603SMT	Panasonic	ERA-3YEB131V	RES 130 OHM 1/16W .1% 0603 SMD
79	6	R89,R90,R108,R110,R230,R231	51R-0603SMT	Panasonic	ERJ-3GEYJ510V	RES 51 OHM 1/10W 5% 0603 SMD
80	7	R91,R92,R96,R97,R138,R139,R232	150R-0603SMT	Panasonic	ERA-3YEB151V	RES 150 OHM 1/16W .1% 0603 SMD
81	10	R93,R94,R106,R107,R111,R112,R123,R124,R263,R264	82R-0603SMT	Yageo	RC0603FR-0782RL	RES 82.0 OHM 1/10W 1% 0603 SMD
		Alt: RC0603FR-0782RL				
82	2	R95,R114	1_62K-0603SMT	Panasonic	ERJ-3EKF1621V	RES 1.62K OHM 1/10W 1% 0603 SMD
83	2	R98,R117	3_4K-0603SMT	Panasonic	ERJ-3EKF3401V	RES 3.4K OHM 1/10W 1% 0603 SMD
84	2	R99,R120	2_8K-0603SMT	Panasonic	ERJ-3EKF2801V	RES 2.8K OHM 1/10W 1% 0603 SMD
85	3	R100,R113,R260	1_6R-0603SMT	Panasonic	ERJ-3GEYJ1R6V	RESISTOR 1.6 OHM 1/10W 5% 0603
86	2	R141,R148	130R-0402SMT	Panasonic	ERJ-2RKF1300X	RES 130 OHM 1/16W 1% 0402 SMD
87	1	R143	160R-0402SMT	Panasonic	ERJ-2RKF1600X	RES 160 OHM 1/16W 1% 0402 SMD
88	1	R144	12K-0402SMT	Rohm	MCR01MZPF1202	RES 12.0K OHM 1/16W 1% 0402 SMD
89	2	R145,R149	82R-0402SMT	Panasonic	ERJ-2RKF82R0X	RES 82 OHM 1/16W 1% 0402 SMD
		Alt: CRCW040282R0FKED				
90	1	R146	OPEN-0402SMT			
91	3	R150,R151,R154	750R-0402SMT	Panasonic	ERJ-2RKF7500X	RES 750 OHM 1/16W 1% 0402 SMD
92	8	R152,R153,R156,R157,R158,R159,R160,R161	150R-0402SMT	Panasonic	ERJ-2RKF1500X	RES 150 OHM 1/16W 1% 0402 SMD
93	5	R155,R204,R205,R300,R301	4_7K-0402SMT	Panasonic	ERJ-2RKF4701X	RES 4.70K OHM 1/16.0W 1% 0402 SM

Table 27. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
94	2	R163,R164	220R-0402SMT	Panasonic	ERJ-2RKF2200X	RES 220 OHM 1/16W 1% 0402 SMD
95	25	R165,R167,R168,R169,R170,R171,R172,R174,R175,R176,R178,R179,R180,R181,R182,R183,R184,R185,R186,R188,R189,R190,R191,R201,R202	33R-0402SMT	Panasonic	ERJ-2GEJ330X	RES 33 OHM 1/16W 5% 0402 SMD
96	1	R187	1_5K-0402SMT	Panasonic	ERJ-2RKF1501X	RES 1.50K OHM 1/16W 1% 0402 SMD
97	1	R192	5K-0402SMT	Panasonic	ERJ-2RKF5001X	RES 5K OHM 1/16W 1% 0402 SMD
		Alt: ERJ-2RKF4991X				
98	8	R193,R194,R195,R196,R197,R198,R199,R200	49_9R-0402SMT	Panasonic	ERJ-2RKF49R9X	RES 49.9 OHM 1/16W 1% 0402 SMD
99	5	R136,R137,R203,R235	22R-0603SMT	Yageo	RC0603FR-0722RL	RES 22.0 OHM 1/10W 1% 0603 SMD
100	5	R213,R221,R225,R248,R255	1K_ADJ/SMT3MM	BC Components	ST3A102CT	POT 1K 3MM CERM SQ S/T SMD
101						
102	2	R256,R257	100R-0402SMT	Panasonic	ERJ-2GEJ101X	RES 100 OHM 1/16W 5% 0402 SMD
103	24	SP1,SP2,SP3,SP4,SP5,SP6,SP7,SP8,SP9,SP10,SP11,SP12,SP13,SP14,SP15,SP16,SP17,SP18,SP19,SP20,SP21,SP22,SP23,SP24	TEST POINT			
104	2	SW1,SW3	SW PUSHBUTTON-SPST	C&K Components	EP11FPD	SPST- Momentary RA SMT
105	1	SW2	SW DIP-3 CTS 194-3MST	CTS Corporation Resistor/ Electrocomponents	194-3MST	SWITCH SIDE ACTUATED GOLD 3 SEC
106	3	SW4,SW5,SW6	EVQ-P2H02B	Panasonic	EVQ-P2H02B	SWITCH LT 4.7MMX3.5MM 250GF SMD
107	7	SW7,SW8,SW9,SW10,SW11,SW12,SW13	TDA DIP-8	ITT	TDA08H0SK1	SWITCH DIP 8POS HALF PITCH SMT
108	1	SW14	SW DIP-8/SM	C&K Components	BPA08SB	8-POSITION DIP PACK
109	1	TB1	Terminal Block/ED1202DS	On-Shore Tech.	ED120/2DS	TERMINAL BLOCK 5.08MM VERT 2POS
110	38	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP26,TP27,TP28,TP29,TP30,TP31,TP32,TP33,TP34,TP35,TP36,TP37,TP38	TestPoint			
111	1	U1	LFE3-95E-#FN1156CES	LATTICE SUPPLIED		
112	1	U4	PTH12060W	Texas Instruments	PTH12060WAH	TH MODULE PIP 12VIN 10A ADJ 10-TH
113	4	U3,U5,U6,U7	SC1592	Semtech	SC1592IMTRT	IC LDO ADJ REG 3A TO-263-7
114	1	U8	24AA1025-ISM	Microchip Technology	24AA1025-I/SM	IC SRL EEPROM 1024K 1.8V 8SOIC
115	1	U9	MAX6692	Maxim	MAX6692MSA	IC TEMP SENSING I2C
116	1	U10	POWR1220AT8	LATTICE SUPPLIED		
117	1	U11	M25P64-FLASH	Macronix	MX25L6405MC20G	IC SRL FLASH 64MBIT 3V 16-SOP Wide(300MIL)
118	1	U12	MAX6817	Maxim	MAX6817-EUT+T	±15kV ESD-Protected, Dual, CMOS Switch Debouncers
119	2	U13,U15	NC7WZ16-MACO6A/ Fairchild TinyLogic	Fairchild	NC7WZ16P6X	IC BUFFER UHS DUAL SC70-6
120	1	U14	SN74LVC125A/SO14	Texas Instruments	SN74LVC125AD	IC QUAD BUS BUFFER GATE 14-SOIC
121	1	U16	S29GL064A	Spansion	S29GL064N90BFI040	48fBGA FLASH-VBN048
122	1	U17	LCMXO1200C-CSBGA132	LATTICE SUPPLIED		
123	1	U18	MC100LVEL56	ON Semiconductor	MC100LVEL56DW	3.3V ECL Dual Differential 2:1 Multiplexer
124	1	U19	CDC7005	Texas Instruments	CDC7005-QFN	Clock cleaner QFN package
125	1	U20	LT1963-ADJ	Linear Tech	LT1963ES8	IC REG LDO ADJ 1.5A LN 8SOIC
126	1	U21	88e1111	Marvell	88e1111-Bx-BAB-C000(Bx indicates any revision code)	single-port Gigabit Ethernet(117TFBGA)
127	4	U22,U23,U24,U26	LP2996-SO8	National Semi	LP2996M	IC DDR TERMINATION REG 8SOIC
130	1	U28	CY2304-1	Cypress Semiconductor	CY2304SC-1	zero delay buffer
131	1	VCXO1	TCO-2111	Epson-Toyocom	TCO2111-245.76MHZ	VCXO 13.9x9.8mm SMT
		Alt: TCO-2111T 245.7600MHZ:RO				

Table 27. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
132	1	Y1	CW-P423-156.25MHZ	Connor-Winfield	CW-P423F-156.25MHZ	5x7.5mm SMT Oscillator 156.25MHz
133	1	Y2	CW-P423-125.00MHZ	Connor-Winfield	CW-P423F-125.0MHZ	5x7.5mm SMT Oscillator 1525.0MHz
134	1	Y3	25MHz	Epson Toyocom Corporation	SG-636PCE 25.0000MC0:ROHS	OSCILLATOR 25.0000MHZ SMD 10.5mm x 5.8mm
135	1	Y4	CTS-CB3LV-3C -100.00MHZ-50ppm	CTS-Frequency Controls	CB3LV-3C-100M0000-T	OSC CLOCK 100.000 MHZ 3.3V SMD
136	DNP	Y5				5x7.5mm SMT Oscillator
137	1	U2	PTH12060L	Texas Instruments	PTH12060LAH	TH MODULE PIP 12VIN 10A ADJ 10-TH(0.8v-1.8v)
138	2	D29,D30	MMBZ5221BLT1	On-Semi	MMBZ5221BLT1	Zener Voltage Regulators 225 mW SOT?23 Surface Mount
139	0	Q20	MMBT3906	Diodes Inc	MMBT3906-7-F	TRANS PNP 40V 300MW SMD SOT23
140	1	R20	464R-0603SMT	Panasonic	ERJ-3EKF4640V	RES 464 OHM 1/10W 1% 0603 SMD
141	A/R	Socket	ISI HLS-341156-B-10			
142	1	R269	ERJ-3EKF4531V	Panasonic	ERJ-3EKF4531V	
143	0	FB17 , FB21	CRCW12100000ZSTA	Vishay		
144	2	R327,R328	0R-2010SMT	Vishay/Dale	CRCW20100000Z0EF	RES 0.0 OHM1/2W 5% 2010 SMD
145	1	J42	HEADER2X5	Samtec	TSW-105-07-T-D	5x2-0.25 Header
146	1	U29	MAX3232	Texas Instruments	MAX3232IPWR	IC DRVR/RCVR MLTCH RS232 16TSSOP
147	4	C397, C398, C399, C400	100NFX5R-0402SMT	Kemet	C0402C104K8PACTU	CAP .10UF 10V CERAMIC X5R 0402
148	1	U30	FT232	Future Technology Devices International Ltd	FTDI_FT232RL	USB Serial Converter SSOP28
149	1	C402	1UF-16V-0805SMT	Panasonic	ECJ-2FB1C105K	CAP 1UF 16V CERAMIC 0805 X5R
150	2	C403,C407	10NF-0603SMT	Kemet	C0603C103K5RACTU	CAP .01UF 50V CERAMIC X7R 0603
151	2	C404, C405	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603
152	1	R331	10K-0603SMT	Panasonic	ERJ-3GEYJ103V	RES 10K OHM 1/10W 5% 0603 SMD
153	1	J43	USB MINI AB	MOLEX	MOLEX_56579-0576	
154	1	L3	INDUCTOR	Panasonic	Inductor 1uH 10% 230mA 1210 (Digikey PCD1008CT-ND)	ELJ-FA1R0KF2
155	2	TP39, TP40	TestPoint			
156	1	J45	SMA	Molex	73391-0060	CONN JACK SMA STR 50 OHM PCB
157	1	R337	50R-0603SMT	Vishay	FC0603E50R0BTBT1	RES 50 OHM 125MW .1% 0603 SMD
158	2	C406, C408	1K-0603	Kemet	C0603C103K5RACTU	CAP .01UF 50V CERAMIC X7R 0603
159	1	C401	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603
160	2	SP25, SP26	TestPoint			
161	1	DP3	DIFFTESTPOINT			
162	2	D31, D32	GREEN_LED	Lite-On	LTST-C190GKT	
163	2	R329, R330	330R-0402SMT	Panasonic	ERJ-2GEJ331X	RES 330 OHM 1/16W 5% 0402 SMD
164	1	J41	HEADER3X2	Samtec	TSW-103-07-T-D	3x2-0.25 Header
165	1	J44	HEADER 2	Samtec	TSW-102-07-T-S	2x1-0.25 Header
166	4	R353,R354,R355,R356	1K-0603SMT	Panasonic	ERJ-3EKF1001V	RES 1.00K OHM 1/16W 1% 0603 SMD
167	2	R338, R339	62R-0603SMT	Panasonic	ERJ-3GEYJ620V	RES 62 OHM 1/10W 5% 0603 SMD
168	3	R340,R341,R342	100R-0402SMT	Panasonic	ERJ-2GEJ101X	RES 100 OHM 1/10W 5% 0402 SMD
169	4	R343,R344,R345,R347	100K-0402SMT	Panasonic	ERJ-2GEJ104X	RES 100K OHM 1/10W 5% 0402 SMD
179	1	R346	10K-0603SMT	Panasonic	ERJ-2RKF1002X	RES 10.0K OHM 1/16W 1% 0402 SMD

Table 27. Bill of Materials (Continued)

Item	Quantity	Reference	Part	Manufacturer	Part Number	Description
180	4	C418,C409,C411,C413	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603
181	5	C419,C427,C431,C220,C221	10NF-0402SMT	Panasonic	ECJ0EB1E103K	CAP .01UF 25V CERAMIC X7R 0402
182	1	U31	SN74LV125	Texas Instruments	SN74LVC125AD	IC QUAD BUS BUFFER GATE 14-SOIC
183	3	C415,C416,C417	10PF-0402SMT	Panasonic	ECJ-0EC1H100D	CAP 10PF 50V CERAMIC 0402 SMD
184	2	R350,R351	0R-0603SMT	Panasonic	ERJ-3GEY0R00V	RES ZERO OHM 1/10W 5% 0603 SMD
185	1	J48	SMA	Molex	73391-0060	CONN JACK SMA STR 50 OHM PCB
186	1	J47	HDR5	Samtec	TSW-105-07-T-S	5x1-0.25 Header
187	3	D33,D34,D35	SCHOTTKY/VISHAYV12P10	Vishay	V12P10-E3/87A	TO277 SCHOTTKY DIODE
188	6	C420,C421,C422,C423,C425,C429	10UF-16V-TANTBSMT	AVX	TAJB106K016R	CAP TANTALUM 10UF 16V 10% SMD
189	4	R357,R358,R359,R360	OPEN-0603SMT			
190	3	R348,R349,R352,R373	50R-0603SMT	Vishay	FC0603E50R0BTBT1	RES 50 OHM 125MW .1% 0603 SMD
191	8	C424,C426,C428,C430,C438,C410,C412,C414	100NF-0603SMT	Panasonic	ECJ-1VF1C104Z	CAP .1UF 16V CERAMIC Y5V 0603
192	6	R361,R362,R364,R365,R367,R368	50R-0402SMT	Vishay	FC0402E50R0BTBST1	RES 50 OHM 50MW .1% 0402 SMD
193	2	R363,R366	1_6R-0603SMT	Panasonic	ERJ-3GEYJ1R6V	RESISTOR 1.6 OHM 1/10W 5% 0603
194	2	Y6,Y7	CRYSTEK_133MHZ	Crystek	CCLD-033-50-133.000	OSC LVDS 133.0 MHZ 3.3V 7mmx5mm SMD
195	2	R256,R257	50R-0402SMT	Vishay	FC0402E50R0BTBST1	RES 50 OHM 50MW .1% 0402 SMD
196	1	R269	Do Not Populate			
197	2	R300, R301	10K-0402SMT	Panasonic	ERJ-2RKF1002X	RES 10.0K OHM 1/16W 1% 0402 SMD
198	1	R228	240R-0603SMT	Panasonic	ERA-3YEB241V	RES 240 OHM 1/16W .1% 0603 SMD