RELIABILITY REPORT

FOR

MAX13101EETL+

PLASTIC ENCAPSULATED DEVICES

January 20, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX13101EETL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX13101E/MAX13102E/MAX13103E/MAX13108E 16-bit bidirectional CMOS logic-level translators provide the level shifting necessary to allow data transfer in multivoltage systems. These devices are inherently bidirectional due to their design and do not require the use of a direction input. Externally applied voltages, VCC and VL, set the logic levels on either side of the devices. Logic signals present on the VL side of the device appear as a higher voltage logic signal on the VCC side of the device, and vice-versa. The MAX13101E/MAX13102E/MAX13103E feature an enable input (EN) that, when low, reduces the VCC and VL supply currents to less than 2µA. The MAX13108E features a multiplexing input (MULT) that selects one byte between the two, thus allowing multiplexing of the signals. The MAX13101E/MAX13102E/MAX13103E/MAX13108E have ±15kV ESD protection on the I/O VCC side for greater protection in applications that route signals externally. Three different output configurations are available during shutdown, allowing the I/O on the VCC side or the VL side to be put in a high-impedance state or pulled to ground through an internal 6k resistor. The MAX13101E/MAX13102E/MAX13103E/MAX13108E accept VCC voltages from +1.65V to +5.5V and VL voltages from +1.2V to VCC, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX13101E/MAX13102E/MAX13103E/MAX13108E are available in 36-bump WLP and 40-pin TQFN packages, and operate over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	16-Channel Buffered CMOS Logic-Level Translators
B. Process:	C6
C. Number of Device Transistors:	2280
D. Fa brication Location:	California
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	July 21, 2006

III. Packaging Information

A. Package Type:	40-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1780
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	45°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	1.7°C/W

IV. Die Information

A. Dimensions:	113 X 114 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. S ampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot SQJBBQ002A D/C 0603, Latch-up lot SQJBDQ002 D/C 0603)

The LT02-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX13101EETL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SQJDAQ001A, D/C 0509

Note 1: Life Test Data may represent plastic DIP qualification lots.