

MAX5048C

7A Sink/3A Source Current, 8ns, SOT23, MOSFET Driver

General Description

The MAX5048C is a high-speed MOSFET driver capable of sinking/sourcing 7A/3A peak currents. This device takes logic input signals and drives a large external MOSFET. The device has inverting and noninverting inputs that give the user greater flexibility in controlling the MOSFET. The device also has the features necessary to drive low-side enhancement-mode Gallium Nitride (GaN) FETs. The device features two separate outputs working in complementary mode, offering flexibility in controlling both turn-on and turn-off switching speeds.

The device has internal logic circuitry, which prevents shoot-through during output state changes. The logic inputs are protected against voltage spikes up to +14V, regardless of V+ voltage. Propagation delay time is minimized and matched between the inverting and noninverting inputs. The device has very fast switching times combined with very short propagation delays (8ns typ) making it ideal for high-frequency circuits.

The device operates from a +4V to +14V single power supply, typically consuming 0.5mA of supply current and has TTL input logic levels. This device is available in a 6-pin SOT23 package and provides an upgrade path for users of the MAX5048B.

Applications

- Power MOSFET Switching
- Switch-Mode Power Supplies
- DC-DC Converters
- Motor Control
- Power-Supply Modules

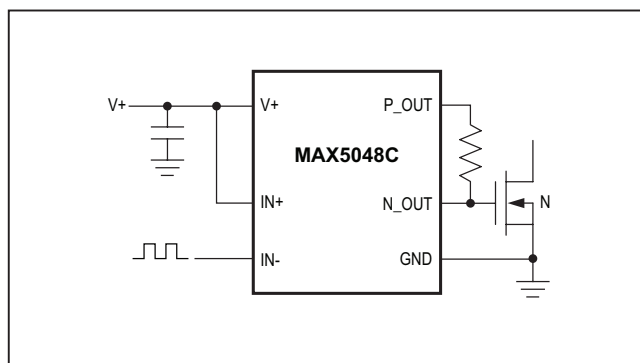
Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX5048C.related.

Features

- Independent Source/Sink Outputs for Controllable Rise and Fall Times
- +4V to +14V Single Power-Supply
- 7A/3A Peak Sink/Source Drive Current
- 0.3Ω Open-Drain n-Channel Sink Output
- 0.84Ω Open-Drain p-Channel Source Output
- Low 8ns Propagation Delay
- Matching Delay Time Between Inverting and Noninverting Inputs
- TTL Logic-Level Inputs with Hysteresis for Noise Immunity
- Inputs Rated to +14V Regardless of V+ Voltage
- Low Input Capacitance (10pF typ)
- 5ns Typical Rise and 4ns Typical Fall Times with 1nF Load
- Thermal-Shutdown Protection
- 6-Pin SOT23 Package
- -40°C to +125°C Operating Temperature Range
- Pin-Compatible with the MAX5048B

Typical Operating Circuit



Absolute Maximum Ratings

V+, IN+, IN-, P_OUT, N_OUT to GND -0.3V to +16V
 Operating Temperature Range -40°C to +125°C
 Storage Temperature Range -65°C to +150°C

Junction Temperature +150°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) 80°C/W

Note 1: Measured on the MAX5048C evaluation kit.

Electrical Characteristics

(V+ = 12V, C_L = 0, T_A = -40°C to +125°C, unless otherwise noted. Typical values are specified at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V+)						
V+ Operating Range	V+		4		14	V
V+ Undervoltage Lockout	UVLO	V+ rising	3.28	3.45	3.63	V
V+ UVLO Hysteresis				200		mV
V+ UVLO to Output Delay		V+ rising, IN+ = V+, IN- = GND		127		μs
V+ Supply Current	I+Q	Not switching, V+ = 14V		0.5	1	mA
	I+SW	V+ = 6 V, switching at 1MHz		2.65		
n-CHANNEL OUTPUT						
Driver Output Resistance Pulling Down	RON-N	V+ = 14V, IN_OUT = -100mA		0.31	0.55	Ω
		V+ = 4.5V, IN_OUT = -100mA		0.32	0.56	
Power-Off Pulldown Resistance		V+ = unconnected, IN_OUT = -10mA, TA = +25°C	4	6.1	8.5	Ω
Power-Off Pulldown Clamp Voltage		V+ = unconnected, IN_OUT = -10mA, TA = +25°C	0.95	1.29	1.65	V
Output Leakage Current	ILK-N	N_OUT = 14V		6.5	11	μA
Peak Output Current (Sinking)	IPK-N	CL = 10 nF		7		A
p-CHANNEL OUTPUT						
Driver Output Resistance Pulling Up	RON-P	V+ = 14V, IP_OUT = 100mA		0.84	1.47	Ω
		V+ = 4.5V, IP_OUT = 100mA		0.88	1.55	
Output Leakage Current	ILK-P	P_OUT = 0V	-1		+1	μA
Peak Output Current (Sourcing)	IPK-P	CL = 10nF		3		A
LOGIC INPUT (IN+, IN-)						
Logic High Input Voltage	VIH		2.0			V
Logic Low Input Voltage	VIL				0.8	V
Logic Input Hysteresis	VHYS			300		mV
Logic Input Current		IN+ = IN- = V+ or 0V, V+ = 14V	-1000		+1000	nA
Logic Input Capacitance	CIN	(Note 3)		10		pF

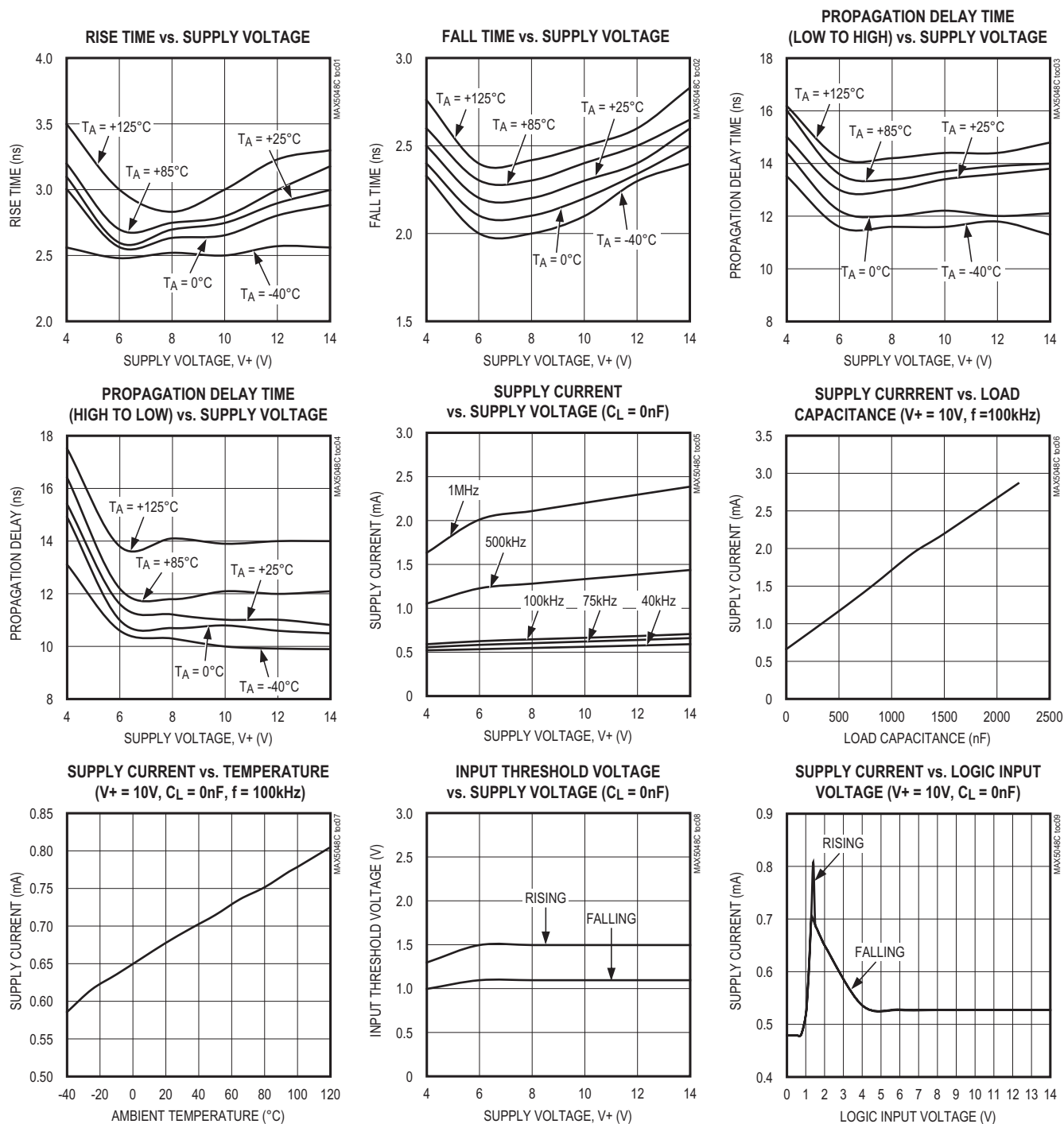
Electrical Characteristics (continued)(V+ = 12V, C_L = 0, T_A = -40°C to +125°C, unless otherwise noted. Typical values are specified at T_A = +25°C.) (Note 2)

SWITCHING CHARACTERISTICS (V+ = 14V) (Figure 2 and Note 3)						
Rise Time	t _R	C _L = 1nF	5			ns
		C _L = 4.7nF	19			
		C _L = 10nF	37			
Fall Time	t _F	C _L = 1nF	4			ns
		C _L = 4.7nF	10			
		C _L = 10nF	18			
Turn-On Delay Time	t _{D-ON}	C _L = 1nF	3	7	18	ns
Turn-Off Delay Time	t _{D-OFF}	C _L = 1nF	3	7	18	ns
Break-Before-Make Time			5			ns
SWITCHING CHARACTERISTICS (V+ = 4.5V) (Figure 2 and Note 3)						
Rise Time	t _R	C _L = 1nF	4			ns
		C _L = 4.7nF	13			
		C _L = 10nF	28			
Fall Time	t _F	C _L = 1nF	4			ns
		C _L = 4.7nF	7			
		C _L = 10nF	13			
Turn-On Delay Time	t _{D-ON}	C _L = 1nF	2	8	21	ns
Turn-Off Delay Time	t _{D-OFF}	C _L = 1nF	2	8	21	ns
Break-Before-Make Time			5			ns
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising	166			°C
Thermal Shutdown Hysteresis			13			°C

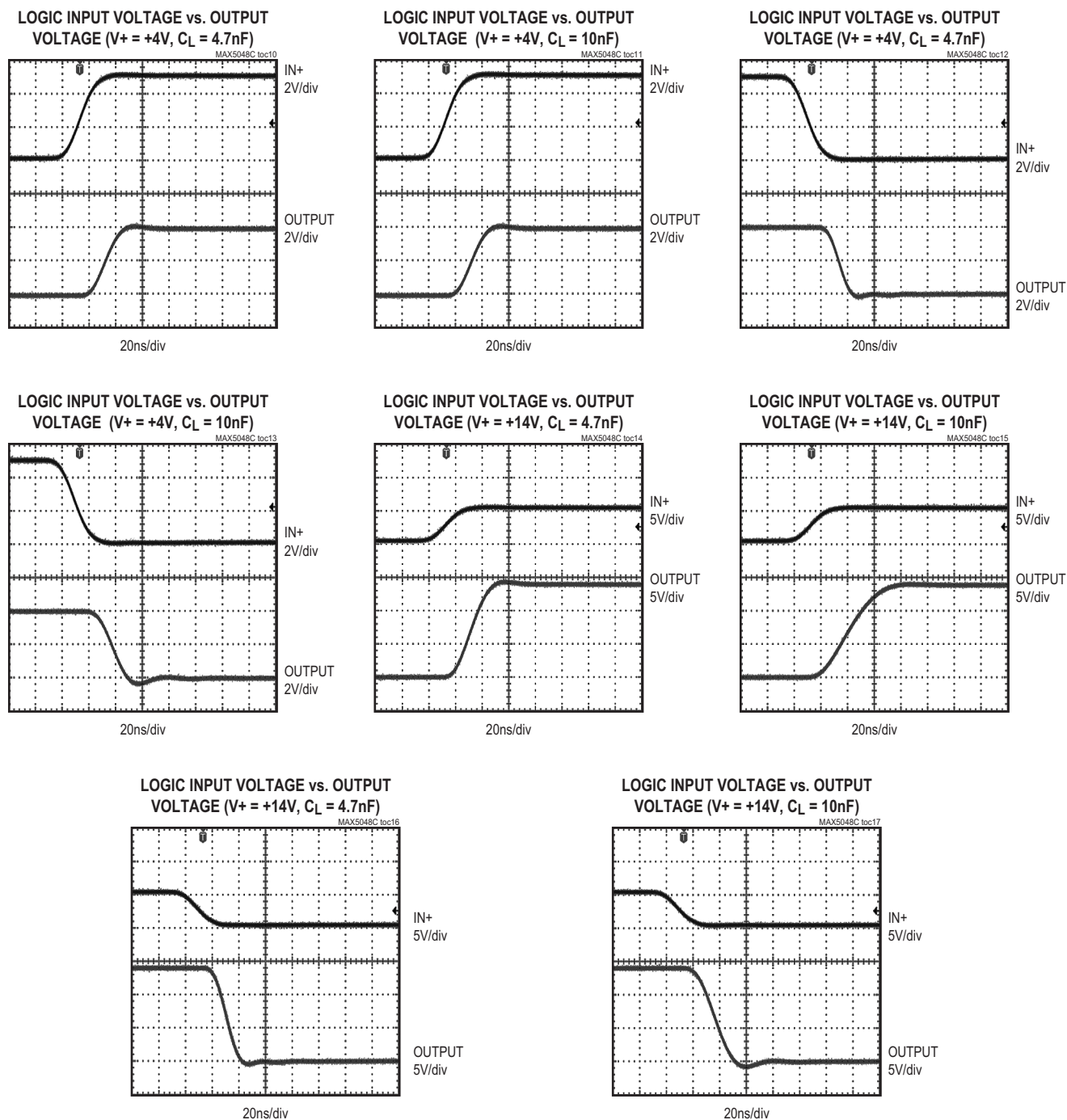
Note 2: All devices are production tested at T_A = +25°C. Limits over temperature are guaranteed by design.**Note 3:** Design guaranteed by bench characterization. Limits are not production tested.

Typical Operating Characteristics

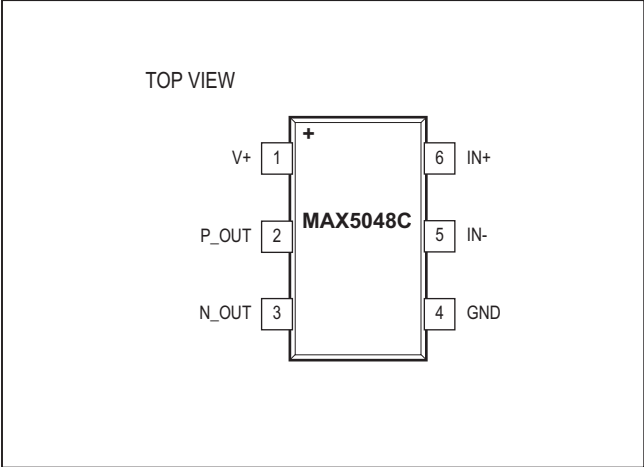
($C_L = 1\text{nF}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Typical Operating Characteristics (continued)

(C_L = 1nF, T_A = +25°C, unless otherwise noted.)

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	V+	Power-Supply Input. Bypass to GND with a minimum of 1μF low-ESR ceramic capacitor.
2	P_OUT	Open-Drain p-Channel Output. Sources current for MOSFET turn-on.
3	N_OUT	Open-Drain n-Channel Output. Sinks current for MOSFET turn-off.
4	GND	Ground
5	IN-	Inverting Logic Input Terminal. Connect to GND when not used.
6	IN+	Noninverting Logic Input Terminal. Connect to V+ when not used.

Functional Diagram

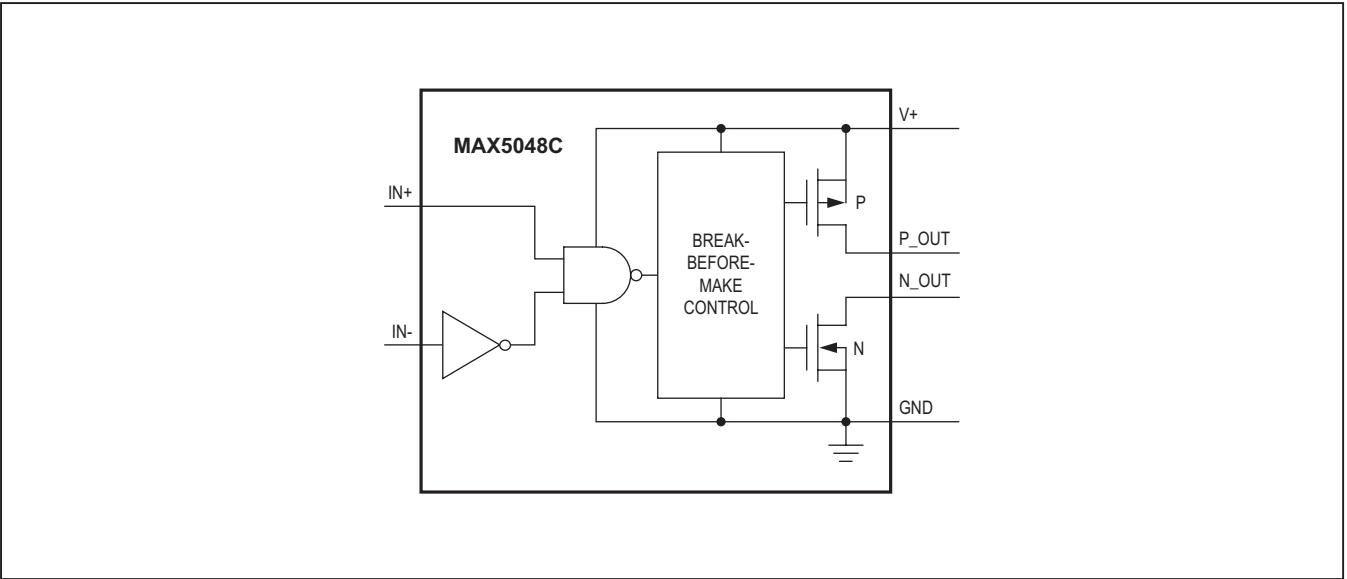


Figure 1. MAX5048C Functional Block Diagram

Timing Diagram and Test Circuit

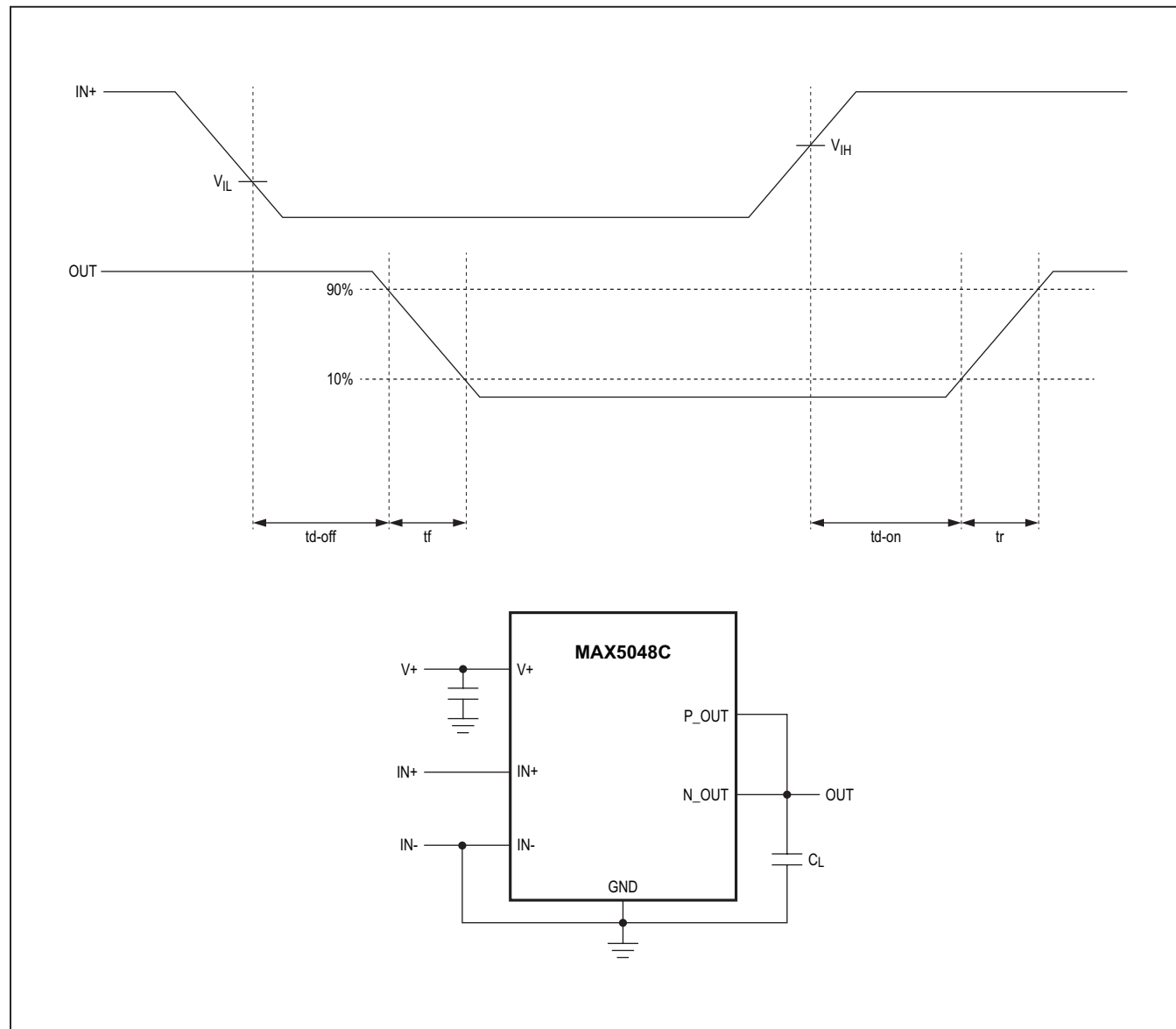


Figure 2. Timing Diagram and Test Circuit for IN+ Operation

Table 1. Truth Table

IN+	IN-	P_OUT	N_OUT
L	L	Off	On
L	H	Off	On
H	L	On	Off
H	H	Off	On

L = Logic-low.

H = Logic-high.

Detailed Description

Logic Inputs

The MAX5048C has a TTL inverting and noninverting input that gives the user greater flexibility in controlling the MOSFET. Table 1 shows all the possible input combinations and the corresponding output states.

Undervoltage Lockout (UVLO)

When V+ is below the UVLO threshold, the output-stage n-channel device is on and the p-channel is off, independent of the state of the inputs. This holds the outputs low. The UVLO is typically 3.45V with 200mV typical hysteresis to avoid chattering.

Driver Outputs

The device provides two separate outputs. One is an open-drain p-channel, the other an open-drain n-channel. They have distinct current sourcing/sinking capabilities to independently control the rise and fall times of the MOSFET gate. Add a resistor in series with P_OUT/N_OUT to slow the corresponding rise/fall time of the MOSFET gate.

Applications Information

Supply Bypassing, Device Grounding, and Placement

Ample supply bypassing and device grounding are extremely important because when large external capacitive loads are driven, the peak current at the V+ pin can approach 3A, while at the GND pin the peak current can approach 7A. V+ drops and ground shifts are forms of negative feedback for inverters and, if excessive, can cause multiple switching when the inverting input is used and the input slew rate is low. The device driving the input should be referenced to the GND pin, especially when the inverting input is used. Ground shifts due to insufficient device grounding may disturb other circuits sharing the same AC ground return path. Any series inductance in

the V+, P_OUT, N_OUT, and/or GND paths can cause oscillations due to the very high di/dt that results when the device is switched with any capacitive load. A minimum of 1μF, low-ESR ceramic capacitor is recommended, bypassing V+ to GND and placed as close as possible to the pins. When driving very large loads (e.g., 10nF) at minimum rise time, 10μF or more of parallel storage capacitance is recommended. A ground plane is highly recommended to minimize ground return resistance and series inductance. Care should be taken to place the device as close as possible to the external MOSFET being driven to further minimize board inductance and AC path resistance.

Power Dissipation

Power dissipation of the device consists of three components, caused by the quiescent current, capacitive charge and discharge of internal nodes, and the output current (either capacitive or resistive load). The sum of these components must be kept below the maximum power-dissipation limit corresponding value.

The quiescent current is 0.5mA (typ). The current required to charge and discharge the internal nodes is frequency dependent (see the *Typical Operating Characteristics*). The device's approximate power dissipation when driving a ground-referenced resistive load is:

$$P = D \times R_{ON} (MAX) \times I_{LOAD}^2$$

where D is the fraction of the period that the device output pulls high, $R_{ON} (MAX)$ is the maximum pullup on-resistance of the device with the output high, and I_{LOAD} is the output load current of the device.

For capacitive loads, the approximate power dissipation is:

$$P = C_{LOAD} \times (V+)^2 \times FREQ$$

where C_{LOAD} is the capacitive load, V+ is the supply voltage, and FREQ is the switching frequency.

PCB Layout Information

The MOSFET driver can source and sink large currents to create very fast rise and fall edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PCB layout guidelines are recommended when designing with the MAX5048C:

- Place at least 1μF decoupling ceramic capacitor from V+ to GND as close as possible to the device. At least one storage capacitor of 10μF (min) should be located on the PCB with a low resistance path to the V+ pin of the device.

- There are two AC current loops formed between the device and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from N_OUT of the device to the MOSFET gate, to the MOSFET source, and to GND of the device.
- When the gate of the MOSFET is being pulled high, the active current loop is from P_OUT of the device, to the MOSFET gate, to the MOSFET source, to the

GND terminal of the decoupling capacitor, to the V+ terminal of the decoupling capacitor, and to the V+ terminal of the device. While the charging current loop is important, the discharging current loop is also critical. It is important to minimize the physical distance and the impedance in these AC current loops.

- In a multilayer PCB, the component surface layer surrounding the device should consist of a GND plane containing the discharging and charging current loops.

Typical Application Circuits

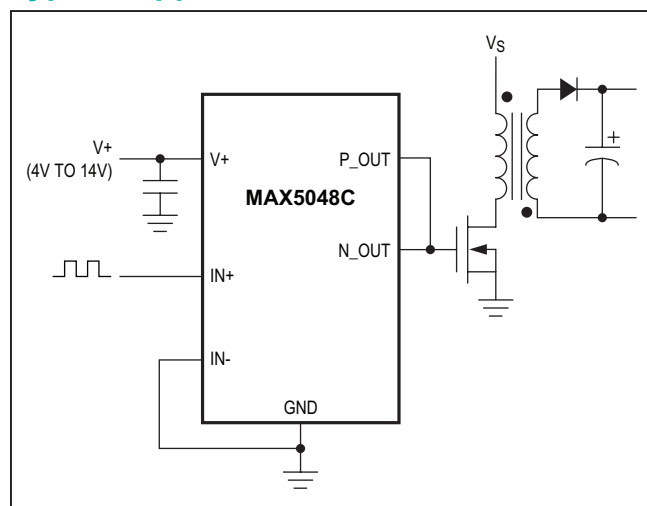


Figure 3. Noninverting Application

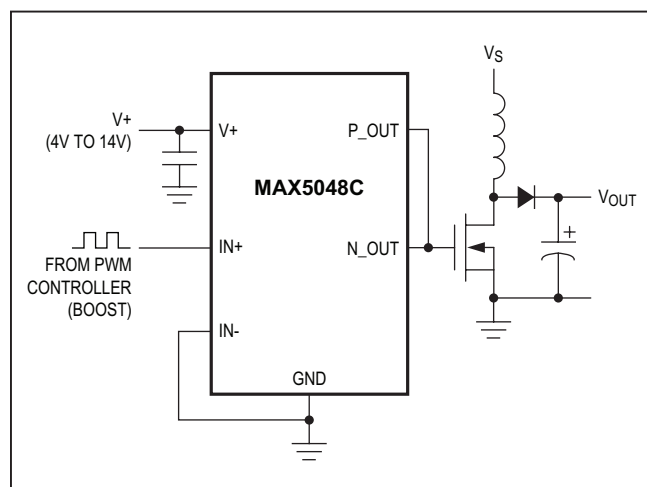


Figure 4. Boost Converter

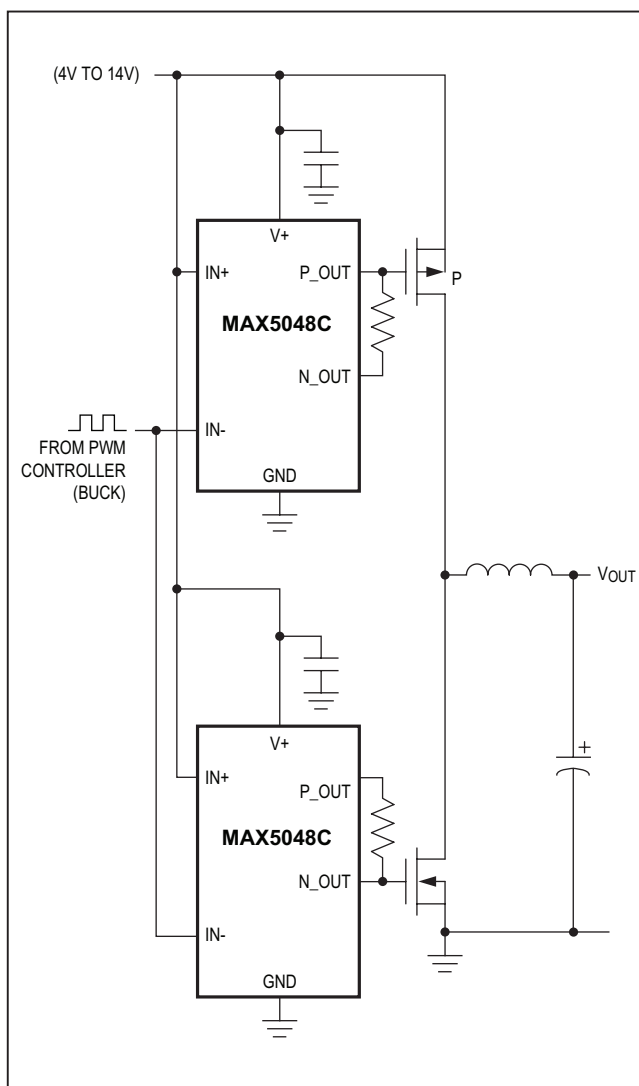


Figure 5. MAX5048C in High-Power Synchronous Buck Converter

MAX5048C

7A Sink/3A Source Current, 8ns,
SOT23, MOSFET Driver

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	LOGIC INPUT	TOP MARK
MAX5048CAUT+	-40°C to +125°C	6 SOT23	TTL	+ACSC

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SOT23	U6+8	21-0058	90-0175

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7A Sink/3A Source Current, 8ns,
SOT23, MOSFET Driver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	11/12	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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