# MAX5703/MAX5704/MAX5705

# Ultra-Small, Single-Channel, 8-/10-/12-Bit Buffered Output Voltage DACs with Internal Reference and SPI Interface

## General Description

The MAX5703/MAX5704/MAX5705 single-channel, low-power, 8-/10-/12-bit, voltage-output digital-to-analog converters (DACs) include output buffers and an internal reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5703/MAX5704/MAX5705 accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (< 1mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a 100kΩ (typ) load to an external reference.

The MAX5703/MAX5704/MAX5705 have a 50MHz, 3-wire SPI/QSPI™/MICROWIRE®/DSP-compatible serial interface. The DAC output is buffered and has a low supply current of 155µA (typical at 3V) and a low offset error of ±0.5mV (typical). On power-up, the MAX5703/MAX5704/MAX5705 reset the DAC outputs to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The internal reference is initially powered down to allow use of an external reference.

The MAX5703/MAX5704/MAX5705 include a user-configurable active-low asynchronous input, $\overline{AUX}$ for additional flexibility. This input can be programmed to asynchronously clear ($\overline{CLR}$) or temporarily gate ($\overline{GATE}$) the DAC output to a user-programmable value. A dedicated active-low asynchronous $\overline{LDAC}$ input is also included. This allows simultaneous output updates of multiple devices.

The MAX5703/MAX5704/MAX5705 are available in 10-pin TDFN/µMAX® packages and are specified over the -40°C to +125°C temperature range.

## Applications

Programmable Voltage and Current Sources

Gain and Offset Adjustment

Automatic Tuning and Optical Control

Power Amplifier Control and Biasing

Process Control and Servo Loops

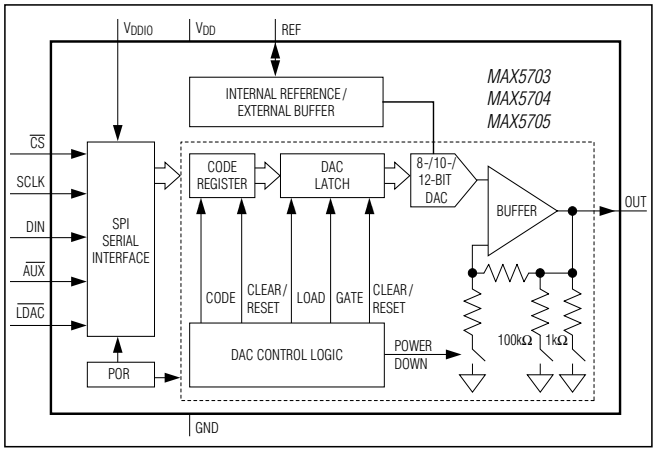
Portable Instrumentation

Data Acquisition

## Benefits and Features

- **Single High-Accuracy DAC Channel**
  - ✧ **12-Bit Accuracy Without Adjustments**
  - ✧ **±1 LSB INL Buffered Voltage Output**
  - ✧ **Monotonic Over All Operating Conditions**
- **Three Precision Selectable Internal References**
  - ✧ **2.048V, 2.500V, or 4.096V**
- **Internal Output Buffer**
  - ✧ **Rail-to-Rail Operation with External Reference**
  - ✧ **6.3µs Settling Time**
  - ✧ **Output Directly Drives 2kΩ Loads**
- **Small, 10-Pin, 2mm x 3mm TDFN and 3mm x 5mm µMAX Packages**
- **Wide 2.7V to 5.5V Supply Range**
- **Flexible 1.8V to 5.5V $V_{DDIO}$**
- **50MHz, 3-Wire, SPI/QSPI/MICROWIRE/DSP-Compatible Serial Interface**
- **Power-On-Reset to Zero-Scale DAC Output**
- **User-Configurable Asynchronous I/O Functions: $\overline{CLR}$, $\overline{LDAC}$, $\overline{GATE}$**
- **Three Software-Selectable Power-Down Output Impedances: 1kΩ, 100kΩ, or High Impedance**
- **Low 155µA DAC Supply Current at 3V**

## Functional Diagram

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*MICROWIRE is a registered trademark of National Semiconductor Corp.*
*µMAX is a registered trademark of Maxim Integrated Products, Inc.*

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to:* **www.maximintegated.com/MAX5703.related**

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.**

*19-6463; Rev 2; 6/13*

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND.....-0.3V to +6V
$V_{DDIO}$ to GND .....-0.3V to +6V
OUT, REF to GND .....-0.3V to lower of ($V_{DD}$ + 0.3V) and +6V
$\overline{CS}$, SCLK, DIN, $\overline{AUX}$, $\overline{LDAC}$ to GND.....-0.3V to +6V
Continuous Power Dissipation ($T_A$ = +70°C)
TDFN (derate 14.9mW/°C above +70°C).....1188.7mW
µMAX (derate 8.8mW/°C above +70°C) .....707.3mW

Maximum Continuous Current into Any Pin ..... ±50mA
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....67.3°C/W
µMAX
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....113.1°C/W
Junction-to-Ambient Thermal Resistance ($\theta_{JC}$).....36°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegated.com/thermal-tutorial**.

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 2.7V to 5.5V, $V_{DDIO}$ = 1.8V to 5.5V, $V_{GND}$ = 0V, $C_L$ = 200pF, $R_L$ = 2kΩ , $T_A$ = -40°C to +125°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC PERFORMANCE (Note 3)** | | | | | | |
| Resolution and Monotonicity | N | MAX5703 | 8 | | | Bits |
| | | MAX5704 | 10 | | | |
| | | MAX5705 | 12 | | | |
| Integral Nonlinearity (Note 4) | INL | MAX5703, 8 bits | -0.25 | ±0.05 | +0.25 | LSB |
| | | MAX5704, 10 bits | -0.5 | ±0.2 | +0.5 | |
| | | MAX5705, 12 bits | -1 | ±0. 5 | +1 | |
| Differential Nonlinearity (Note 4) | DNL | MAX5703, 8 bits | -0.25 | ±0.05 | +0.25 | LSB |
| | | MAX5704, 10 bits | -0.5 | ±0.1 | +0.5 | |
| | | MAX5705, 12 bits | -1 | ±0.2 | +1 | |
| Offset Error (Note 5) | OE | | -5 | ±0.5 | +5 | mV |
| Offset Error Drift | | | | ±10 | | µV/°C |
| Gain Error (Note 5) | GE | | -1.0 | ±0.1 | +1.0 | %FS |
| Gain Temperature Coefficient | | With respect to $V_{REF}$ | | ±2.5 | | ppm of FS/°C |
| Zero-Scale Error | | | 0 | | +10 | mV |
| Full-Scale Error | | With respect to $V_{REF}$ | -0.5 | | +0.5 | %FS |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 2.7V to 5.5V, $V_{DDIO}$ = 1.8V to 5.5V, $V_{GND}$ = 0V, $C_L$ = 200pF, $R_L$ = 2kΩ , $T_A$ = -40°C to +125°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DAC OUTPUT CHARACTERISTICS** | | | | | | | |
| Output Voltage Range (Note 6) | | No load | | 0 | | $V_{DD}$ | V |
| | | 2kΩ load to GND | | 0 | | $V_{DD}$ - 0.2 | |
| | | 2kΩ load to $V_{DD}$ | | 0.2 | | $V_{DD}$ | |
| Load Regulation | | $V_{OUT}$ = $V_{FS}$/2 | $V_{DD}$ = 3V ±10%, $\|I_{OUT}\| \leq$ 5mA | | 300 | | µV/mA |
| | | | $V_{DD}$ = 5V ±10%, $\|I_{OUT}\| \leq$ 10mA | | 300 | | |
| DC Output Impedance | | $V_{OUT}$ = $V_{FS}$/2 | $V_{DD}$ = 3V ±10%, $\|I_{OUT}\| \leq$ 5mA | | 0.3 | | Ω |
| | | | $V_{DD}$ = 5V ±10%, $\|I_{OUT}\| \leq$ 10mA | | 0.3 | | |
| Capacitive Load Handling | $C_L$ | | | | 500 | | pF |
| Resistive Load Handling | $R_L$ | | | 2 | | | kΩ |
| Short-Circuit Output Current | | $V_{DD}$ = 5.5V | Sourcing (output short to GND) | | 30 | | mA |
| | | | Sinking (output shorted to $V_{DD}$) | | 40 | | |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Voltage-Output Slew Rate | SR | Positive and negative | | | 2.0 | | V/µs |
| Voltage-Output Settling Time | | ¼ scale to ¾ scale, to ≤ 1 LSB, MAX5703 | | | 2.8 | | µs |
| | | ¼ scale to ¾ scale, to ≤ 1 LSB, MAX5704 | | | 5.2 | | |
| | | ¼ scale to ¾ scale, to ≤ 1 LSB, MAX5705 | | | 6.3 | | |
| DAC Glitch Impulse | | Major code transition | | | 5.0 | | nV·s |
| Digital Feedthrough | | Code = 0, all digital inputs from 0V to $V_{DDIO}$ | | | 0.5 | | nV·s |
| Power-Up Time | | Startup calibration time (Note 7) | | | 200 | | µs |
| | | From power-down mode | | | 60 | | µs |
| DC Power-Supply Rejection | | $V_{DD}$ = 3V ±10% or 5V ±10% | | | 100 | | µV/V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 2.7V to 5.5V, $V_{DDIO}$ = 1.8V to 5.5V, $V_{GND}$ = 0V, $C_L$ = 200pF, $R_L$ = 2kΩ , $T_A$ = -40°C to +125°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Voltage-Noise Density (DAC Output at Midscale) | | External reference | f = 1kHz | | 88 | | nV/√Hz |
| | | | f = 10kHz | | 79 | | |
| | | 2.048V internal reference | f = 1kHz | | 108 | | |
| | | | f = 10kHz | | 98 | | |
| | | 2.5V internal reference | f = 1kHz | | 117 | | |
| | | | f = 10kHz | | 110 | | |
| | | 4.096V internal reference | f = 1kHz | | 152 | | |
| | | | f = 10kHz | | 145 | | |
| Integrated Output Noise (DAC Output at Midscale) | | External reference | f = 0.1Hz to 10Hz | | 10 | | $\mu V_{P-P}$ |
| | | | f = 0.1Hz to 10kHz | | 72 | | |
| | | | f = 0.1Hz to 300kHz | | 298 | | |
| | | 2.048V internal reference | f = 0.1Hz to 10Hz | | 11 | | |
| | | | f = 0.1Hz to 10kHz | | 89 | | |
| | | | f = 0.1Hz to 300kHz | | 370 | | |
| | | 2.5V internal reference | f = 0.1Hz to 10Hz | | 12 | | |
| | | | f = 0.1Hz to 10kHz | | 99 | | |
| | | | f = 0.1Hz to 300kHz | | 355 | | |
| | | 4.096V internal reference | f = 0.1Hz to 10Hz | | 13 | | |
| | | | f = 0.1Hz to 10kHz | | 128 | | |
| | | | f = 0.1Hz to 300kHz | | 400 | | |
| Output Voltage-Noise Density (DAC Output at Full Scale) | | External reference | f = 1kHz | | 113 | | nV/√Hz |
| | | | f = 10kHz | | 100 | | |
| | | 2.048V internal reference | f = 1kHz | | 172 | | |
| | | | f = 10kHz | | 157 | | |
| | | 2.5V internal reference | f = 1kHz | | 195 | | |
| | | | f = 10kHz | | 180 | | |
| | | 4.096V internal reference | f = 1kHz | | 279 | | |
| | | | f = 10kHz | | 258 | | |
| Integrated Output Noise (DAC Output at Full Scale) | | External reference | f = 0.1Hz to 10Hz | | 12 | | $\mu V_{P-P}$ |
| | | | f = 0.1Hz to 10kHz | | 88 | | |
| | | | f = 0.1Hz to 300kHz | | 280 | | |
| | | 2.048V internal reference | f = 0.1Hz to 10Hz | | 14 | | |
| | | | f = 0.1Hz to 10kHz | | 135 | | |
| | | | f = 0.1Hz to 300kHz | | 530 | | |
| | | 2.5V internal reference | f = 0.1Hz to 10Hz | | 15 | | |
| | | | f = 0.1Hz to 10kHz | | 160 | | |
| | | | f = 0.1Hz to 300kHz | | 550 | | |
| | | 4.096V internal reference | f = 0.1Hz to 10Hz | | 23 | | |
| | | | f = 0.1Hz to 10kHz | | 220 | | |
| | | | f = 0.1Hz to 300kHz | | 610 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 2.7V to 5.5V, $V_{DDIO}$ = 1.8V to 5.5V, $V_{GND}$ = 0V, $C_L$ = 200pF, $R_L$ = 2kΩ , $T_A$ = -40°C to +125°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **REFERENCE INPUT** | | | | | | | |
| Reference Input Range | $V_{REF}$ | | | 1.24 | | $V_{DD}$ | V |
| Reference Input Current | $I_{REF}$ | $V_{REF}$ = $V_{DD}$ = 5.5V | | | 55 | 75 | µA |
| Reference Input Impedance | $R_{REF}$ | | | 75 | 100 | | kΩ |
| **REFERENCE OUPUT** | | | | | | | |
| Reference Output Voltage | $V_{REF}$ | $V_{REF}$ = 2.048V, $T_A$ = +25°C | | 2.043 | 2.048 | 2.053 | V |
| | | $V_{REF}$ = 2.5V, $T_A$ = +25°C | | 2.494 | 2.500 | 2.506 | |
| | | $V_{REF}$ = 4.096V, $T_A$ = +25°C | | 4.086 | 4.096 | 4.106 | |
| Reference Output Noise Density | | $V_{REF}$ = 2.048V | f = 1kHz | | 129 | | nV/√Hz |
| | | | f = 10kHz | | 122 | | |
| | | $V_{REF}$ = 2.500V | f = 1kHz | | 158 | | |
| | | | f = 10kHz | | 151 | | |
| | | $V_{REF}$ = 4.096V | f = 1kHz | | 254 | | |
| | | | f = 10kHz | | 237 | | |
| Integrated Reference Output Noise | | $V_{REF}$ = 2.048V | f = 0.1Hz to 10Hz | | 12 | | $µV_{P-P}$ |
| | | | f = 0.1Hz to 10kHz | | 110 | | |
| | | | f = 0.1Hz to 300kHz | | 390 | | |
| | | $V_{REF}$ = 2.500V | f = 0.1Hz to 10Hz | | 15 | | |
| | | | f = 0.1Hz to 10kHz | | 129 | | |
| | | | f = 0.1Hz to 300kHz | | 430 | | |
| | | $V_{REF}$ = 4.096V | f = 0.1Hz to 10Hz | | 20 | | |
| | | | f = 0.1Hz to 10kHz | | 205 | | |
| | | | f = 0.1Hz to 300kHz | | 525 | | |
| Reference Temperature Coefficient (Note 8) | | MAX5705A | | | ±4 | ±12 | ppm/°C |
| | | MAX5703/MAX5704/MAX5705B | | | ±10 | ±25 | |
| Reference Drive Capacity | | External load | | | 25 | | kΩ |
| Reference Capacitive Load Handling | | | | | 200 | | pF |
| Reference Load Regulation | | $I_{SOURCE}$ = 0 to 500µA | | | 1.0 | | mV/mA |
| Reference Line Regulation | | | | | 0.1 | | mV/V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 2.7V to 5.5V, $V_{DDIO}$ = 1.8V to 5.5V, $V_{GND}$ = 0V, $C_L$ = 200pF, $R_L$ = 2kΩ , $T_A$ = -40°C to +125°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER REQUIREMENTS** | | | | | | | |
| Supply Voltage | $V_{DD}$ | $V_{REF}$ = 4.096V | | 4.5 | | 5.5 | V |
| | | All other options | | 2.7 | | 5.5 | |
| I/O Supply Voltage | $V_{DDIO}$ | | | 1.8 | | 5.5 | V |
| Supply Current (DAC Output at Midscale) (Note 9) | $I_{DD}$ | External reference | $V_{REF}$ = 3V | | 135 | 190 | µA |
| | | | $V_{REF}$ = 5V | | 165 | 225 | |
| | | Internal reference, reference pin undriven | $V_{REF}$ = 2.048V | | 190 | 265 | |
| | | | $V_{REF}$ = 2.5V | | 205 | 280 | |
| | | | $V_{REF}$ = 4.096V | | 250 | 340 | |
| | | Internal reference, reference pin driven | $V_{REF}$ = 2.048V | | 215 | 300 | |
| | | | $V_{REF}$ = 2.5V | | 225 | 315 | |
| | | | $V_{REF}$ = 4.096V | | 275 | 375 | |
| Supply Current (DAC Output at Full Scale) (Note 9) | $I_{DD}$ | External reference | $V_{REF}$ = 3V | | 155 | 210 | µA |
| | | | $V_{REF}$ = 5V | | 200 | 265 | |
| | | Internal reference, reference pin undriven | $V_{REF}$ = 2.048V | | 205 | 280 | |
| | | | $V_{REF}$ = 2.5V | | 220 | 300 | |
| | | | $V_{REF}$ = 4.096V | | 275 | 375 | |
| | | Internal reference, reference pin driven | $V_{REF}$ = 2.048V | | 225 | 310 | |
| | | | $V_{REF}$ = 2.5V | | 240 | 330 | |
| | | | $V_{REF}$ = 4.096V | | 300 | 410 | |
| Power-Down Mode Supply Current (DAC Powered Down, Reference Remains Active) (Note 9) | $I_{DD}$ | Internal reference, reference pin driven | $V_{REF}$ = 2.048V | | 90 | 135 | µA |
| | | | $V_{REF}$ = 2.5V | | 93 | 135 | |
| | | | $V_{REF}$ = 4.096V | | 100 | 150 | |
| Power-Down Mode Supply Current (Note 9) | $I_{PD}$ | External reference, $V_{DD}$ = $V_{REF}$ | | | 0.4 | 2 | µA |
| Digital Supply Current (Note 9) | $I_{DDIO}$ | | | | | 1.0 | µA |
| **DIGITAL INPUT CHARACTERISTICS (CS, SCLK, DIN, LDAC, AUX)** | | | | | | | |
| Input High Voltage | $V_{IH}$ | 2.2V < $V_{DDIO}$ < 5.5V | | 0.7 x $V_{DDIO}$ | | | V |
| | | 1.8V < $V_{DDIO}$ < 2.2V | | 0.8 x $V_{DDIO}$ | | | |
| Input Low Voltage | $V_{IL}$ | 2.2V < $V_{DDIO}$ < 5.5V | | | | 0.3 x $V_{DDIO}$ | V |
| | | 1.8V < $V_{DDIO}$ < 2.2V | | | | 0.2 x $V_{DDIO}$ | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 2.7V to 5.5V, $V_{DDIO}$ = 1.8V to 5.5V, $V_{GND}$ = 0V, $C_L$ = 200pF, $R_L$ = 2kΩ , $T_A$ = -40°C to +125°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Hysteresis Voltage | $V_H$ | | | | 0.15 | | V |
| Input Leakage Current (Note 9) | $I_{IN}$ | | | | ±0.1 | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | | 3 | | pF |
| **SPI TIMING CHARACTERISTICS ($\overline{CS}$, SCLK, DIN, $\overline{LDAC}$, $\overline{AUX}$) (Note 10)** | | | | | | | |
| SCLK Frequency | | $2.7V \le V_{DDIO} \le 5.5V$ | | 0 | | 50 | MHz |
| | | $1.8V \le V_{DDIO} < 2.7V$ | | 0 | | 33 | |
| SCLK Period | $t_{SCLK}$ | $2.7V \le V_{DDIO} \le 5.5V$ | | 20 | | | ns |
| | | $1.8V \le V_{DDIO} < 2.7V$ | | 30 | | | |
| SCLK Pulse Width High | $t_{CH}$ | | | 8 | | | ns |
| SCLK Pulse Width Low | $t_{CL}$ | | | 8 | | | ns |
| $\overline{CS}$ Fall to SCLK Fall Setup Time | $t_{CSS0}$ | To first SCLK falling edge | $2.7V \le V_{DDIO} \le 5.5V$ | 8 | | | ns |
| | | | $1.8V \le V_{DDIO} < 2.7V$ | 12 | | | |
| $\overline{CS}$ Fall to SCLK Fall Hold Time | $t_{CSH0}$ | Applies to inactive SCLK falling edge preceding the first SCLK falling edge | | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Fall Hold Time | $t_{CSH1}$ | Applies to the 24th SCLK falling edge | | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Fall | $t_{CSA}$ | Applies to the 24th SCLK falling edge, aborted sequence | | 12 | | | ns |
| SCLK Fall to $\overline{CS}$ Fall | $t_{CSF}$ | Applies to 24th SCLK falling edge | | 100 | | | ns |
| $\overline{CS}$ Pulse Width High | $t_{CSPW}$ | | | 20 | | | ns |
| DIN to SCLK Fall Setup Time | $t_{DS}$ | | | 5 | | | ns |
| DIN to SCLK Fall Hold Time | $t_{DH}$ | | | 4.5 | | | ns |
| CLR Pulse Width Low | $t_{CLPW}$ | | | 20 | | | ns |
| CLR Rise to $\overline{CS}$ Fall | $t_{CSC}$ | Required for command to be executed | | 20 | | | ns |
| $\overline{LDAC}$ Pulse Width Low | $t_{LDPW}$ | | | 20 | | | ns |
| $\overline{LDAC}$ Fall to SCLK Fall Hold | $t_{LDH}$ | Applies to 24th SCLK falling edge | | 20 | | | ns |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 2.7V to 5.5V, $V_{DDIO}$ = 1.8V to 5.5V, $V_{GND}$ = 0V, $C_L$ = 200pF, $R_L$ = 2kΩ , $T_A$ = -40°C to +125°C, unless otherwise noted.) (Note 2)

**Note 2:** Electrical specifications are production tested at $T_A$ = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at $T_A$ = +25°C.
**Note 3:** DC Performance is tested without load.
**Note 4:** Linearity is tested with unloaded outputs to within 20mV of GND and $V_{DD}$.
**Note 5:** Gain and offset calculated from measurements made with $V_{REF}$ = $V_{DD}$ at code 30 and 4065 for MAX5705, code 8 and 1016 for MAX5704, and code 2 and 254 for MAX5703.
**Note 6:** Subject to zero and full-scale error limits and $V_{REF}$ settings.
**Note 7:** On power-up, the device initiates an internal 200µs (typ) calibration sequence. All commands issued during this time will be ignored.
**Note 8:** Specification is guaranteed by design and characterization.
**Note 9:** Static logic inputs with $V_{IL}$ = $V_{GND}$ and $V_{IH}$ = $V_{DDIO}$.
**Note 10:** All timing is tested with $V_{IL}$ = $V_{GND}$ and $V_{IH}$ = $V_{DDIO}$.

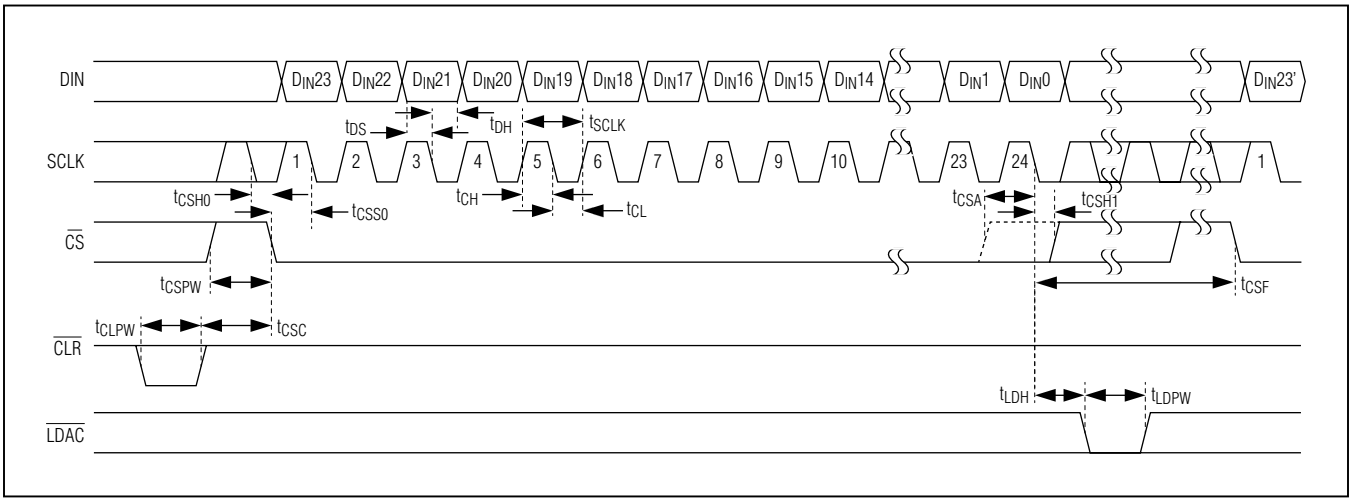
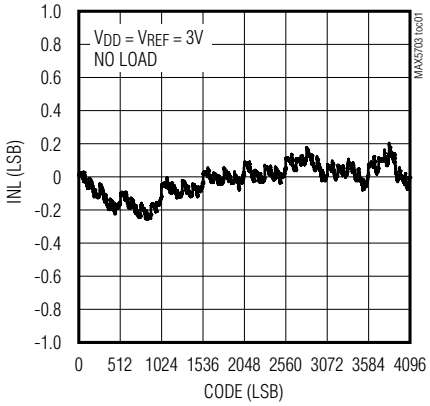



*Figure 1. SPI Serial Interface Timing Diagram*

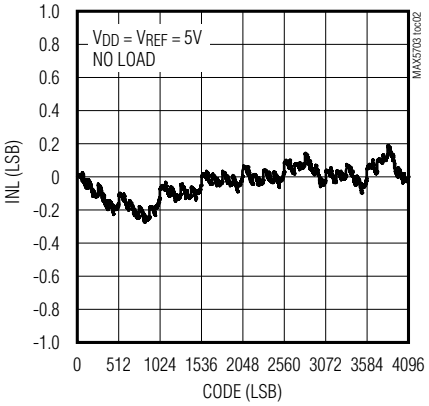
## Typical Operating Characteristics

(MAX5705, 12-bit performance, $T_A$ = +25°C, unless otherwise noted.)

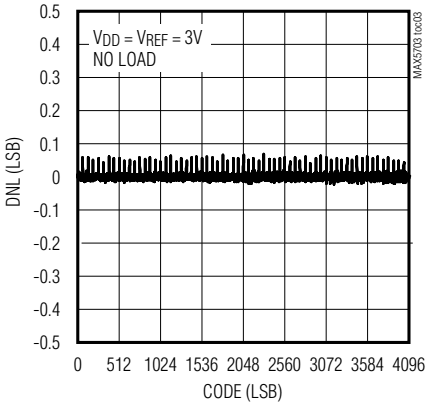
**INL vs. CODE**



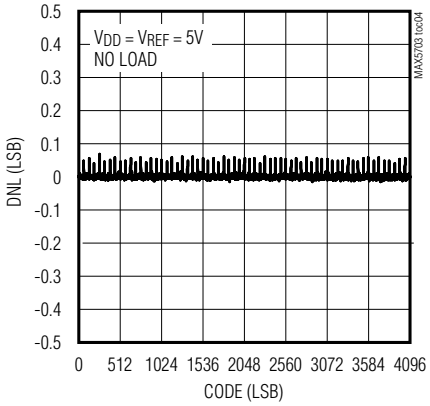

**INL vs. CODE**



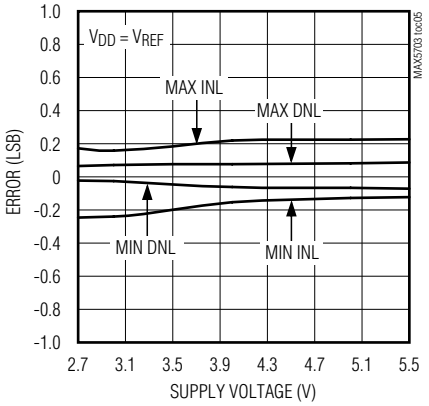

**DNL vs. CODE**



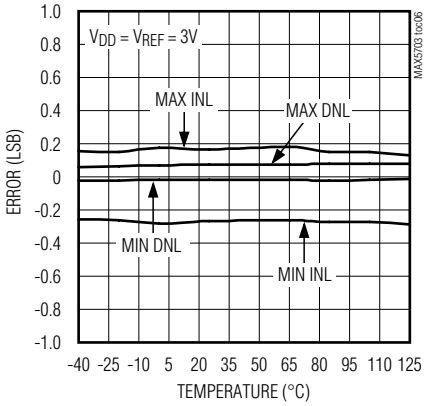

**DNL vs. CODE**



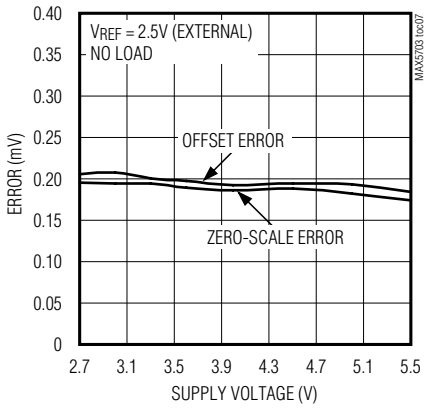

**INL AND DNL vs. SUPPLY VOLTAGE**



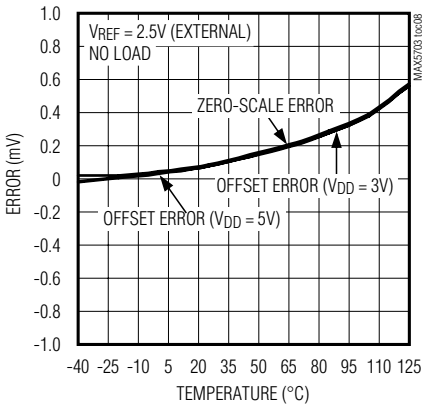

**INL AND DNL vs. TEMPERATURE**



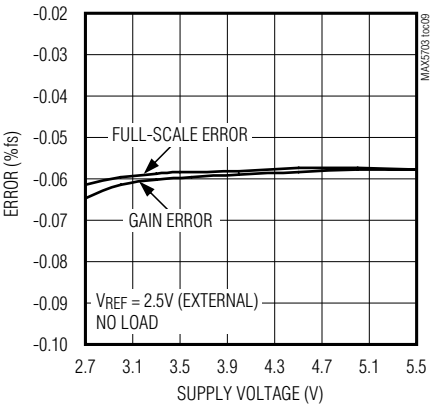

**OFFSET AND ZERO-SCALE ERROR vs. SUPPLY VOLTAGE**




**OFFSET AND ZERO-SCALE ERROR vs. TEMPERATURE**



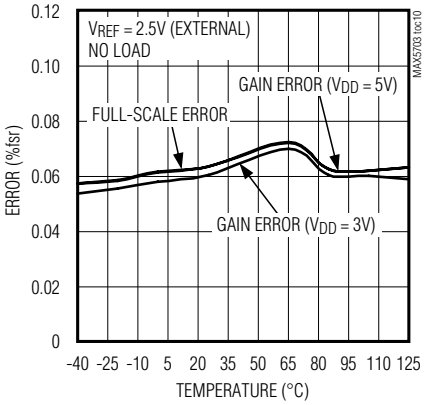

**FULL-SCALE ERROR AND GAIN ERROR vs. SUPPLY VOLTAGE**



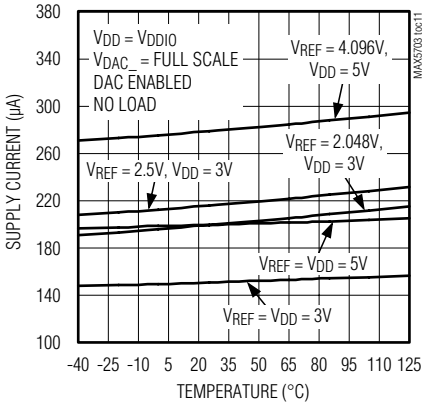
## *Typical Operating Characteristics (continued)*

(MAX5705, 12-bit performance, $T_A$ = +25°C, unless otherwise noted.)

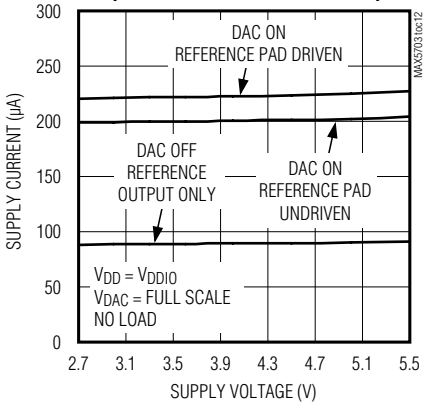
**FULL-SCALE ERROR AND GAIN ERROR vs. TEMPERATURE**



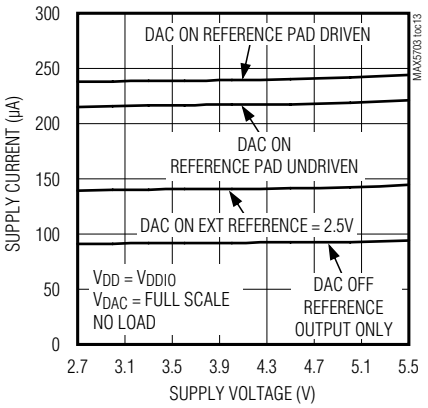

**SUPPLY CURRENT vs. TEMPERATURE (PIN UNDRIVEN FOR INTERNAL REF MODES)**



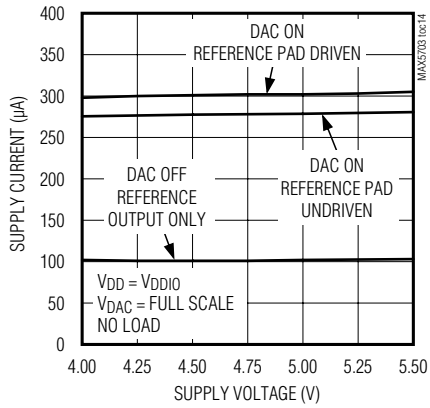

**SUPPLY CURRENT vs. SUPPLY VOLTAGE (2.048V INTERNAL REFERENCE)**



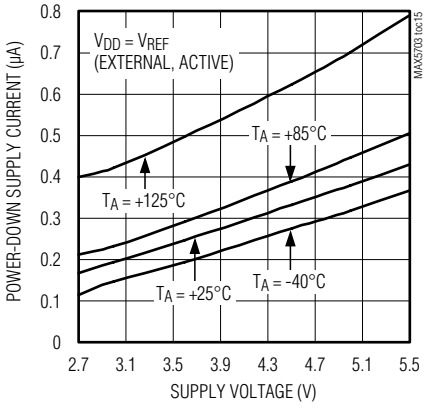

**SUPPLY CURRENT vs. SUPPLY VOLTAGE (2.500V INTERNAL REFERENCE)**



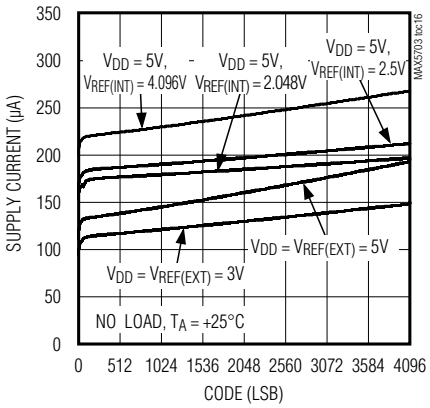

**SUPPLY CURRENT vs. SUPPLY VOLTAGE (4.096V INTERNAL REFERENCE)**



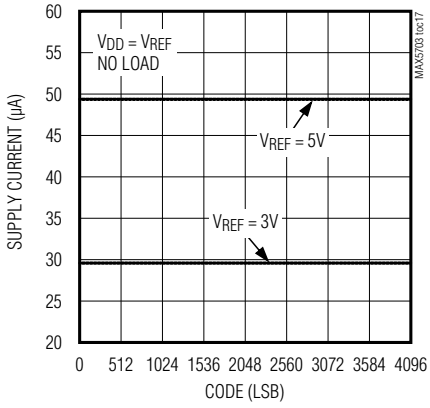

**POWER-DOWN MODE CURRENT vs. SUPPLY VOLTAGE**




**SUPPLY CURRENT vs. CODE (FOR INTERNAL REF, PIN IS UNDRIVEN)**



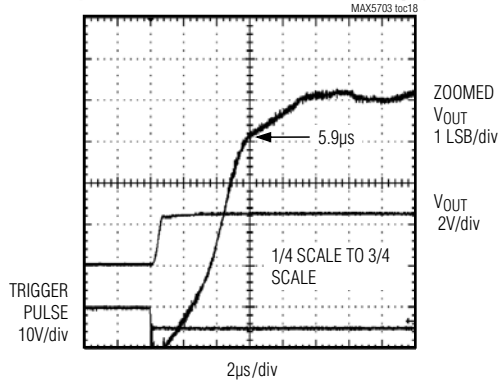

**IREF (EXTERNAL) vs. CODE**



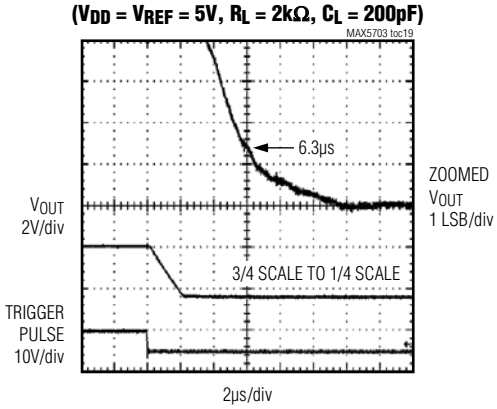
## *Typical Operating Characteristics (continued)*

(MAX5705, 12-bit performance, $T_A$ = +25°C, unless otherwise noted.)

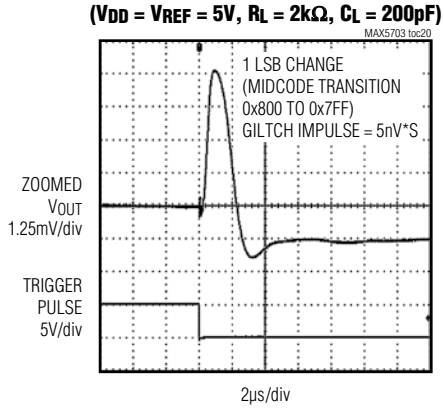
**SETTLING TO ±1 LSB**
**($V_{DD}$ = $V_{REF}$ = 5V, $R_L$ = 2kΩ, $C_L$ = 200pF)**



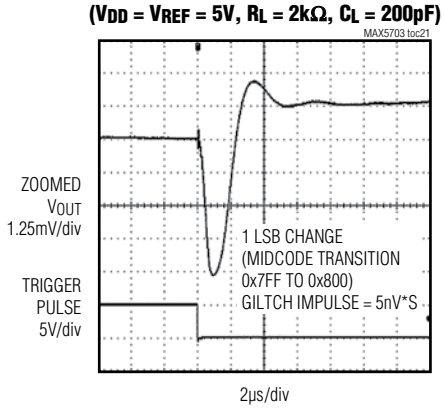

**SETTLING TO ±1 LSB**
**($V_{DD}$ = $V_{REF}$ = 5V, $R_L$ = 2kΩ, $C_L$ = 200pF)**



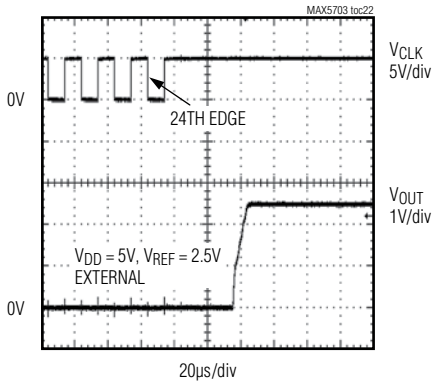

**MAJOR CODE TRANSITION GLITCH ENERGY**
**($V_{DD}$ = $V_{REF}$ = 5V, $R_L$ = 2kΩ, $C_L$ = 200pF)**



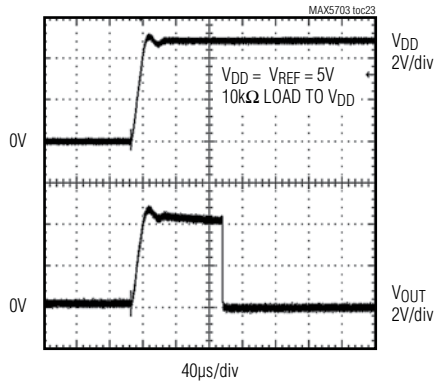

**MAJOR CODE TRANSITION GLITCH ENERGY**
**($V_{DD}$ = $V_{REF}$ = 5V, $R_L$ = 2kΩ, $C_L$ = 200pF)**




**$V_{OUT}$ vs. TIME TRANSIENT**
**EXITING POWER-DOWN**



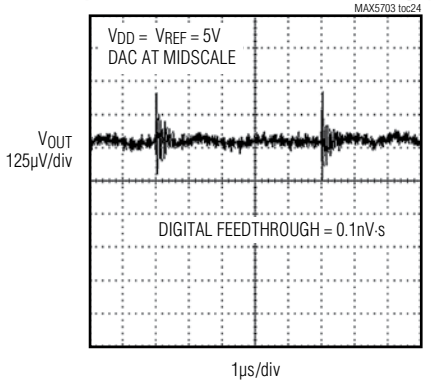

**POWER-ON RESET TO 0V**



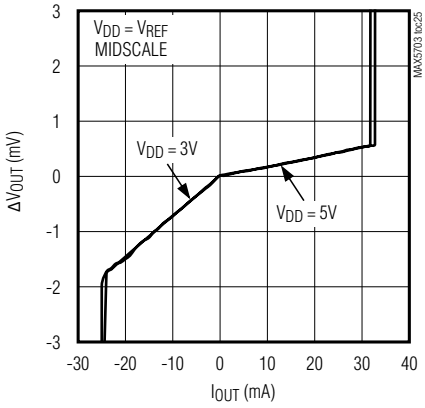
## *Typical Operating Characteristics (continued)*

(MAX5705, 12-bit performance, $T_A$ = +25°C, unless otherwise noted.)

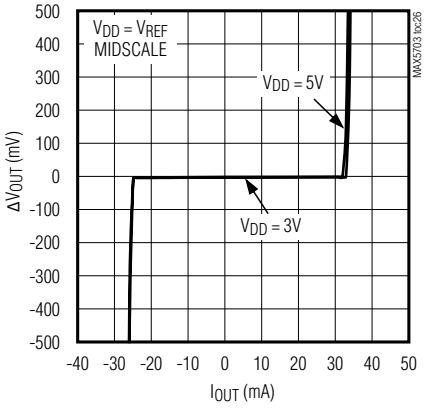
**DIGITAL FEEDTHROUGH**
**($V_{DD}$ = $V_{REF}$ = 5V, $R_L$ = 2kΩ, $C_L$ = 200pF)**



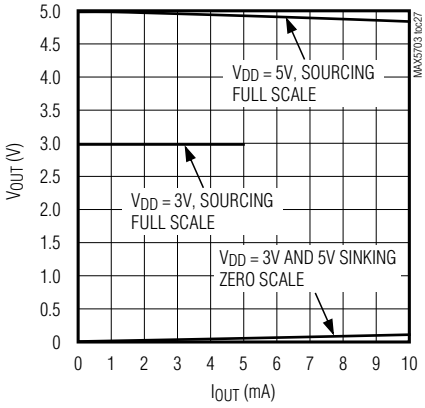

**OUTPUT LOAD REGULATION**



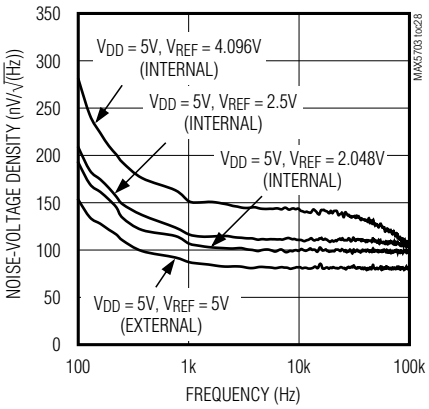

**OUTPUT CURRENT LIMITING**



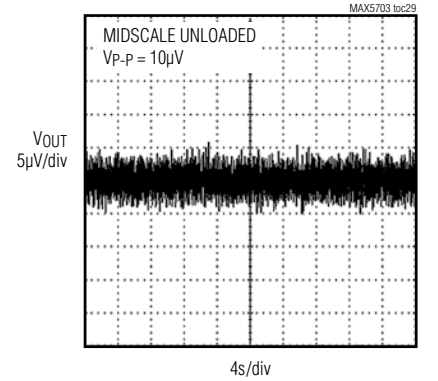

**HEADROOM AT RAILS**
**vs. OUTPUT CURRENT ($V_{DD}$ = $V_{REF}$)**



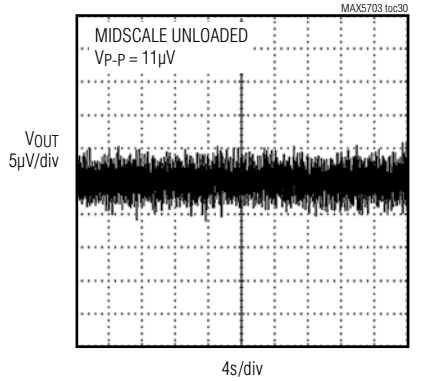

**NOISE-VOLTAGE DENSITY**
**vs. FREQUENCY (DAC AT MIDSCALE)**




**0.1Hz TO 10Hz OUTPUT NOISE, EXTERNAL REFERENCE ($V_{DD}$ = 5V, $V_{REF}$ = 4.5V)**



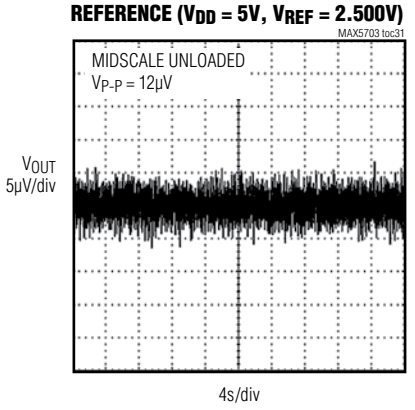

**0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD}$ = 5V, $V_{REF}$ = 2.048V)**



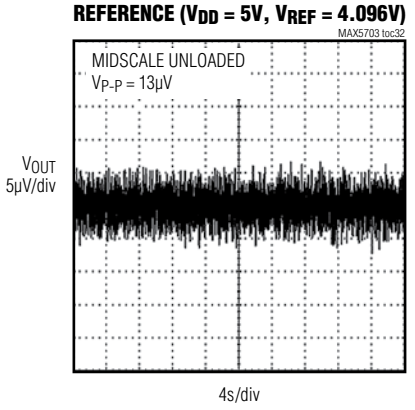
## *Typical Operating Characteristics (continued)*

(MAX5705, 12-bit performance, $T_A$ = +25°C, unless otherwise noted.)

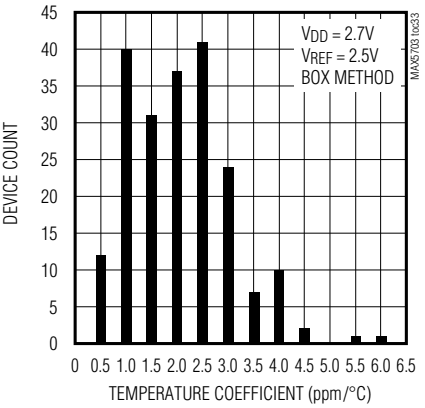
**0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD}$ = 5V, $V_{REF}$ = 2.500V)**



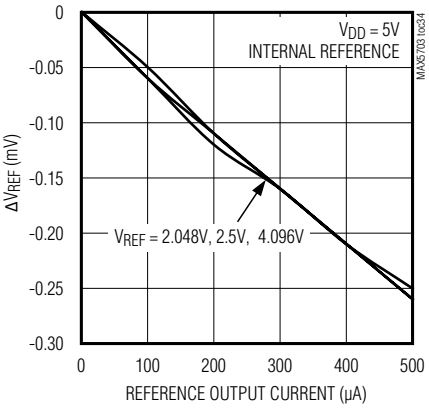

**0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD}$ = 5V, $V_{REF}$ = 4.096V)**



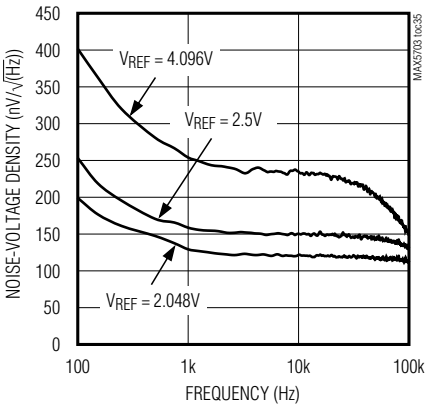

**$V_{REF}$ DRIFT vs. TEMPERATURE**



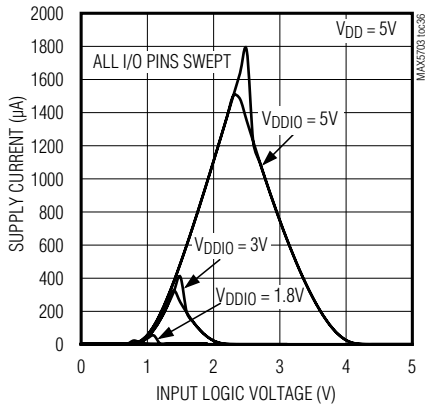

**REFERENCE LOAD REGULATION**



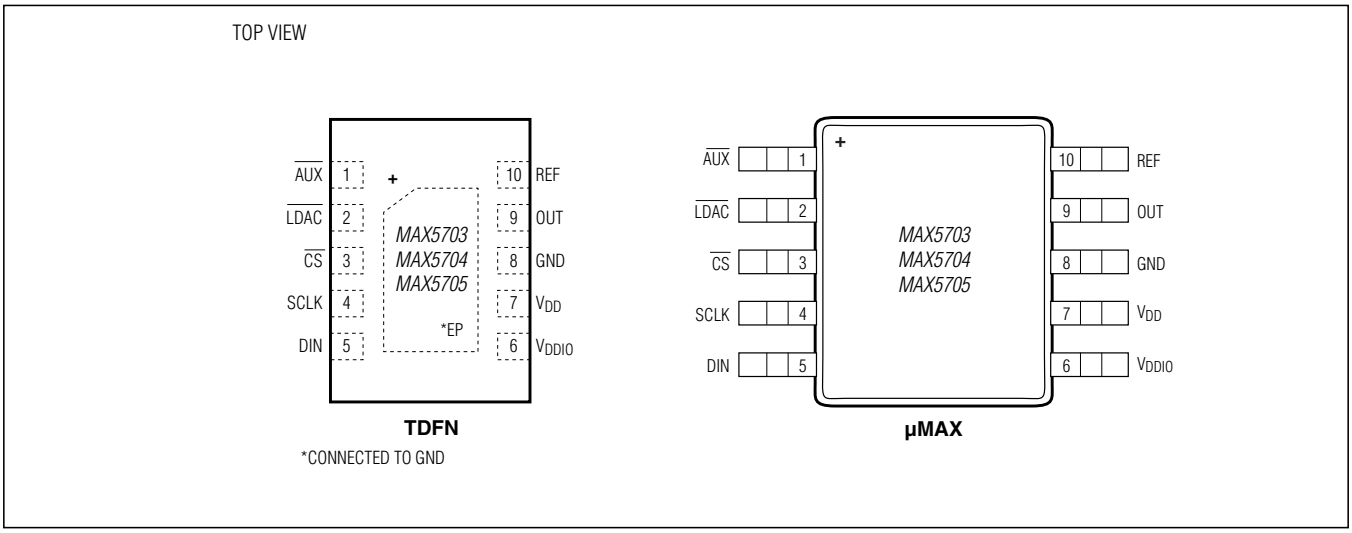

**INTERNAL REFERENCE NOISE DENSITY vs. FREQUENCY**




**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



## Pin Configurations




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $\overline{AUX}$ | Active-Low Auxilliary Asynchronous Input. User configurable, see Table 7. |
| 2 | $\overline{LDAC}$ | Dedicated Active-Low Asynchronous Load DAC |
| 3 | $\overline{CS}$ | SPI Chip-Select Input |
| 4 | SCLK | SPI Interface Clock Input |
| 5 | DIN | SPI Interface Data Input |
| 6 | $V_{DDIO}$ | Digital Interface Power-Supply Input |
| 7 | $V_{DD}$ | Supply Voltage Input. Bypass $V_{DD}$ with a 0.1µF capacitor to GND. |
| 8 | GND | Ground |
| 9 | OUT | Buffered DAC Output |
| 10 | REF | Reference Voltage Input/Output |
| — | EP | Exposed Pad (TDFN Only). Connect to ground. |

## Detailed Description

The MAX5703/MAX5704/MAX5705 are single-channel, low-power, 8-/10-/12-bit voltage-output digital-to-analog converters (DACs) with an internal output buffer. The wide supply voltage range of 2.7V to 5.5V and low power consumption accommodate low-power and low-voltage applications. The devices present a 100kΩ (typ) load to the external reference. The internal output buffer allows rail-to-rail operation. An internal voltage reference is available with software selectable options of 2.048V, 2.500V, or 4.096V. The devices feature a 50MHz, 3-wire SPI/QSPI/MICROWIRE/DSP-compatible serial interface to save board space and reduce complexity in isolated applications. The MAX5703/MAX5704/MAX5705 include a serial-in/parallel-out shift register, internal CODE and DAC registers, a power-on-reset (POR) circuit to initialize the DAC output to code zero, and control logic. A user-configurable $\overline{AUX}$ pin is available to asynchronously clear or gate the device output independent of the serial interface.

### DAC Output (OUT)

The MAX5703/MAX5704/MAX5705 include an internal buffer on the DAC output. The internal output buffer provides improved load regulation for the DAC output. The output buffer slews at 1V/µs (typ) and drives up to 2kΩ in parallel with 500pF. The analog supply voltage ($V_{DD}$) determines the maximum output voltage range of the devices as $V_{DD}$ powers the output buffer. Under no-load conditions, the output buffer drives from GND to $V_{DD}$, subject to offset and gain errors. With a 2kΩ load to GND, the output buffer drives from GND to within and 200mV of $V_{DD}$. With a 2kΩ load to $V_{DD}$, the output buffer drives from $V_{DD}$ to within 200mV of GND.

The DAC ideal output voltage is defined by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N}$$

Where D = code loaded into the DAC register, $V_{REF}$ = reference voltage, N = resolution.

### Internal Register Structure

The user interface is separated from the DAC logic to minimize digital feedthrough. Within the serial interface is an input shift register, the contents of which can be routed to control registers or the DAC itself, as determined by the user command.

Within the device there is a CODE register followed by a DAC Latch register (see the *Functional Diagram*). The contents of the CODE register hold pending DAC output settings which can later be loaded into the DAC registers. The CODE register can be updated using both CODE and CODE_LOAD user commands. The contents of the DAC register hold the current DAC output settings. The DAC register can be updated directly from the serial interface using the CODE_LOAD commands or can upload the current contents of the CODE register using LOAD commands or the $\overline{LDAC}$ input.

The contents of both CODE and DAC registers are maintained during all software power-down states, so that when the DAC is returned to a normal operating mode, it returns to its previously stored output settings. Any CODE or LOAD commands issued during software power-down states continue to update the register contents. The SW_CLEAR command clears the contents of the CODE and DAC registers to the user-programmable default values. The SW_RESET command resets all configuration registers to their power-on default states, while resetting the CODE and DAC registers to zero scale.

### Internal Reference

The MAX5703/MAX5704/MAX5705 include an internal precision voltage reference that is software selectable to be 2.048V, 2.500V, or 4.096V. When an internal reference is selected, that voltage is available on the REF pin for other external circuitry (see the *Typical Operating Circuits*) and can drive a 25kΩ load.

### External Reference

The external reference input features a typical input impedance of 100kΩ and accepts an input voltage from +1.24V to $V_{DD}$. Connect an external voltage supply between REF and GND to apply an external reference. The MAX5703/4/5 power up and reset to external reference mode. Visit **www.maximintegated.com/products/references** for a list of available external voltage-reference devices.

### $\overline{AUX}$ Input

The MAX5703/MAX5704/MAX5705 provide an asynchronous $\overline{AUX}$ (active-low) input. Use the CONFIG command to program the device to use the input in one of the following modes: $\overline{CLR}$ (default), $\overline{GATE}$, or disabled.

### $\overline{CLR}$ Mode

In $\overline{CLR}$ mode, the $\overline{AUX}$ input performs an asynchronous level sensitive CLEAR operation when pulled low. If $\overline{CLR}$ is configured and asserted, all CODE and DAC data registers are cleared to their default/return values as defined by the configuration settings. Other user-configuration settings are not affected.

Some SPI interface commands are gated by $\overline{CLR}$ activity during the transfer sequence. If $\overline{CLR}$ is issued during a command write sequence, any gated commands within the sequence are ignored. Any non-gated commands appearing in the transfer sequence are executed. For the gating condition to be removed, drive $\overline{CLR}$ high, satisfying the $t_{CSC}$ requirements.

### $\overline{GATE}$ Mode

Use of the $\overline{GATE}$ mode provides a means of momentarily holding the DAC in a user-selectable default/return state, returning the DAC to the last programmed state upon removal. The MAX5703/MAX5704/MAX5705 also feature a software-accessible GATE command. While asserted in $\overline{GATE}$ mode, the $\overline{AUX}$ pin does not interfere with RETURN, CODE, or DAC register updates and related load activity.

### $\overline{LDAC}$ Input

The MAX5703/MAX5704/MAX5705 provide a dedicated asynchronous $\overline{LDAC}$ (active-low) input. The $\overline{LDAC}$ input performs an asynchronous level sensitive LOAD operation when pulled low. Use of the $\overline{LDAC}$ input mode provides a means of updating multiple devices together as a group. Users wishing to control the DAC update instance independently of the I/O instruction should hold $\overline{LDAC}$ high during programming cycles. Once programming is complete, $\overline{LDAC}$ may be strobed and the new CODE register content is loaded into the DAC latch output. Users wishing to load new DAC data in direct response to I/O CODE register activity should connect $\overline{LDAC}$ permanently low; in this configuration, the MAX5703/MAX5704/MAX5705 DAC output updates in response to each completed I/O CODE instruction update edge. A software LOAD command is also provided.

The $\overline{LDAC}$ operation does not interact with the user interface directly. However, in order to achieve the best possible glitch performance, timing with respect to the interface update edge should follow $t_{LDH}$ specifications when issuing CODE commands.

### $V_{DDIO}$ Input

The MAX5703/MAX5704/MAX5705 feature a separate supply pin ($V_{DDIO}$) for the digital interface (1.8V to 5.5V). Connect $V_{DDIO}$ to the I/O supply of the host processor.

### SPI Serial Interface

The MAX5703/MAX5704/MAX5705 3-wire serial interface is compatible with MICROWIRE/SPI/QSPI and DSPs. The interface provides three inputs: SCLK, $\overline{CS}$, and DIN. The chip-select input ($\overline{CS}$, active-low) frames the data loaded through the serial data input (DIN). Following a $\overline{CS}$ input high-to-low transition, the data is shifted in synchronously and latched into the input register on each falling edge of the serial clock input (SCLK). Each serial operation word is 24-bits long. The DAC data is left justified as shown in Table 1. The serial input register transfers its contents to the destination registers after loading 24 bits of data on the 24th SCLK falling edge. To initiate a new SPI operation, drive $\overline{CS}$ high and then low to begin the next operation sequence, being sure to meet all relevant timing requirements. During $\overline{CS}$ high periods, SCLK is ignored, allowing communication to other devices on the same bus. SPI operations consisting of more than 24 SCLK cycles are executed on the 24th SCLK falling edge, using the first three bytes of data available. SPI operations consisting of less than 24 SCLK cycles will not be executed. The content of the SPI operation consists of a command byte followed by a two byte data word.

Figure 1 shows the timing diagram for the complete 3-wire serial interface transmission. The DAC code settings (D) for the MAX5703/MAX5704/MAX5705 are accepted in an offset binary format (see Table 1). Otherwise, the expected data format for each command is listed in Table 2.

### SPI User-Command Register Map

This section lists the user-accessible commands and registers for the MAX5703/MAX5704/MAX5705.

Table 2 provides detailed information about the SPI Command Registers.

### CODE Command

The CODE command (B[23:20] = 1000) updates the CODE register content for the DAC. Changes to the CODE register content based on this command will not affect the DAC output directly unless the $\overline{LDAC}$ input is in a low state. Otherwise, a subsequent hardware or software LOAD operation will be required to move this content to the active DAC latch. This command is gated when $\overline{CLR}$ is asserted, updates to this register are ignored while the register is being cleared. See Table 1 and Table 2.

### LOAD Command

The LOAD command (B[23:20] = 1001) updates the DAC latch register content by uploading the current contents of the CODE register. This command is gated when $\overline{CLR}$ is asserted, updates to this register are ignored while the register is being cleared. See Table 2.

### CODE_LOAD Command

The CODE_LOAD command (B[23:20] = 1010 and 1011) updates the CODE register contents as well as the DAC register content of the DAC. This command is gated when $\overline{CLR}$ is asserted, updates to these registers are ignored while the register is being cleared. See Table 1 and Table 2.

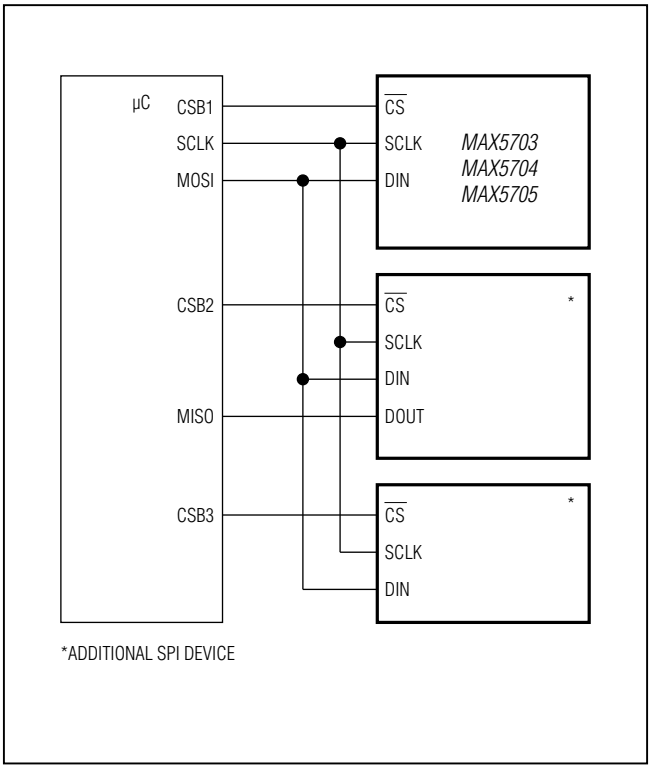



*Figure 2. Typical SPI Application Circuit*

## Table 1. DAC Data Bit Positions

| PART | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MAX5703 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | X | X | X | X | X | X |
| MAX5704 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | X | X | X | X |
| MAX5705 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | X | X |

## Table 2. SPI Commands Summary

| COMMAND | B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DAC COMMANDS** | | | | | | | | | | | | | | | | | | | | | | | | | |
| CODE | 1 | 0 | 0 | 0 | X | X | X | X | CODE REGISTER DATA[11:4] | | | | | | | | CODE REGISTER DATA[3:0] | | | | X | X | X | X | Writes data to the CODE register |
| LOAD | 1 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | Transfers data from the CODE registers to the DAC register |
| CODE_LOAD | 1 | 0 | 1 | 0 | X | X | X | X | CODE AND DAC REGISTER DATA[11:4] | | | | | | | | CODE AND DAC REGISTER DATA[3:0] | | | | X | X | X | X | Simultaneously writes data to the CODE register while updating DAC register |
| CODE_LOAD | 1 | 0 | 1 | 1 | X | X | X | X | CODE AND DAC REGISTER DATA[11:4] | | | | | | | | CODE AND DAC REGISTER DATA[3:0] | | | | X | X | X | X | Simultaneously writes data to the CODE register while updating DAC register |
| RETURN | 0 | 1 | 1 | 1 | X | X | X | X | RETURN REGISTER DATA[11:4] | | | | | | | | RETURN REGISTER DATA[3:0] | | | | X | X | X | X | Updates the RETURN register contents for the DAC |

## Table 2. SPI Commands Summary (continued)

| COMMAND | B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CONFIGURATION COMMANDS** | | | | | | | | | | | | | | | | | | | | | | | | | |
| REF | 0 | 0 | 1 | 0 | 0 = No Drive<br>1 = Drive Pin | 0 = Default<br>1 = Always ON | Ref Mode<br>00 = EXT<br>01 = 2.5V<br>10 = 2.0V<br>11 = 4.1V | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | Sets the reference operating mode. |
| SOFTWARE | 0 | 0 | 1 | 1 | X | Type:<br>000 = END<br>001 = GATE<br>100 = CLR<br>101 = RST<br>Other = No Effect | | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | Executes a software operation of the type chosen |
| POWER | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | **Power Mode:**<br>00 = DAC<br>01 = 1kΩ<br>10 = 100kΩ<br>11 = HiZ | | X | X | X | X | X | X | Sets the Power mode |
| CONFIG | 0 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | $\overline{AUX}$ Mode:<br>011 = GATE<br>110 = CLEAR<br>111 = NONE<br>Other = No Effect | | | X | X | X | Updates the function of the $\overline{AUX}$ input |
| DEFAULT | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | **Default Values:**<br>000 = POR<br>001 = ZERO<br>010 = MID<br>011 = FULL<br>100 = RETURN<br>Other = No Effect | | | X | X | X | X | X | Sets the default value for the DAC |
| **NO OPERATION COMMANDS** | | | | | | | | | | | | | | | | | | | | | | | | | |
| No Operation | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | These commands will have no effect on the part. |
| | 1 | 1 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | |
| **Reserved Commands:** Any commands not specifically listed above are reserved for Maxim internal use only. | | | | | | | | | | | | | | | | | | | | | | | | | |

### REF Command

The REF (B[23:20] = 0010) command updates the global reference setting used for the DAC. Set B[17:16] = 00 to use an external reference for the DAC or set B[17:16] to 01, 10, or 11 to select either the 2.5V, 2.048V, or 4.096V internal reference, respectively.

If RF3 (B19) is set to zero (default) in the REF command, the REF I/O will not be driven by the internal reference circuit, saving current. If RF3 is set to one, the REF I/O will be driven by the internal reference circuit, consuming an additional 25µA (typ) of current when the reference is powered; when the reference is powered down, the REF I/O will be high-impedance.

If RF2 (B18) is set to zero (default) in the REF command, the reference will be powered down any time the DAC is powered down (in STANDBY mode). If RF2 (B18) is set to one, the reference will remain powered even if the DAC is powered down, allowing continued operation of external circuitry. In this mode, the 1µA shutdown state is not available. See Table 3.

### SOFTWARE Commands

The SOFTWARE (B[23:20] = 0011) commands provide a means of issuing several flexible software actions. See Table 4.

The SOFTWARE Command Action Mode is selected by B[18:16]:

END (000): Used to end any active gate operation, returning to normal operation (default).

GATE (001): DAC contents will be gated to their DEFAULT selected values until the gate condition is removed.

CLEAR (100): All CODE and DAC contents will be cleared to their DEFAULT selected values.

RESET (101): All CODE, DAC, RETURN, and configuration registers reset to their power-up defaults (including REF, POWER, and CONFIG settings), simulating a power cycle reset.

OTHER: No effect.

## Table 3. REF (0010) Command Format

| B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | RF3 | RF2 | RF1 | RF0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| REF COMMAND | | | | 0 = REF Not driven<br>1 = REF Driven | 0 = Off in Standby<br>1 = On in Standby | Ref Mode:<br>00 = EXT<br>01 = 2.5V<br>10 = 2.0V<br>11 = 4.0V | | Don't Care | | | | | | | | Don't Care | | | | | | | |
| DEFAULT VALUES | | | | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| COMMAND BYTE | | | | | | | | DATA HIGH BYTE | | | | | | | | DATA LOW BYTE | | | | | | | |

## Table 4. SOFTWARE (0011) Command Format

| B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | X | SW2 | SW1 | SW0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| SOFTWARE COMMANDS | | | | Don't Care | Mode:<br>000: END<br>001: GATE<br>100: CLR<br>101: RST<br>Other: No Effect | | | Don't Care | | | | | | | | Don't Care | | | | | | | |
| DEFAULT VALUES | | | | X | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| COMMAND BYTE | | | | | | | | DATA HIGH BYTE | | | | | | | | DATA LOW BYTE | | | | | | | |

### *POWER Command*

The MAX5703/MAX5704/MAX5705 feature a software-controlled POWER mode command (B[23:20] = 0100).

In power-down, the DAC output is disconnected from the buffer and is grounded with either one of the two selectable internal resistors or set to high impedance. See Table 5 and Table 6 for the selectable internal resistor values in power-down mode. In power-down mode, the DAC register retains its value so that the output is restored when the device powers up. The serial interface remains active in power-down mode with all registers accessible.

In power-down mode, the internal reference can be powered down or it can be set to remain powered-on for external use. Also, in power-down mode, parts using the external reference do not load the REF pin. See Table 5.

## Table 5. POWER (0100) Command Format

| B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | PD1 | PD0 | X | X | X | X | X | X |
| POWER COMMAND | | | | Don't Care | | | | Don't Care | | | | | | | | Power Mode: 00 = Normal 01 = 1kΩ 10 = 100kΩ 11 = Hi-Z | | Don't Care | | | | | |
| DEFAULT VALUES | | | | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | X | X | X | X | X | X |
| COMMAND BYTE | | | | | | | | DATA HIGH BYTE | | | | | | | | DATA LOW BYTE | | | | | | | |

## Table 6. Selectable DAC Output Impedance in Power-Down Mode

| PD1 (B7) | PD0 (B6) | OPERATING MODE |
|---|---|---|
| 0 | 0 | Normal operation |
| 0 | 1 | Power-down with internal 1kΩ pulldown resistor to GND. |
| 1 | 0 | Power-down with internal 100kΩ pulldown resistor to GND. |
| 1 | 1 | Power-down with high-impedance output. |

### CONFIG Command

The CONFIG command (B[23:20] = 0101) updates the function of the $\overline{AUX}$ input enabling its gate, load, or clear (default) operation mode. See Table 7.

$\overline{AUX}$ Config settings are written by B[5:3]:

GATE (011): $\overline{AUX}$ functions as a $\overline{GATE}$. DAC code is gated to DEFAULT value input when pin is low.

CLEAR (110): $\overline{AUX}$ functions as a $\overline{CLR}$ input (default). CODE and DAC content is cleared to DEFAULT value if pin is low.

NONE (111): $\overline{AUX}$ functions are disabled.

OTHER: $\overline{AUX}$ function is not altered.

### DEFAULT Command

DEFAULT (0110): The DEFAULT command selects the default value for the DAC. These default values are used for all future clear and gate operations. The new default setting is determined by bits DF[2:0]. See Table 8.

Available default values are:

POR (000): DAC defaults to power-on reset value (default).

ZERO (001): DAC defaults to zero scale.

MID (010): DAC defaults to midscale.

FULL (011): DAC defaults to full scale.

RETURN (100): DAC defaults to value specified by the RETURN register

OTHER: No effect, the default setting remains unchanged.

**Note:** The selected default values do not apply to resets initiated by SW_RESET commands or supply cycling, both of which return the DACs to the power-on reset state (zero scale).

## Table 7. CONFIG (0101) Command Format

| B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | AB2 | AB1 | AB0 | X | X | X |
| CONFIG COMMAND | | | | Don't Care | | | | Don't Care | | | | | | | | Don't Care | | AUXB Mode: 011 = GATE 110 = CLEAR 111 = NONE Other = No Effect | | | Don't Care | | |
| DEFAULT VALUES | | | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | 1 | 0 | X | X | X |
| COMMAND BYTE | | | | | | | | DATA HIGH BYTE | | | | | | | | DATA LOW BYTE | | | | | | | |

## Table 8. DEFAULT (0110) Command Format

| B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | DF2 | DF1 | DF0 | X | X | X | X | X |
| DEFAULT COMMAND | | | | Don't Care | | | | Don't Care | | | | | | | | Default Values: 000: POR 001: ZERO 010: MID 011: FULL 100: RETURN Other: No Effect | | | Don't Care | | | | |
| DEFAULT VALUES | | | | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | X | X | X | X | X |
| COMMAND BYTE | | | | | | | | DATA HIGH BYTE | | | | | | | | DATA LOW BYTE | | | | | | | |

### RETURN Command

The RETURN command (B[23:20] = 0111) updates the RETURN register content for the DAC. If the DEFAULT configuration register is set to RETURN mode, the DAC will be cleared or gated to the RETURN register value in the event of a SW or HW CLEAR or GATE condition. It is not necessary to program this register if the DEFAULT = RETURN mode will not be used. The data format for the RETURN register is identical to that used for CODE and LOAD operations. See Table 1 and Table 2.

## Applications Information

### Power-On Reset (POR)

When power is applied to $V_{DD}$, the DAC output is set to zero scale. To optimize DAC linearity, wait until the supplies have settled and the internal setup and calibration sequence completes (200µs, typ).

### Power Supplies and Bypassing Considerations

Bypass $V_{DD}$ with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect GND to the analog ground plane.

### Layout Considerations

Digital and AC transient signals on GND can create noise at the output. Connect GND to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5703/MAX5704/MAX5705 GND. Carefully layout the traces between channels to reduce AC cross-coupling. Do not use wire-wrapped boards and sockets. Use shielding to maximize noise immunity. Do not run analog and digital signals parallel to one another, especially clock signals. Avoid routing digital lines underneath the MAX5703/MAX5704/MAX5705 package.

## Definitions

### Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a straight line drawn between two codes once offset and gain errors have been nullified.

### Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL ≤ 1 LSB, the DAC guarantees no missing codes and is monotonic. If the magnitude of the DNL ≥ 1 LSB, the DAC output may still be monotonic.

### Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function. The offset error is calculated from two measurements near zero code and near maximum code.

### Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

### Zero-Scale Error

Zero-scale error is the difference between the DAC output voltage when set to code zero and ground. This includes offset and other die level nonidealities.

### Full-Scale Error

Full-scale error is the difference between the DAC output voltage when set to full scale and the reference voltage. This includes offset, gain error, and other die level nonidealities.

### Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

### Digital Feedthrough

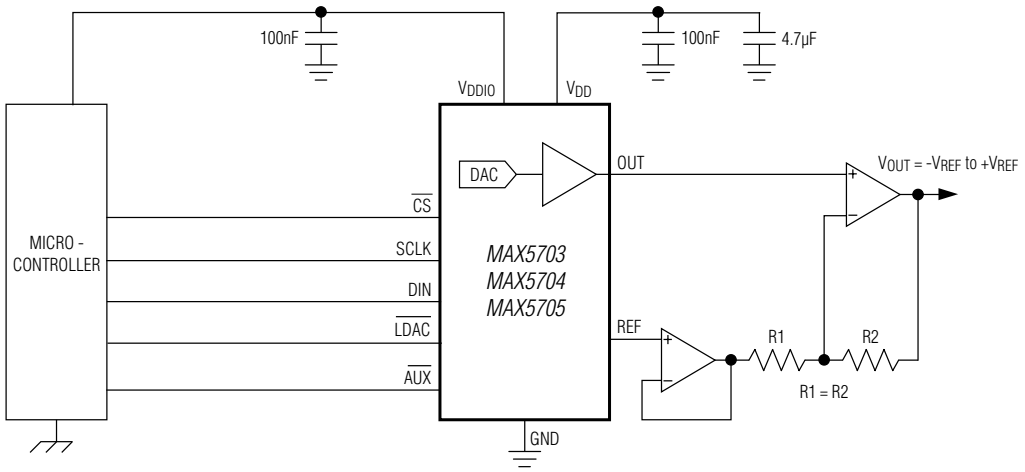
Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

### Digital-to-Analog Glitch Impulse

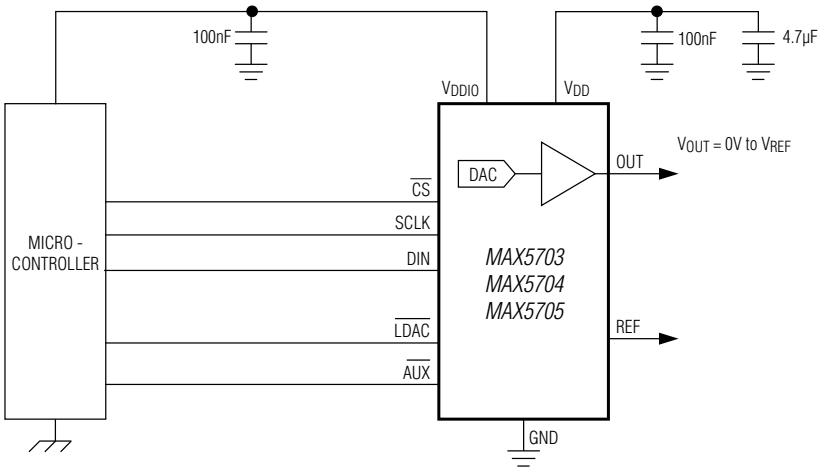
A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

## Typical Operating Circuits




**NOTE:** BIPOLAR OPERATION SHOWN




**NOTE:** UNIPOLAR OPERATION SHOWN

## Ordering Information

| PART | PIN-PACKAGE | RESOLUTION (BIT) | INTERNAL REFERENCE TEMPCO (ppm/°C) |
|---|---|---|---|
| **MAX5703**ATB+T | 10 TDFN-EP* | 8 | 10 (typ), 25 (max) |
| MAX5703AUB+ | 10 µMAX | 8 | 10 (typ), 25 (max) |
| **MAX5704**ATB+T | 10 TDFN-EP* | 10 | 10 (typ), 25 (max) |
| MAX5704AUB+ | 10 µMAX | 10 | 10 (typ), 25 (max) |
| **MAX5705**AAUB+ | 10 µMAX | 12 | 4 (typ), 12 (max) |
| MAX5705BATB+T | 10 TDFN-EP* | 12 | 10 (typ), 25 (max) |
| MAX5705BAUB+ | 10 µMAX | 12 | 10 (typ), 25 (max) |

***Note:*** *All devices are specified over the -40°C to +125°C temperature range.*
*+Denotes a lead(Pb)-free/RoHS-compliant package.*
*T = Tape and reel.*
**EP = Exposed pad.*

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 10 TDFN-EP | T1032N+1 | 21-0429 | 90-0082 |
| 10 µMAX | U10+2 | 21-0061 | 90-0330 |

# Ultra-Small, Single-Channel, 8-/10-/12-Bit Buffered Output Voltage DACs with Internal Reference and SPI Interface

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 11/12 | Initial release | — |
| 1 | 2/13 | Released MAX5703/MAX5704. Updated the *Electrical Characteristics*. | 2–8, 25 |
| 2 | 6/13 | Released the MAX5703/MAX5704/MAX5705 TDFN packages. | 25 |