FUJITSU MICROELECTRONICS
DATA SHEET

DS04-29130-1Ea

ASSP

Multi-output Spread Spectrum Clock Generator

MB88181

■ DESCRIPTION

The MB88181 is a multi-output, EMI resistant clock generator that is suitable for applications such as LCD, PDPs, MFPs, and mobile phones. This chip has 8 output pins, of which a maximum of 3 pins can be used to output a spread-spectrum clock.

■ FEATURES

- Built-in PLL : 4
  Without spread-spectrum function : 3 (PLL1, PLL2, PLL3)
  With spread-spectrum function : 1 (SSCG)
- Output setting pins : 2 pins (Able to select from 4 different combinations of output frequency and modulation index) *
- Clock output pins : 8 pins (Spread spectrum clock output : 3 pins (Max)) *
- Input frequency : 16 MHz to 32 MHz
- Output frequency : 8 MHz to 166 MHz (4 different combinations of output frequencies are selectable) *
- Modulation index setting : selectable from no modulation, ± 0.5%, ± 1.0%, ± 1.5% or ± 2.0%*
- Equipped with power down function
- Clock output duty cycle : 45% to 55%

* : Set various settings by mask option.

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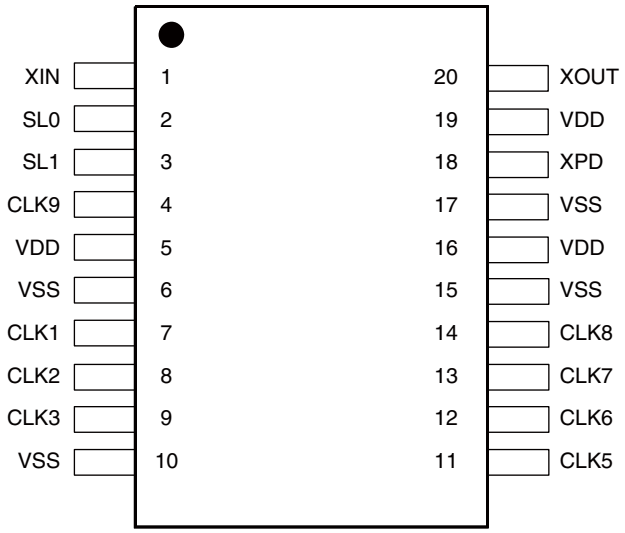
- Clock cycle-cycle jitter : Less than100 ps
- Low current consumption by CMOS process :
  At normal operation : 55 mA (power supply voltage : 3.3 V, normal temperature, no load)
  At power down : 5 μA (power supply voltage : 3.6 V, normal temperature, no load)
- Power supply voltage : 3.0 V to 3.6 V
- Operating temperature : − 40 °C to + 85 °C
- Package : TSSOP 20-pin

■ PIN ASSIGNMENT

TOP VIEW

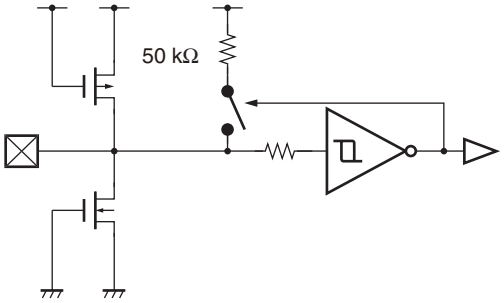
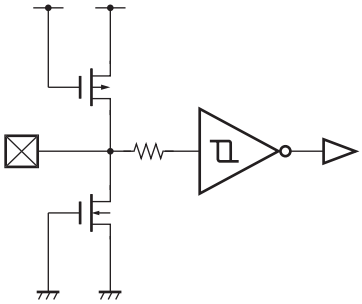
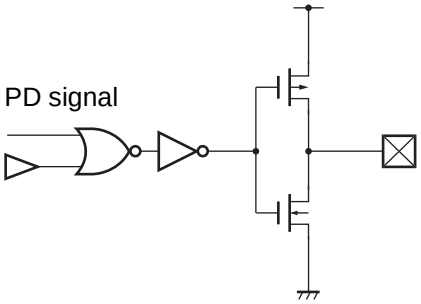
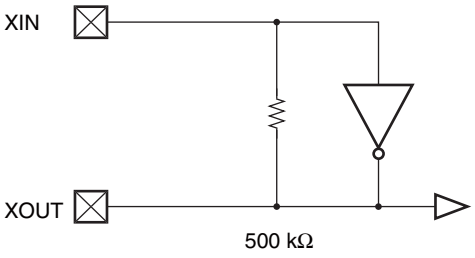


(FPT-20P-M06)

■ PIN DESCRIPTION

Pin no.	I/O	Pin no.	Description
XIN	I	1	Crystal oscillator connection pin/input pin
SL0	I	2	Frequency/modulation index setting pin 0
SL1	I	3	Frequency/modulation index setting pin 1
CLK9	O	4	Clock output pin 9
VDD	—	5	Power supply pin
VSS	—	6	GND pin
CLK1	O	7	Clock output pin 1
CLK2	O	8	Clock output pin 2
CLK3	O	9	Clock output pin 3
VSS	—	10	GND pin
CLK5	O	11	Clock output pin 5
CLK6	O	12	Clock output pin 6
CLK7	O	13	Clock output pin 7
CLK8	O	14	Clock output pin 8
VSS	—	15	GND pin
VDD	—	16	Power supply pin
VSS	—	17	GND pin
XPD	I	18	Power down pin (power down when set to “L”)
VDD	—	19	Power supply pin
XOUT	O	20	Crystal oscillator connection pin/input pin

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
XPD		• With pull-up resistance The pull-up resistance is disconnected when the XPD line is “L”. • CMOS hysteresis input
SL0, SL1		CMOS hysteresis input
CLK1 to CLK3 CLK5 to CLK9		• CMOS output • At PD active high, “L” output or Hi-Z output (selectable).
XIN, XOUT		• Oscillator circuit • Built-in feedback resistors 500 kΩ

■ HANDLING DEVICES

(1) Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than power supply voltage or a voltage lower than GND is applied to an input or output pin or (b) a voltage higher than the rating is applied between power supply and GND pins. The latch-up may cause components to burn out because the power supply current increases significantly. Make sure that the maximum ratings are not exceeded while the device is being used.

(2) Handling unused pins

Leaving unused input pins unconnected may cause a malfunction. Handle unused pins by connecting to a pull-up or pull-down resistor.

(3) Power supply pins

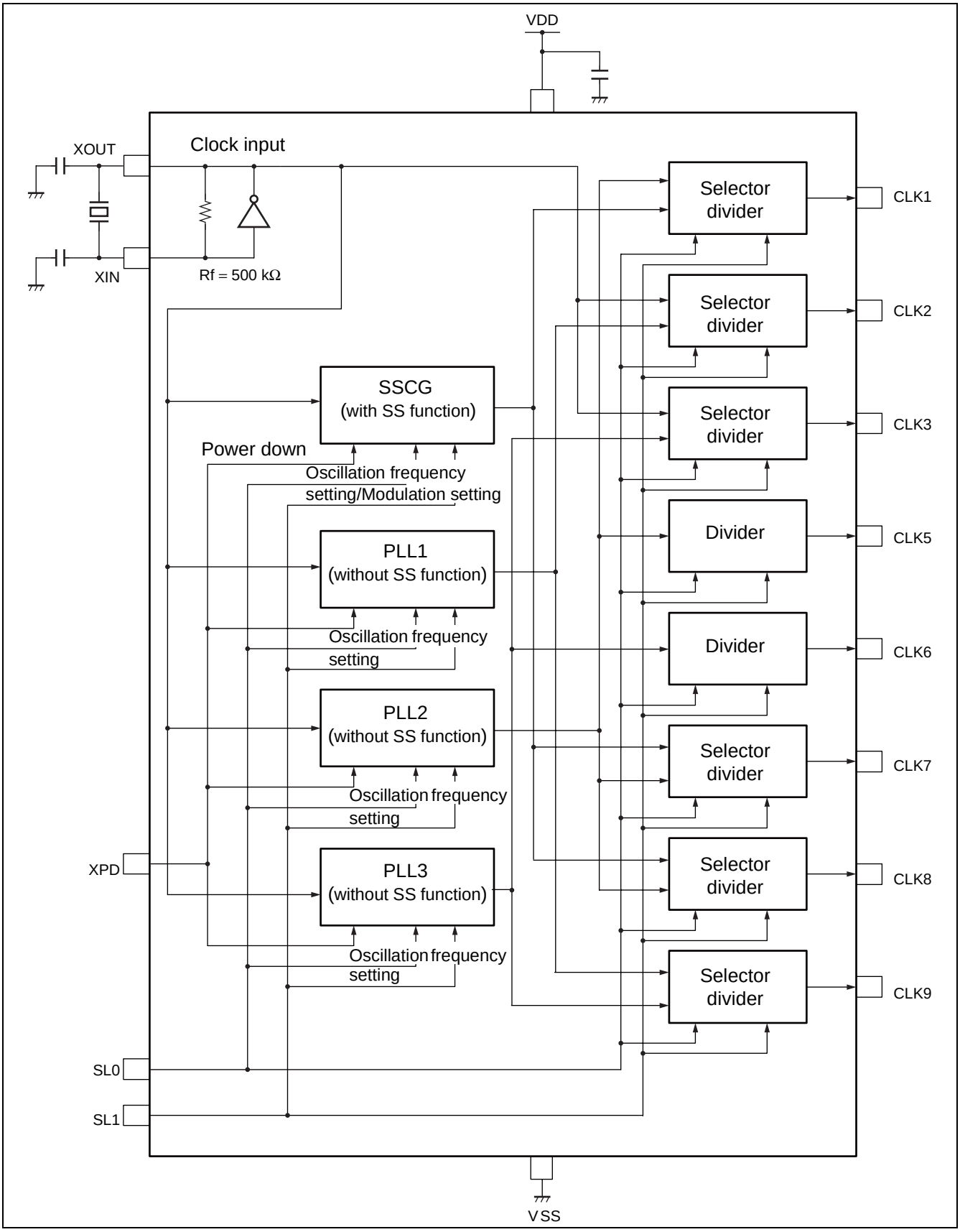
Ensure that the impedance of the connection from the power supply source to the power supply pins on the device is as low as possible.

It is recommended that a ceramic capacitor of approx. 0.01 μF and an electrolytic capacitor of approx. 10 μF are connected in parallel between the power supply pins and ground pins as near to the device as possible to act as bypass capacitors.

(4) Crystal oscillator circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design the printed circuit so that the wiring between the crystal oscillator and the XIN and XOUT pins does not cross over any other wiring as much as possible. It is strongly recommended that the circuit board artwork is designed such that the XIN and XOUT pins are surrounded by ground plane for more stable operation.

■ BLOCK DIAGRAM



■ OSCILLATION FREQUENCY

The frequencies of the PLL1, PLL2, PLL3, and SSCG can be determined by the following formula.

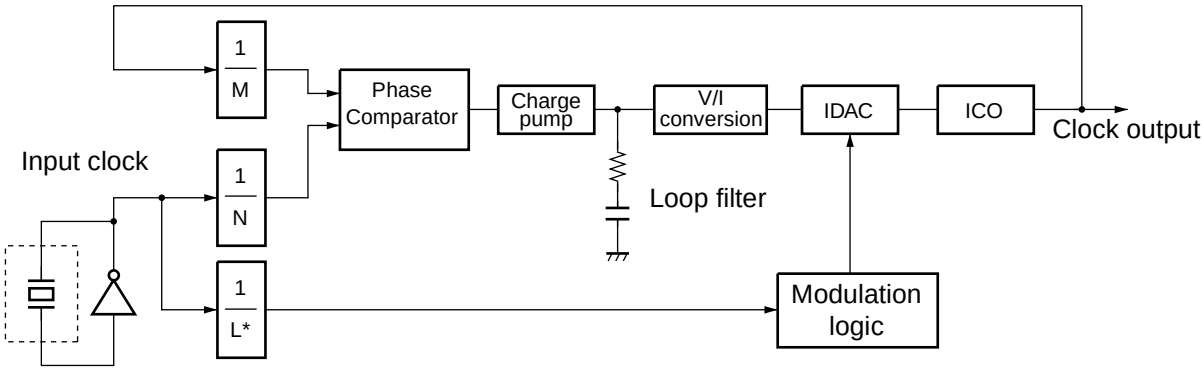
$$\text{Oscillation frequency} = \frac{M}{N} \times \text{(reference clock (input clock) frequency)}$$

[M is an integer between 8 and 512, N is an integer between 7 and 32]

Note : From among the range of frequencies that can be selected by the above formula, the range of frequencies that can actually be generated is from 128 MHz to 400 MHz.

M and N can be configured separately for each of the PLL1, PLL2, PLL3, and SSCG. Furthermore, these can be configured separately for each of the SL0, SL1 pin settings.

• MB88181 PLL unit block diagram



* : L is the modulation period setting

■ MODULATION INDEX AND MODULATION PERIOD

The SSCG is able to output the clock which is applied spectrum modulation. The modulation index is selectable from OFF, ± 0.5%, ± 1.0%, ± 1.5%, and ± 2.0%, and can be changed independently for each of the SL0 and SL1 pin settings.

The period of modulation can be determined from the following equation.

$$\frac{\text{Reference clock frequency}}{300 \times L} \quad (L = 2, 3)$$

Note : The value of L is fixed by mask option.
It can not be changed according to the SL0 or SL1 pin setting.

■ OUTPUT FREQUENCY

The output pins can output the reference clock, or the clocks SSCG, PLL1, PLL2, or PLL3 frequency divided by 2 to 16 (they can not output by dividing the reference clock). Pins which do not need the clock output can be configured as fixed “L” outputs or as Hi-Z. The frequency division ratio can be configured by mask option and by setting SL0 and SL1 pins.

The clock sources that can be selected for each of the clock outputs are as shown in the following table.

	PLL1	PLL2	PLL3	SSCG	Reference clock	Output stop “L” or Hi-Z
CLK1	—	○	—	○	—	○
CLK2	○	—	—	—	○	○
CLK3	—	—	○	—	○	○
CLK5	—	○	—	—	—	○
CLK6	—	—	○	—	—	○
CLK7	—	○	—	○	—	○
CLK8	—	○	—	○	—	○
CLK9	○	—	○	—	—	○

○ : Enable, — : Disable

Note : Set by mask option.

■ POWER DOWN

XPD = “H” : Normal operating mode

XPD = “L” : Power-down mode. Clock outputs (CLK pins) are set to “L” or Hi-Z.

Note : If the XPD pin is set to “L”, all of the PLL oscillator circuits are stopped and are placed in the power-down state, and the device enters a low-power consumption mode. In the power-down state, the clock output pins CLK1 to CLK3 and CLK5 to CLK9 output “L” or are placed in the Hi-Z state.
The output pin state during power-down is fixed by mask option.
The SL0, SL1 pin settings do not enable to switch the fixed states between “L” and “Hi-Z”.

■ ABSOLUTE MAXIMUM RATINGS

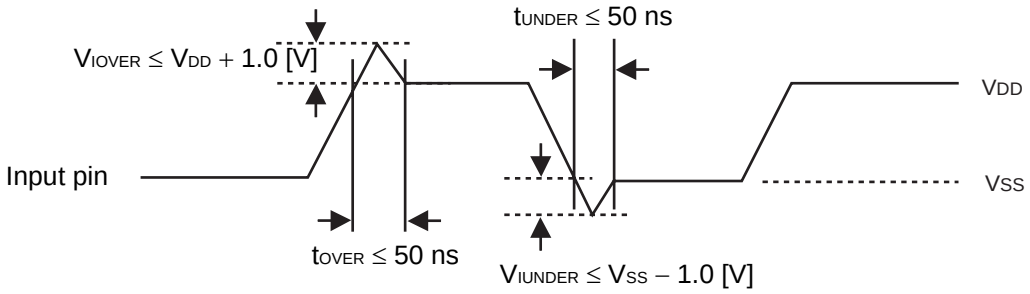
Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*1	V_{DD}	− 0.5	+ 4.0	V
Input voltage*1	V_I	V_{SS} − 0.5	V_{DD} + 0.5	V
Output voltage*1	V_O	V_{SS} − 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	− 55	+ 125	°C
Operation junction temperature	T_J	− 40	+ 125	°C
Output current	I_O*2	− 14	+ 14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} − 1.0 (t_{UNDER} ≤ 50 ns)	—	V

*1 : The parameter is based on V_{SS} = 0.0 V.

*2 : The current per pin.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

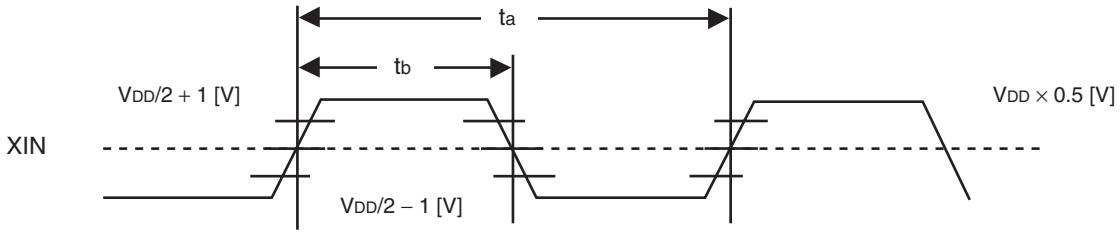
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	VDD	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	XIN, SL0, SL1, XPD	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}	XIN, SL0, SL1, XPD	—	V_{SS}	—	$V_{DD} \times 0.2$	V
Input clock duty cycle	t_{DCI}	XIN	16 MHz to 32 MHz	40	50	60	%
Operating temperature	Ta	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

(Ta = –40 °C to + 85 °C, V_{DD} = 3.0 V to 3.6 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	VDD	Original oscillation : 20 MHz SSCG : 200 MHz oscillation PLL1 : 240 MHz oscillation PLL2 : 160 MHz oscillation PLL3 : 360 MHz oscillation CLK1 : 20 MHz output CLK2 : REF output CLK3 : “L” output CLK5 : 32 MHz output CLK6 : 36 MHz output CLK7 : 50 MHz output CLK8 : 40 MHz output CLK9 : 80 MHz output (No load capacitance at output)	—	55	60	mA
Power down current	I_{PD}	VDD	XPD = 0	—	5	80	μA
Output voltage	V_{OH}	CLK1 to CLK3 CLK5 to CLK9	“H” level output, I_{OH} = – 8 mA	0.8 × V_{DD}	—	V_{DD}	V
	V_{OL}	CLK1 to CLK3 CLK5 to CLK9	“L” level output, I_{OL} = 8 mA	V_{SS}	—	0.2 × V_{DD}	V
Output impedance	Z_{OC}	CLK1 to CLK3 CLK5 to CLK9	8 MHz to 80 MHz	—	30	—	Ω
			80 MHz to 166 MHz	—	20	—	
Load capacitance	C_L	CLK1 to CLK3 CLK5 to CLK9	8 MHz to 166 MHz	—	—	15	pF
Input pull-up resistance	R_{XPD}	XPD	V_{IH} = 0.8 × V_{DD}*	25	—	200	kΩ

* : The XPD pin input pull-up resistance is disconnected when the XPD pin is set to “L”.

• AC Characteristics

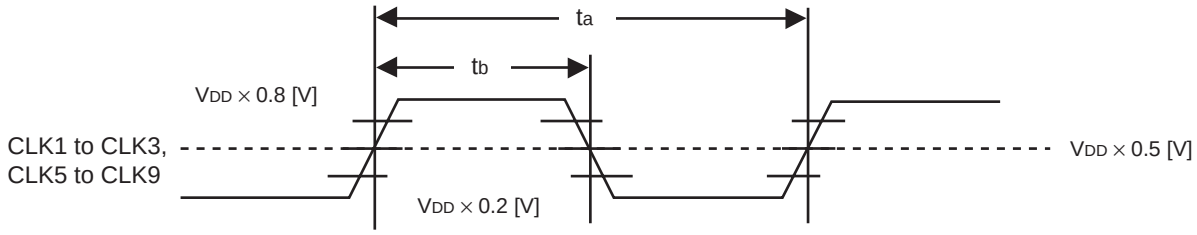
(Ta = –40 °C to + 85 °C, V_{DD} = 3.0 V to 3.6 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f_{in}	XIN	Crystal oscillator input	16	—	32	MHz
Crystal oscillator frequency	f_x	XIN, XOUT	Fundamental frequency	16	—	32	MHz
Output frequency	f_{OUT}	CLK1 to CLK3 CLK5 to CLK9	—	8	—	166	MHz
Output clock rise time	tr	CLK1 to CLK3 CLK5 to CLK9	0.2 × V_{DD} to 0.8 × V_{DD} Load capacitance 15 pF	0.4	—	4.0	ns
Output clock fall time	tf	CLK1 to CLK3 CLK5 to CLK9	0.2 × V_{DD} to 0.8 × V_{DD} Load capacitance 15 pF	0.4	—	4.0	ns
Output clock duty cycle	t_{DCC}	CLK1 to CLK3 CLK5 to CLK9	0.5 × V_{DD} Divided clock output	45	—	55	%
			0.5 × V_{DD} Reference clock output	40	—	60	
Modulation period	f_{MOD}	CLK1 to CLK3 CLK5 to CLK9	Input clock : 20 MHz	—	33.3	—	kHz
Lock-up time	t_{LK}	CLK1 to CLK3 CLK5 to CLK9	—	—	4	10	ms
Cycle-cycle jitter*	t_{JC}	CLK1 to CLK3 CLK5 to CLK9	Ta = + 25 °C, V_{DD} = 3.3 V, No load capacitance, Effective value	—	—	100	ps-rms
Power down enable “L” width	t_{PDLW}	XPD	—	1	—	—	µs
Power-on time	t_{VDR}	VDD	0.0 V to 3.0 V	100	—	—	µs
“L” output start time after power down entry	t_{PEL}	CLK1 to CLK3 CLK5 to CLK9	When PD rise/fall time is 5 ns	—	—	10	ns
“L” output release time after power down exit	t_{PIL}	CLK1 to CLK3 CLK5 to CLK9	When PD rise/fall time is 5 ns	0	—	—	ns
Output start time after power down exit	t_{PIO}	CLK1 to CLK3 CLK5 to CLK9	When PD rise/fall time is 5 ns No load capacitance 15 pF	—	—	10	ns

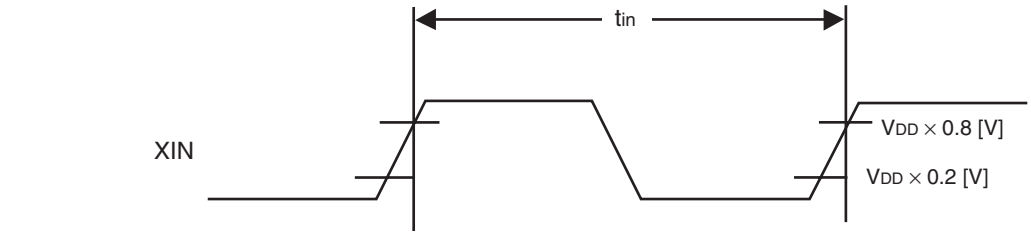
* : The rated value when outputting on only one pin.
The jitter value varies depending on the combination of output frequency and output pin.

Note : The modulation clock stabilization wait time is required after the power is turned on, or when the settings are changed for power down, multiplication index and modulation. Ensure that the modulation clock stabilization wait time has as long as the maximum lock-up time.

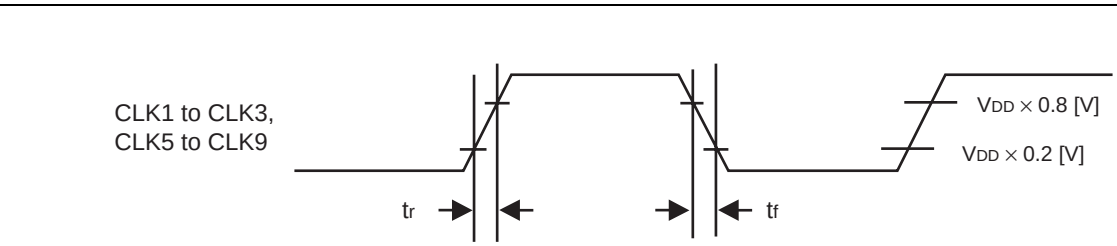
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)



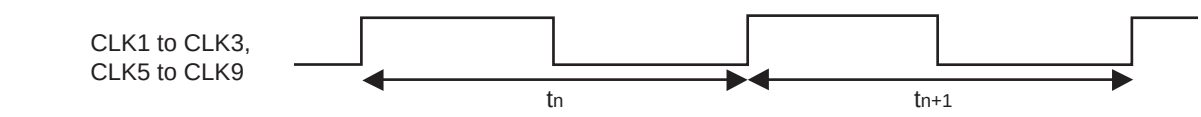
■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)



■ OUTPUT SLEW RATE

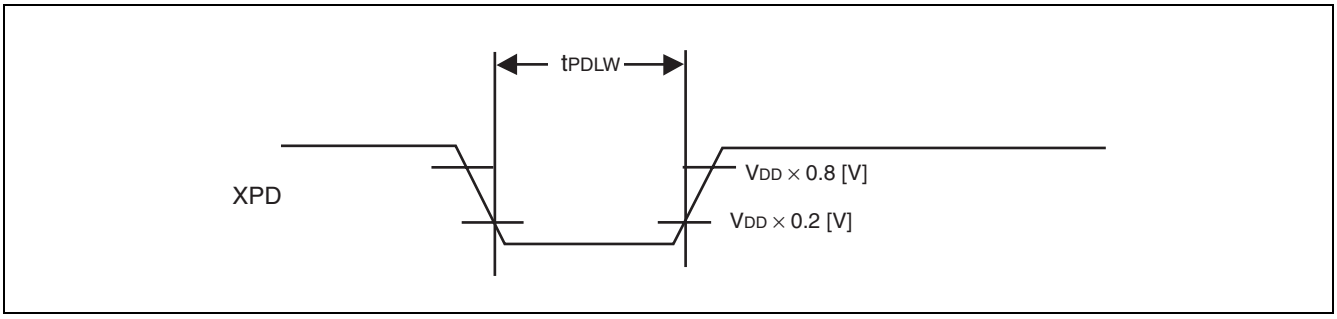


■ CYCLE-CYCLE JITTER ($t_{JC} = |t_n - t_{n+1}|$)

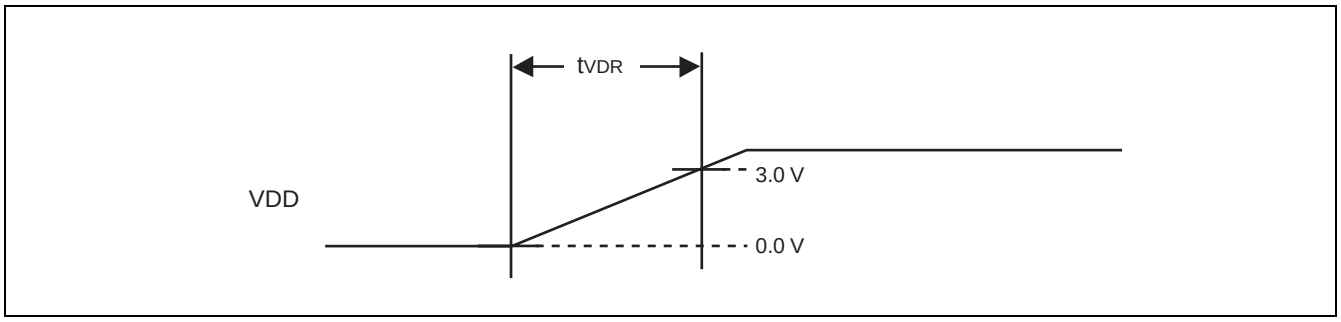


Note : Cycle-cycle jitter is defined as the difference in the period between a given cycle and the following cycle (or the previous cycle).

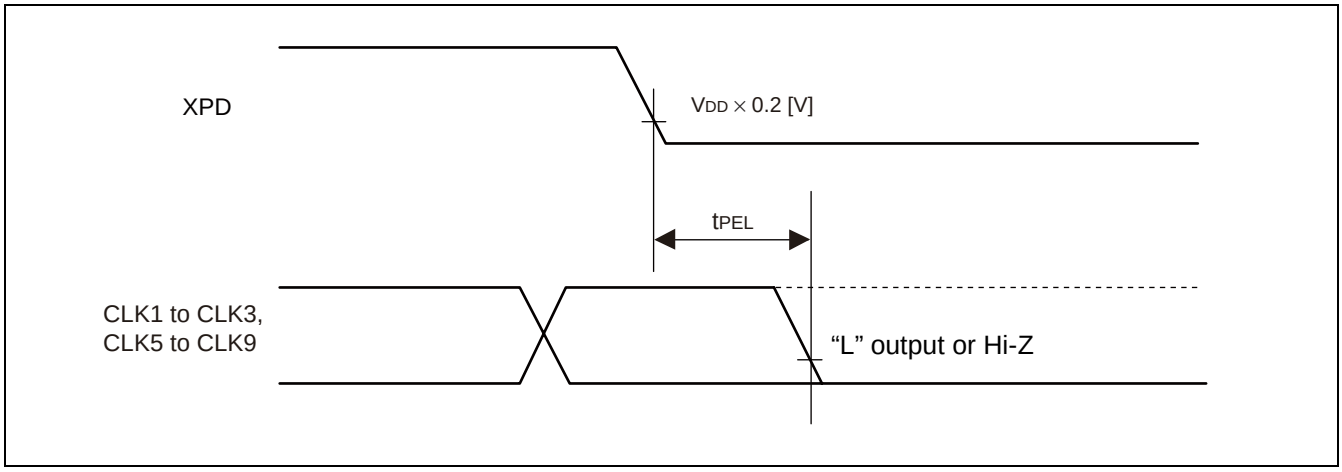
■ POWER DOWN “L” WIDTH



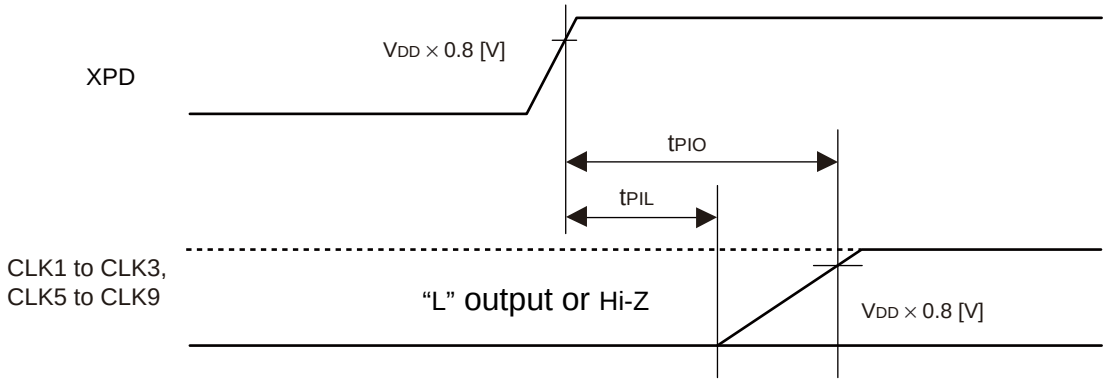
■ POWER-ON TIME



■ “L” OUTPUT START TIME AFTER POWER DOWN ENTRY

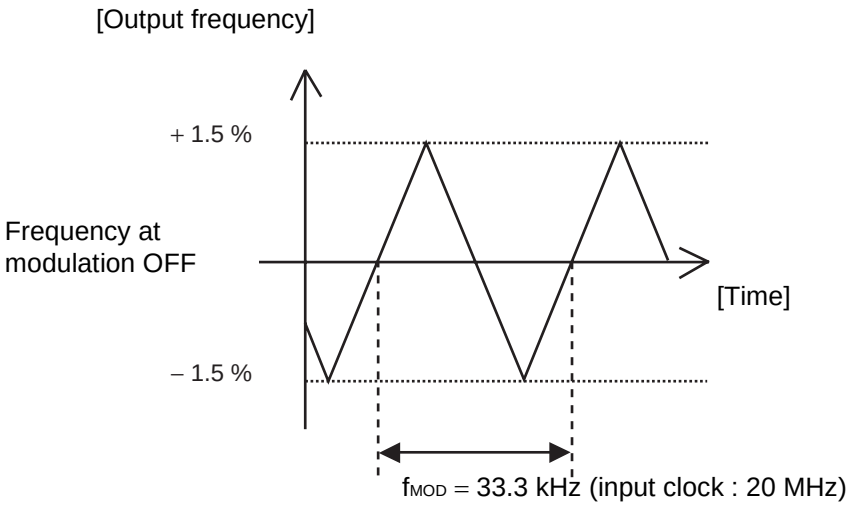


■ “L” OUTPUT RELEASE TIME AND OUTPUT START TIME AFTER POWER DOWN EXIT



■ MODULATION WAVEFORM

- ± 1.5%, example of center spread

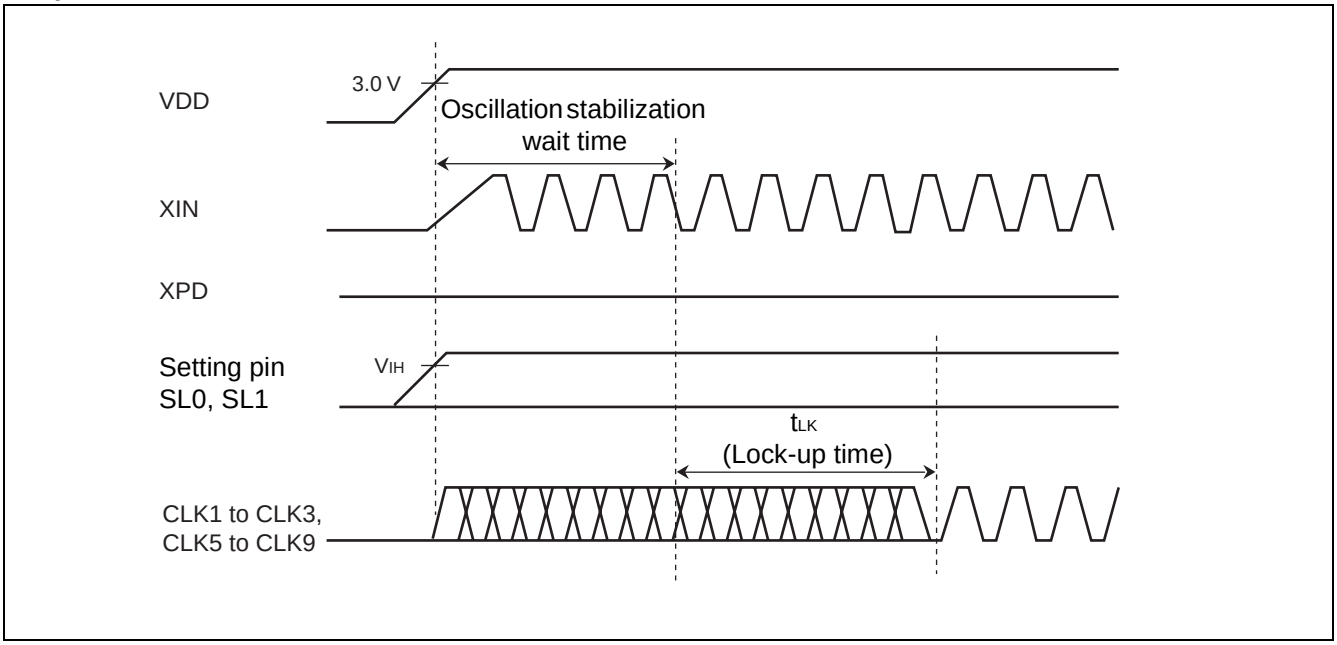


■ LOCK-UP TIME

The clock outputs from the CLK1 to CLK3 and CLK5 to CLK9 pins conform to the ratings after the lock-up time (t_{LK}) has elapsed after the states of all of the power supply, input clock, and pin settings have stabilized. The output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter are not guaranteed during the lock-up period. It is therefore recommended that processing, such as releasing device reset, is performed until after the lock-up time has elapsed.

Check the characteristics of the oscillator or clock being used for the stabilization wait time of the input clock. If the built-in oscillator circuit is used, the stabilization wait time depends on the characteristics of the oscillator.

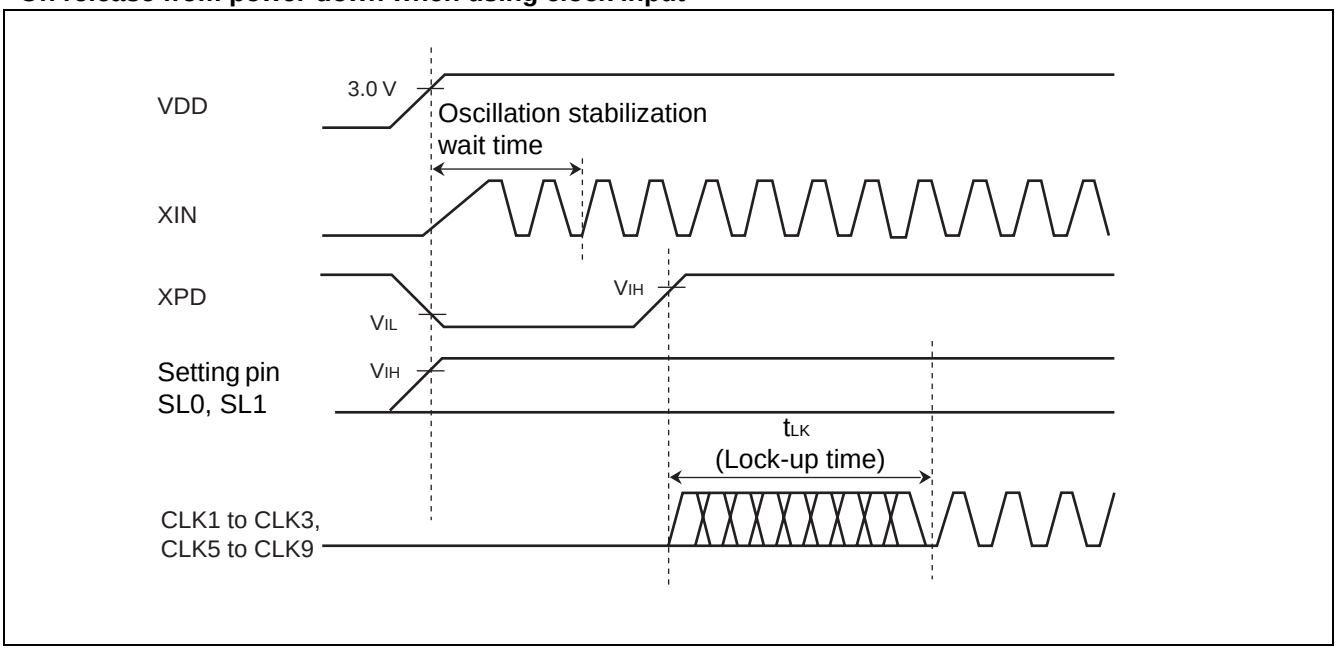
<At power-on>



The input clock oscillation stabilization wait time is required when the power is turned on.

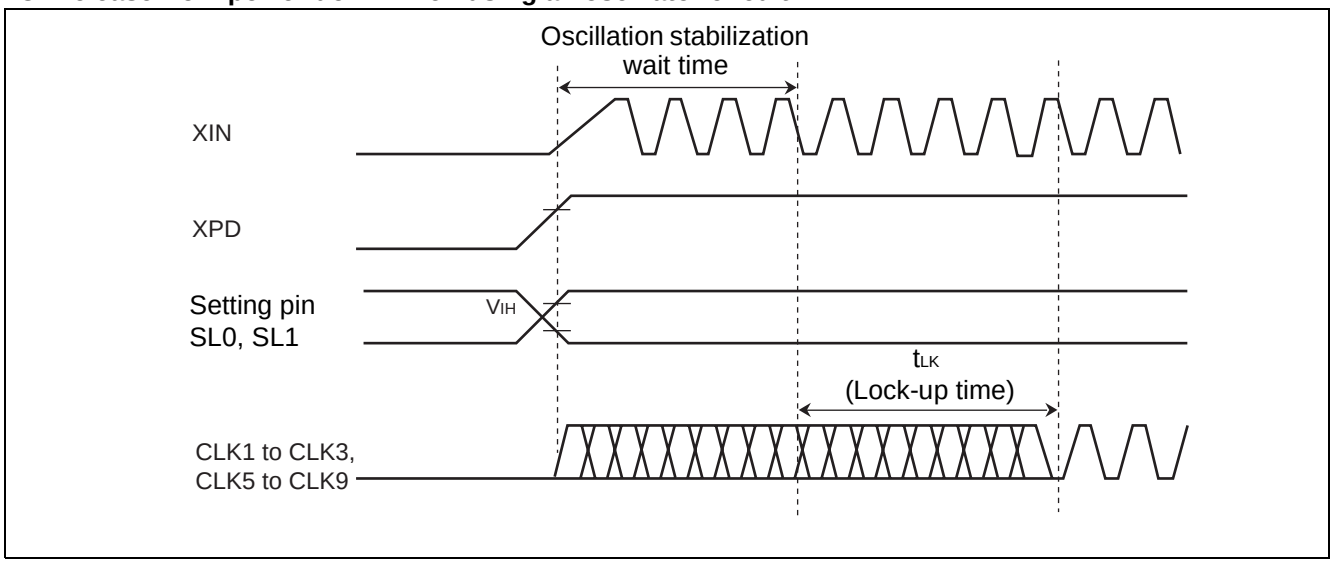
When the XPD pin is fixed at “H”, the desired clock can be obtained after a maximum of the stabilization wait time of the clock being input to XIN plus the lock-up time (t_{LK}) has elapsed.

<On release from power-down when using clock input>



When the power down is controlled by the XPD pin, the desired clock is obtained after the pin is set to “H” level until the maximum lock-up time t_{LK} has elapsed.

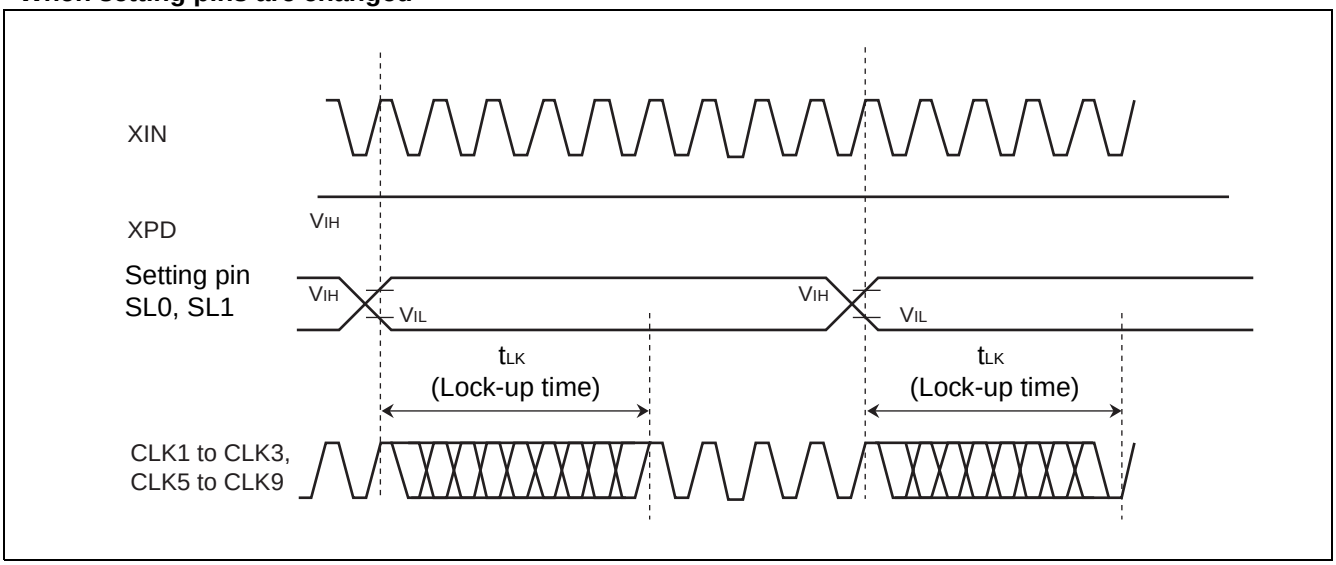
<On release from power-down when using an oscillator circuit>



When the XPD pin is set to an “L” level, the device enters power-down mode, and oscillator on the XIN and XOUT pins is stopped in order to stop the internal oscillator circuit of the device.

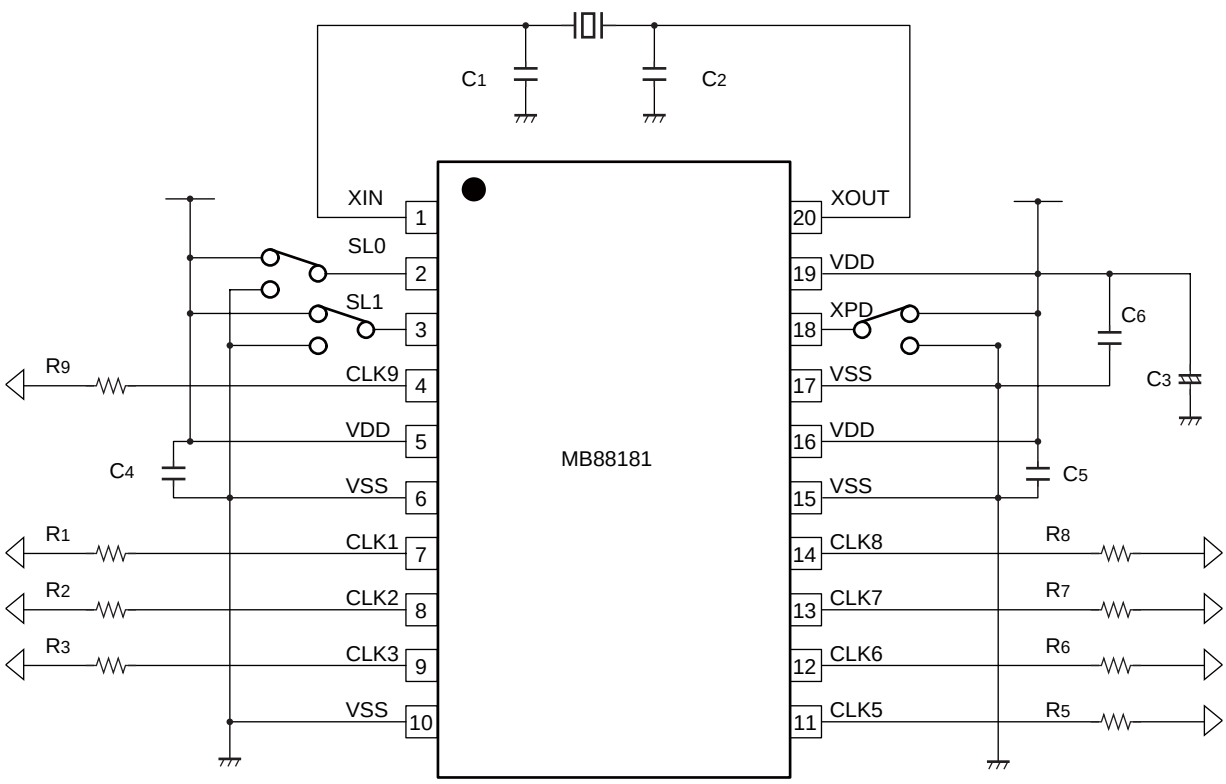
When the XPD pin is set to the “H” level and the device changes to normal operating mode, the oscillator circuit begins operating and the XIN and XOUT oscillator is started. However, a prescribed time is required until the input clock becomes stable (the stabilization wait time). Furthermore, because the lock-up time is required before the output clock stabilizes, the maximum amount of time from when the power-down is released until the output clock stabilizes is [oscillator stabilization time] + [lock-up time].

<When setting pins are changed>



If the clock is controlled by changing the setting pins (SL0, SL1) during operation, the desired clock signal can be obtained when a maximum of the lock-up time (t_{LK}) has elapsed after the setting pins are set.

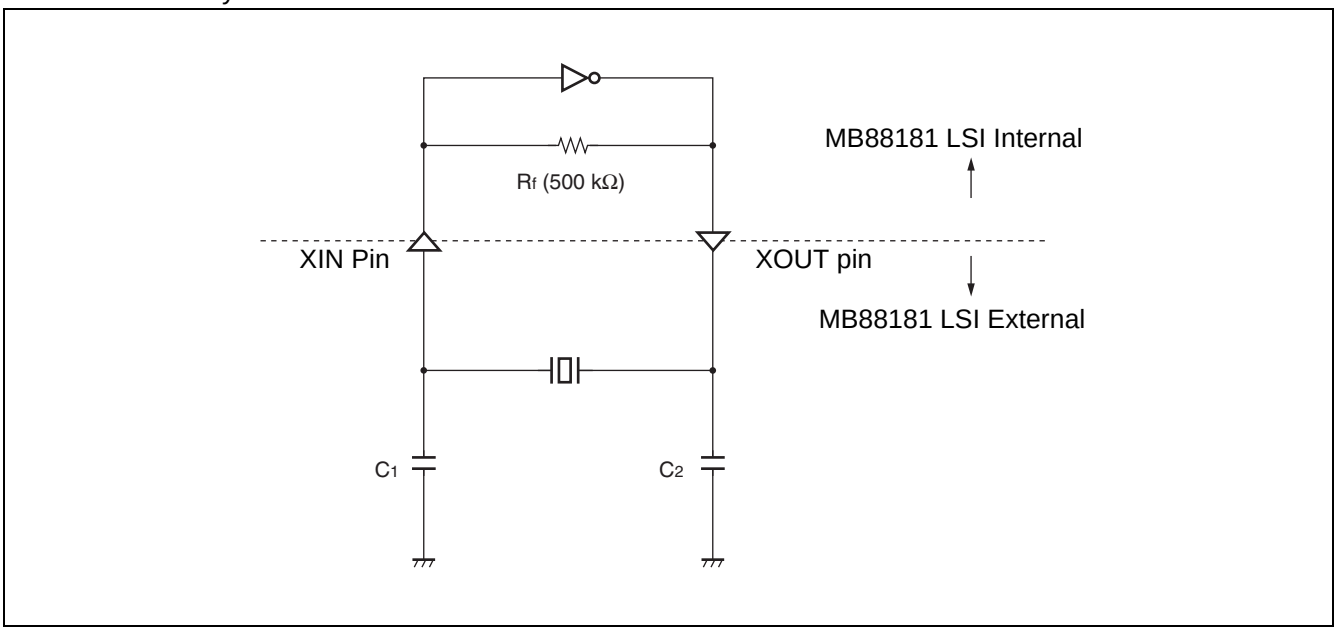
■ RECOMMENDED CIRCUIT



C_1, C_2	: Oscillation stabilization capacitors (refer to the following description)
C_3	: Tantalum capacitor or electrolytic of 10 μF or higher
C_4 to C_6	: Laminated ceramic capacitor about 0.01 μF (connect the capacitor close to the SSCG.)
R_1 to R_3, R_5 to R_9	: Resistors for impedance matching with the board pattern

■ CRYSTAL OSCILLATOR CIRCUIT

The figure below shows an example of the connection of a generic crystal oscillator. The oscillator circuit has a built-in feedback resistance (500 kΩ). The values of the capacitors (C1 and C2) need to be set to the optimal values of the crystal oscillator.



■ EXAMPLE OUTPUT SETTINGS

The following table shows examples of the M and N frequency dividers, the output frequency divider, and the modulation index settings for each of the SL0 and SL1 pin settings.

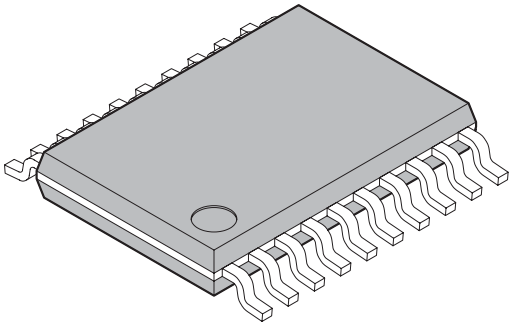
SL0	**0**	**1**	**0**	**1**	**Remarks**
SL1	**0**	**0**	**1**	**1**	
SSCG	200 MHz ± 1.0% modulation	200 MHz ± 1.0% modulation	300 MHz ± 1.0% modulation	300 MHz ± 2.0% modulation	
PLL1	300 MHz	300 MHz	350 MHz	350 MHz	No modulation
PLL2	158 MHz	158 MHz	158 MHz	158 MHz	No modulation
PLL3	330 MHz	330 MHz	260 MHz	260 MHz	No modulation
CLK1	Divided by 10 of SSCG 20 MHz output ± 1.0% modulation	Divided by 10 of SSCG 20 MHz output ± 2.0% modulation	Divided by 15 of SSCG 20 MHz output ± 1.0% modulation	Divided by 15 of SSCG 20 MHz output ± 2.0% modulation	CLK divided by SSCG or PLL2
CLK2	REF output	REF output	REF output	REF output	CLK divided by PLL1 or REFCLK
CLK3	REF output	REF output	Divided by 4 of PLL3 65 MHz output	Divided by 5 of PLL3 52 MHz output	CLK divided by PLL3 or REFCLK
CLK5	Divided by 4 of PLL2 39.5 MHz output	Divided by 4 of PLL2 39.5 MHz output	Divided by 4 of PLL2 39.5 MHz output	Divided by 4 of PLL2 39.5 MHz output	CLK divided by PLL2
CLK6	Divided by 12 of PLL3 27.5 MHz output	Divided by 12 of PLL3 27.5 MHz output	Divided by 8 of PLL3 27.5 MHz output	Divided by 8 of PLL3 27.5 MHz output	CLK divided by PLL3
CLK7	No output	No output	Divided by 4 of SSCG 75 MHz output ± 1.0% modulation	Divided by 4 of SSCG 75 MHz output ± 2.0% modulation	CLK divided by SSCG or PLL2
CLK8	Divided by 4 of SSCG 50 MHz output ± 1.0% modulation	Divided by 5 of SSCG 40 MHz output ± 1.0% modulation	No output	No output	CLK divided by SSCG or PLL2
CLK9	Divided by 15 of PLL3 22 MHz output	Divided by 5 of PLL3 66 MHz output	Divided by 5 of PLL1 70 MHz output	Divided by 14 of PLL1 25 MHz output	CLK divided by PLL1 or PLL3

■ ORDERING INFORMATION

Part number	Package
MB88181PFT-G-XXX-BNDE1	20-pin plastic TSSOP (FPT-20P-M06)

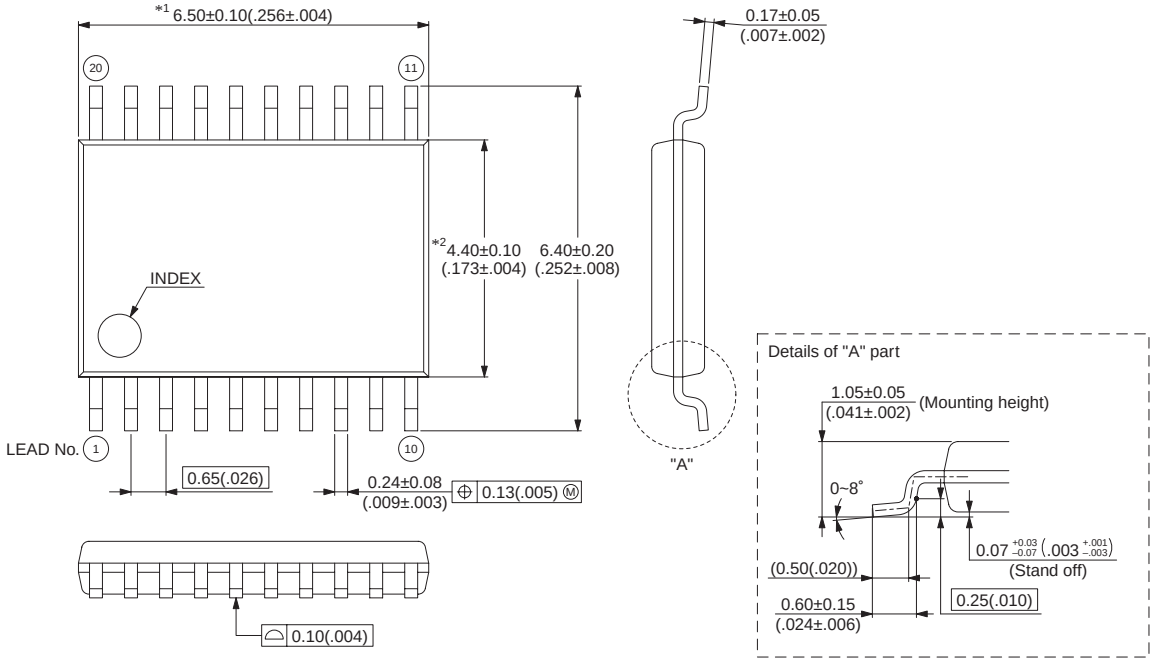
Note : The different figures XXX are assigned by the mask options.

■ PACKAGE DIMENSION

20-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.10 mm MAX
	Weight	0.08g
(FPT-20P-M06)	Code (Reference)	P-TSSOP20-4.4×6.5-0.65

20-pin plastic TSSOP
(FPT-20P-M06)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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