# MC9S08DZ128 Data Sheet Errata

by:   Microcontroller Division

This errata document describes corrections to the *MC9S08DZ128 Data Sheet*, order number MC9S08DZ128. For convenience, the addenda items are grouped by revision. Please check our website at www.freescale.com for the latest updates.

The current version available of the *MC9S08DZ128 Data Sheet* is Revision 1.

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# 1 Errata for Revision 1

**Table 1. MC9S08DZ128 Rev 1 Errata**

| Location | Description |
|---|---|
| Table 2-1, "Pin Availability by Package Pin-Count"/Page 34 | Pin assignments for rows numbered 9–15 in table 2-1 required updating. The correct information is shown below. |
| 16.4.2.3 Edge-Aligned PWM Mode/Page 373 | Add the following text at the end of Section 16.4.2.3:<br><br>Writing to TPMxSC cancels any values written to TPMxMODH and/or TPMxMODL and resets the coherency mechanism for the modulo registers. Writing to TPMxCnSC cancels any values written to the channel value registers and resets the coherency mechanism for TPMxCnVH:TPMxCnVL. |

Table within first row:

| Pin Number | | | <-- Lowest **Priority** --> Highest | | | |
|---|---|---|---|---|---|---|
| **100** | **64** | **48** | **Port Pin/Interrupt** | | **Alt 1** | **Alt 2** |
| 9 | 7 | 4 | | | | $V_{DD}$ |
| 10 | 8 | 5 | | | | $V_{SS}$ |
| 11 | 9 | 6 | PTG0 | | EXTAL | |
| 12 | 10 | 7 | PTG1 | | XTAL | |
| 13 | 11 | 8 | | | | $\overline{RESET}$ |
| 14 | — | — | PTJ2 | PIJ2 | TPM3CH2 | |
| 15 | — | — | PTJ3 | PIJ3 | TPM3CH3 | |

# 2 Revision History

Table 2 provides a revision history for this document.

**Table 2. Revision History Table**

| Rev. Number | Substantive Changes | Date of Release |
|---|---|---|
| 0 | • Initial release. | 10/2010 |
| 1 | • Added update to Edge-Aligned PWM Mode section. | 7/2011 |

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