Reference Manual

DOC. REV. 10/17/2013

VL-EPICs-36 (Komodo)

Intel Core 2 Duo Based SBC with Ethernet, Video, SUMIT and PC/104 interface

VERSALOGIC CORPORATION

WWW.VERSALOGIC.COM

12100 SW Tualatin Road
Tualatin, OR 97062-7341
(503) 747-2261
Fax (971) 224-4708

Notice:

Although every effort has been made to ensure this document is error-free, VersaLogic makes no representations or warranties with respect to this product and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose.

VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

PC/104 and the PC/104 logo are trademarks of the PC/104 Consortium.

The SUMIT name and logo are trademarks of the Small Form Factor Special Interest Group.

Product Release Notes

Rev 1.00 – Initial commercial release.

Support Page

The VL-EPICs-36 support page, at http://www.versalogic.com/private/komodosupport.asp, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades

This is a private page for VL-EPICs-36 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

Contents

1 Introduction

Description

Features and Construction

The VL-EPICs-36 is a feature-packed single board computer (SBC) designed for OEM control projects requiring fast processing and designed-in reliability and longevity (product lifespan). Its features include:

- Intel Core 2 Duo 2.267 GHz, 1067 MT/s FSB, 3 MB cache
- Up to 4 GB DDR3 socketed memory, one SO-DIMM
- MiniBlade SSD interface supports USB 2.0 and SATA 2.0 (3 Gb/s)
- Intel 82574IT based Ethernet interface, autodetect 10BaseT / 100BaseTX / 1000BaseT
- High speed 3D video accelerator (Gen 5.0) with analog and LVDS flat panel outputs
- SUMIT-A and SUMIT-B expansion, supports three PCIe x1 lanes, LPC, SPI, USB, and SMBus
- Two SATA ports
- One eUSB port
- PC/104 (ISA) expansion
- Ten USB 2.0 channels for keyboard, mouse, floppy, and other devices
- TVS devices for ESD protection
- Intel High Definition Audio (HDA) compatible
- CPU temperature sensor
- Two RS-232 and two RS-232/422/485 COM ports, 460K baud max.
- Expansion with VersaLogic SPX add-on I/O modules
- EPIC-compliant 4.5” x 6.5” footprint
- Field upgradeable BIOS with OEM enhancements
- Customizing available

The VL-EPICs-36 is a SUMIT-EPIC single board computer with an Intel Core 2 Duo processor. The board is compatible with popular operating systems such as Windows, QNX, VxWorks and Linux.

The VL-EPICs-36 features high reliability design and construction, including voltage sensing reset circuits and self-resetting fuses on the 5V and 3.3V supplies to the user I/O connectors.

VL-EPICs-36 boards are subjected to 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service and product longevity for this exceptional SBC.

The VL-EPICs-36 is equipped with a multifunction utility cable (breakout board) that provides standard I/O interfaces, including four COM ports, PS/2 mouse and keyboard, pushbutton reset, programmable LED and speaker. Additional I/O expansion is available through the high-speed SUMIT AB (PCI Express) and PC/104 (ISA) connectors.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size:
4.5" x 6.5" (EPIC standard)

Storage Temperature:
-40° C to 85° C

Operating Temperature:
VL-EPICs-36S: 0° C to +60° C free air, no airflow
VL-EPICs-36E: -40° C to +85° C free air

Power Requirements: *(+5 V with 1 GB RAM, keyboard and mouse, running Windows XP)*
VL-EPICs-36S: Idle 2.5A (12.5W), Typical 4.8A (24W), Max 5.5A (27.5W)
VL-EPICs-36E: Idle 2.3A (11.5W), Typical 3.2A (16W), 3.9A (19.5W)
+3.3V or ± 12V might be required by some expansion modules

System Reset:
Major power rails monitored by Super I/O chip
CPU and base board temperature monitoring
Fan monitor

DRAM:
One SO-DIMM socket up to 4 GB DDR3

Video Interface:
Up to 1280 x 1024 (18/24 bits)
LVDS output for TFT FPDs
VGA standard output
Simultaneous independent analog/FPD output

SATA Interface:
Two SATA headers plus MiniBlade

Flash Storage:
MiniBlade (USB 2.0 / SATA 2.0)
eUSB (USB 2.0)

Ethernet Interface:
Intel 82574IT based 10BaseT / 100GBaseTX / 1000BaseT Ethernet Controller

COM1-2 Interface:
RS-232, 16C550 compatible, 115 kbps max., full 9-wire

COM3-4 Interface:
RS-232/422/485, 16C550 compatible, 460 kbps max., 4-wire RS-232

USB:
Ten USB 2.0. Four USB type A ports (on-board), four channels on SUMIT A connector, one channel on MiniBlade, and one on eUSB.

Audio:
HD audio CODEC
Stereo Line in and Stereo Line out

SPX:
Supports four external SPI chips of user design or any SPX™ series expansion board

BIOS:
Phoenix Technologies Embedded BIOS with OEM enhancements
Field-upgradeable with Flash BIOS Update Utility

Bus Speed:
CPU FSB: VL-EPICs-36S: 1.066 GHz; VL-EPICs-36E: 800 MHz
DDR3: VL-EPICs-36S: 1066 MT/s; VL-EPICs-36E: 800 MT/s
PCI Express: 2.5 Gbps
USB 2.0: 480 Mbps
LPC: 33.33 MHz
PC/104 (ISA): 8.33 MHz
SPI/SPX: 8 MHz max.

Compatibility:
SUMIT – Three x1 PCIe lanes, LPC, SPI, USB
PC/104 – Partial compliance

Weight:
VL-EPICs-36S – 0.672 lbs (0.304 kg)
VL-EPICs-36E – 0.671 lbs (0.304 kg)

SUMIT Resources

Form Factor: SUMIT-EPIC

	SUMIT A	SUMIT B
PCIe x1	1	2
PCIe x4		–
USB	4	
ExpressCard	–	
LPC	✓	
SPI / uWire	SPI	
SMBus/ I^2C	SMBus	
+12V	✓	
+5V	✓	✓
+5Vsb	+5V	+5V
+3.3V	✓	✓

Specifications are subject to change without notice.

VL-EPICs-36 Block Diagram

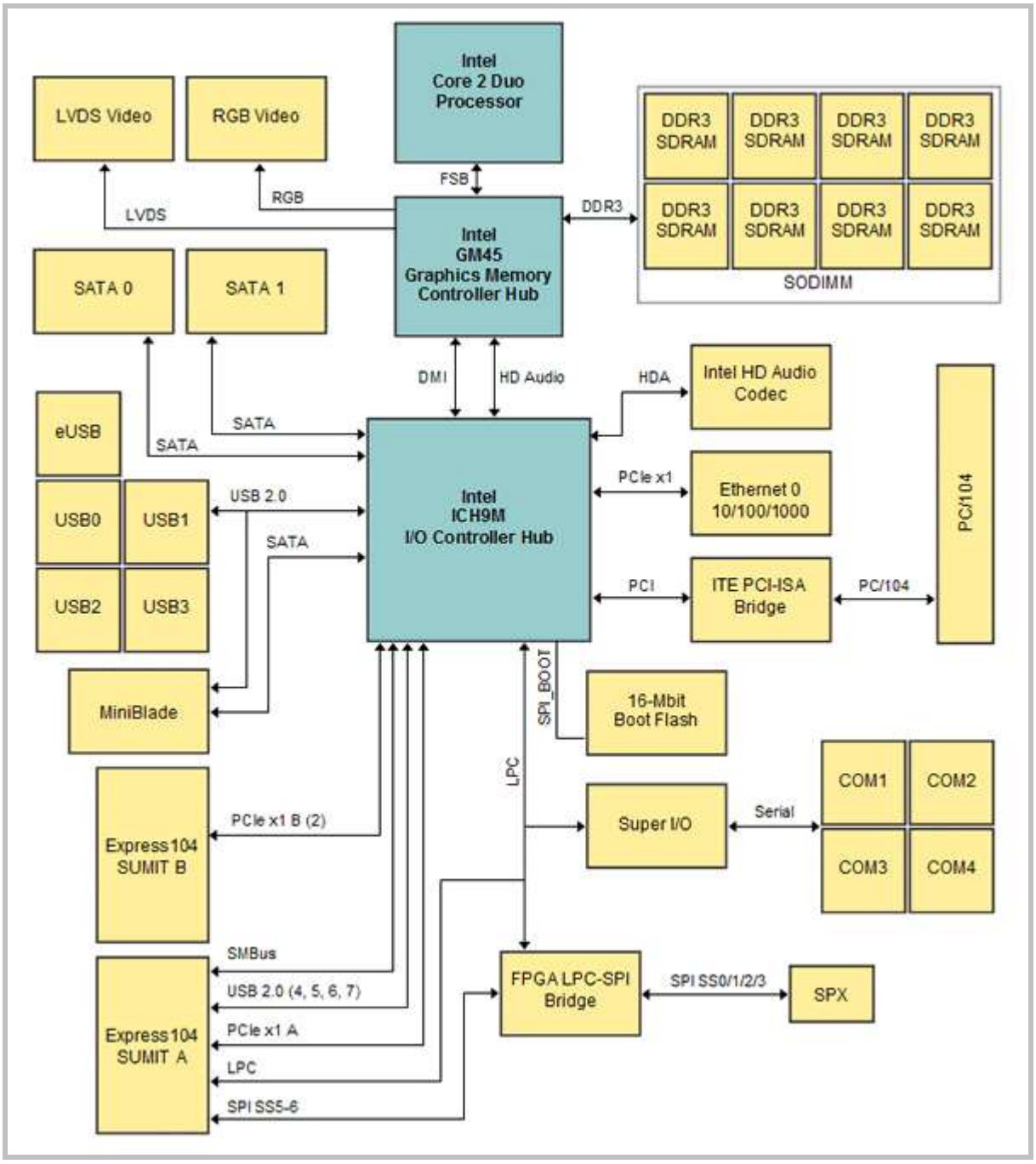

Figure 1. System Block Diagram

Thermal Considerations

CPU Die Temperature

The CPU die temperature is affected by numerous conditions, such as CPU utilization, CPU speed, ambient air temperature, air flow, thermal effects of adjacent circuit boards, external heat sources, and many others.

The CPU is protected from over temperature conditions by several mechanisms.

The CPU will automatically slow down by 50% whenever its die temperature exceeds 105° C. When the temperature falls back below 105° C, the CPU resumes full speed operation.

As a failsafe, if the CPU die temperature climbs above 115° C, the CPU will turn itself off to prevent damage to the chip.

Note: Intel does not warrant their CPUs in the event of this occurrence.

Model Differences

VersaLogic offers both standard and extended temperature models of the VL-EPM-35. The basic operating temperature specification for both models is shown below.

- VL-EPICs-36S: 0° C to +60° C free air, no airflow
- VL-EPICs-36E: -40° C to +85° C free air

To reliably function at extreme temperatures the extended temperature model specifications deviate from the standard model in the following ways:

- The DRAM interface is slowed. PC3-6400 memory runs at 600 MHz. PC3-8500 memory runs at 800 MHz.
- The DRAM refresh rates are doubled.
- The Front Side Bus speed is reduced to 800 MHz.
- Maximum processor speed is limited to 1200 MHz.
- The graphics core is limited to 400 MHz.

RoHS Compliance

The VL-EPICs-36 is RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

Electrostatic Discharge

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the VL-EPICs-36.

Lithium Battery

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner.

HANDLING CARE

Warning! Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling, resulting in CMOS resetting to factory defaults.

Technical Support

If you are unable to solve a problem after reading this manual please visit the VL-EPICs-36 Product Support web page below. The support page provides links to component datasheets, device drivers, and BIOS and PLD code updates.

VL-EPICs-36 Support Page

The VersaTech KnowledgeBase contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the VL-EPICs-36.

VersaTech KnowledgeBase

If you have further questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling(503) 747-2261.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contacted if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning.

Configuration and Setup

2

Initial Configuration

The following components are recommended for a typical development system.

- VL-EPICs-36 Computer
- ATX Power Supply
- LVDS Display
- USB Keyboard
- USB Mouse
- SATA Hard Drive
- USB CD-ROM Drive
- DDR3 DRAM module

The following VersaLogic cables are recommended.

- VL-CBR-2010, 2011, or 2012 – LVDS cable
- VL-CBR-0701 – SATA data cable
- VL-CBR-0401 – ATX to SATA power cable
- VL-CBR-2022 – Main power cable

You will also need a Windows (or other OS) installation CD.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The VL-EPICs-36 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the VL-EPICs-36 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the VL-EPICs-36 and their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

Figure 2 shows a typical start-up configuration.

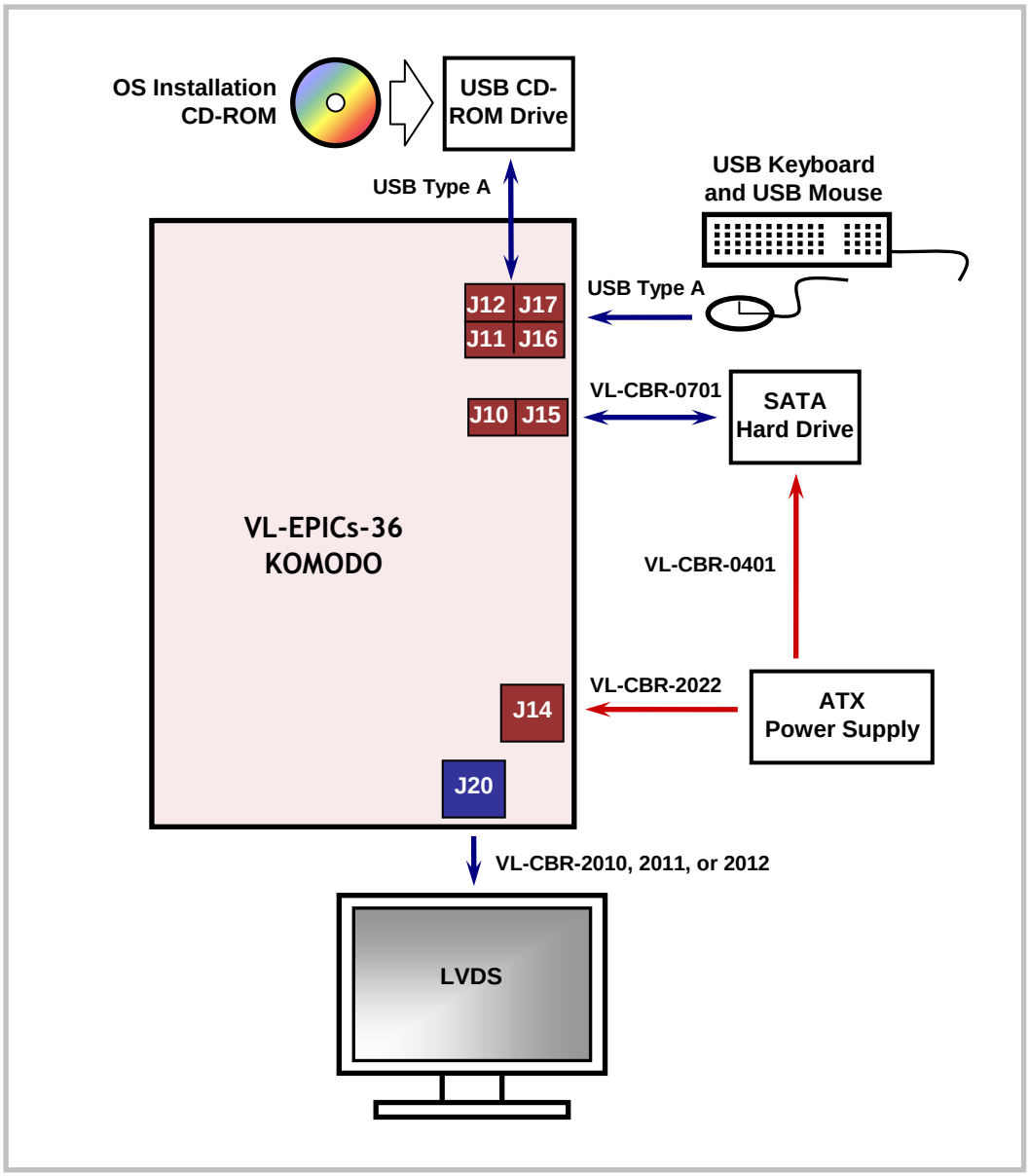

Figure 2. Typical Start-up Configuration

1. Install Memory

- Insert the DDR3 DRAM module into the SO-DIMM socket J21 on the bottom of the board and latch it into place.

2. Attach Cables and Peripherals

- Plug the LVDS adapter cable VL-CBR-2010, 2011, or 2012 into socket J20 on the bottom of the board. Attach the adapter cable to the LVDS display.
- Plug a USB keyboard and USB mouse into any Type A USB connector on the board (J11, J12, J16, or J17).
- Plug the SATA hard drive data cable VL-CBR-0701 into a SATA socket, J10 or J15. Attach a SATA hard drive to the cable.

- Attach an ATX to SATA cable VL-CBR-0401 to the ATX power supply and SATA drive.
- Attach a USB CD-ROM drive to any Type A USB connector on the board (J11, J12, J16, or J17).

3. Attach Power

- Plug the power adapter cable VL-CBR-2022 into socket J14. Attach the motherboard connector of the ATX power supply to the adapter.

4. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the VL-EPICs-36 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

6. Select a Boot Drive

- During startup, press the B key to display the boot menu. Insert the OS installation CD in the CD-ROM drive, and select to boot from the CD-ROM drive.

7. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

  Note: If you intend to operate the VL-EPICs-36 under Windows XP or Windows XP Embedded, be sure to use Service Pack 3 (SP3) for full support of the latest device features.

CMOS Setup

See VersaLogic KnowledgeBase article VT1648 – VL-EPICs-36 Komodo CMOS Setup Reference for complete information about CMOS Setup parameters.

Operating System Installation

The standard PC architecture used on the VL-EPICs-36 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the VL-EPICs-36 Product Support web page at http://www.versalogic.com/private/komodosupport.asp.

Dimensions and Mounting

VL-EPICs-36 Dimensions

The VL-EPICs-36 complies with all PC/104-Express standards. Dimensions are given below to help with pre-production planning and layout.

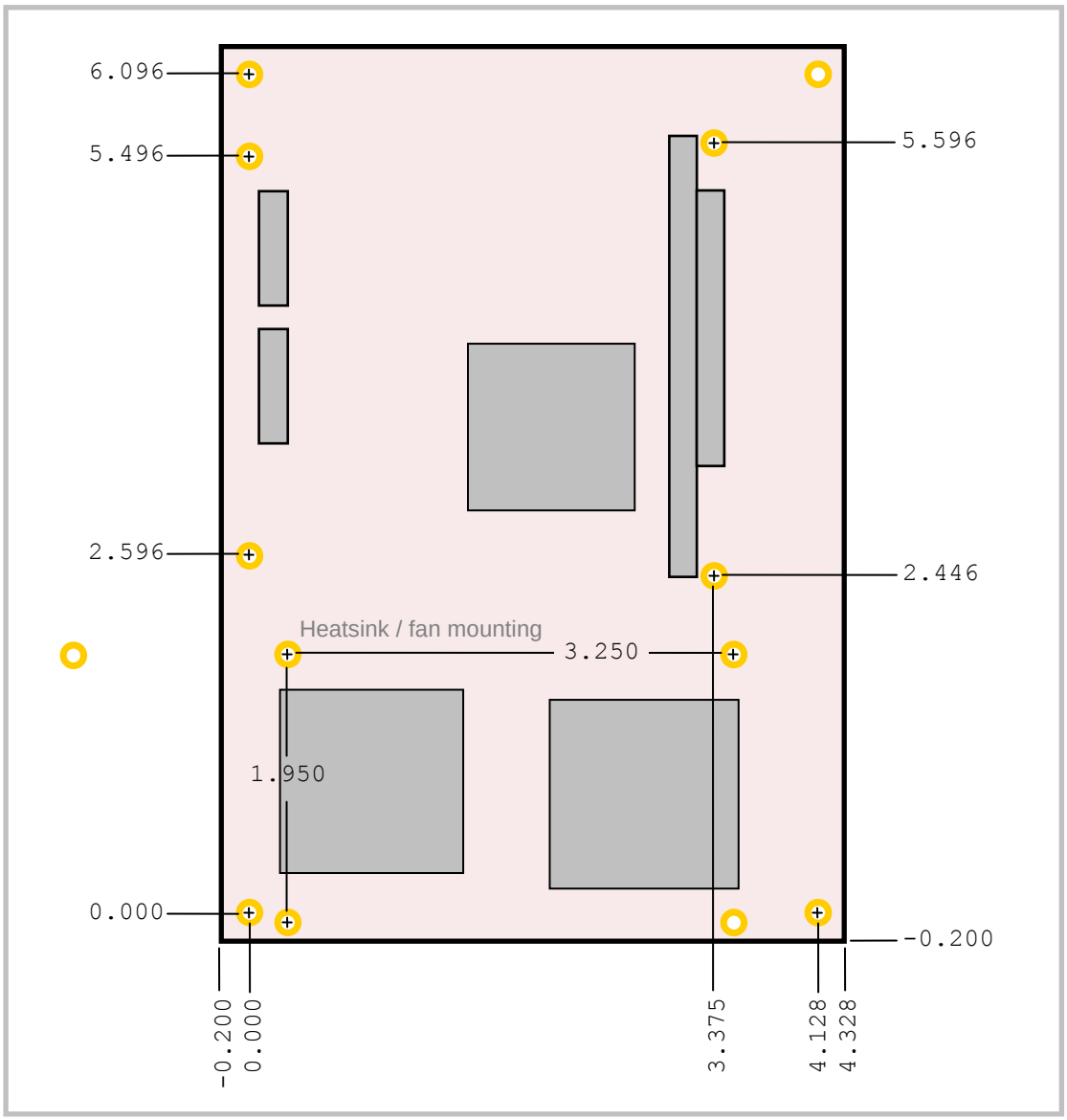

Figure 3.VL-EPICs-36 Dimensions and Mounting Holes

(Not to scale. All dimensions in inches.)

VL-CBR-5009 DIMENSIONS

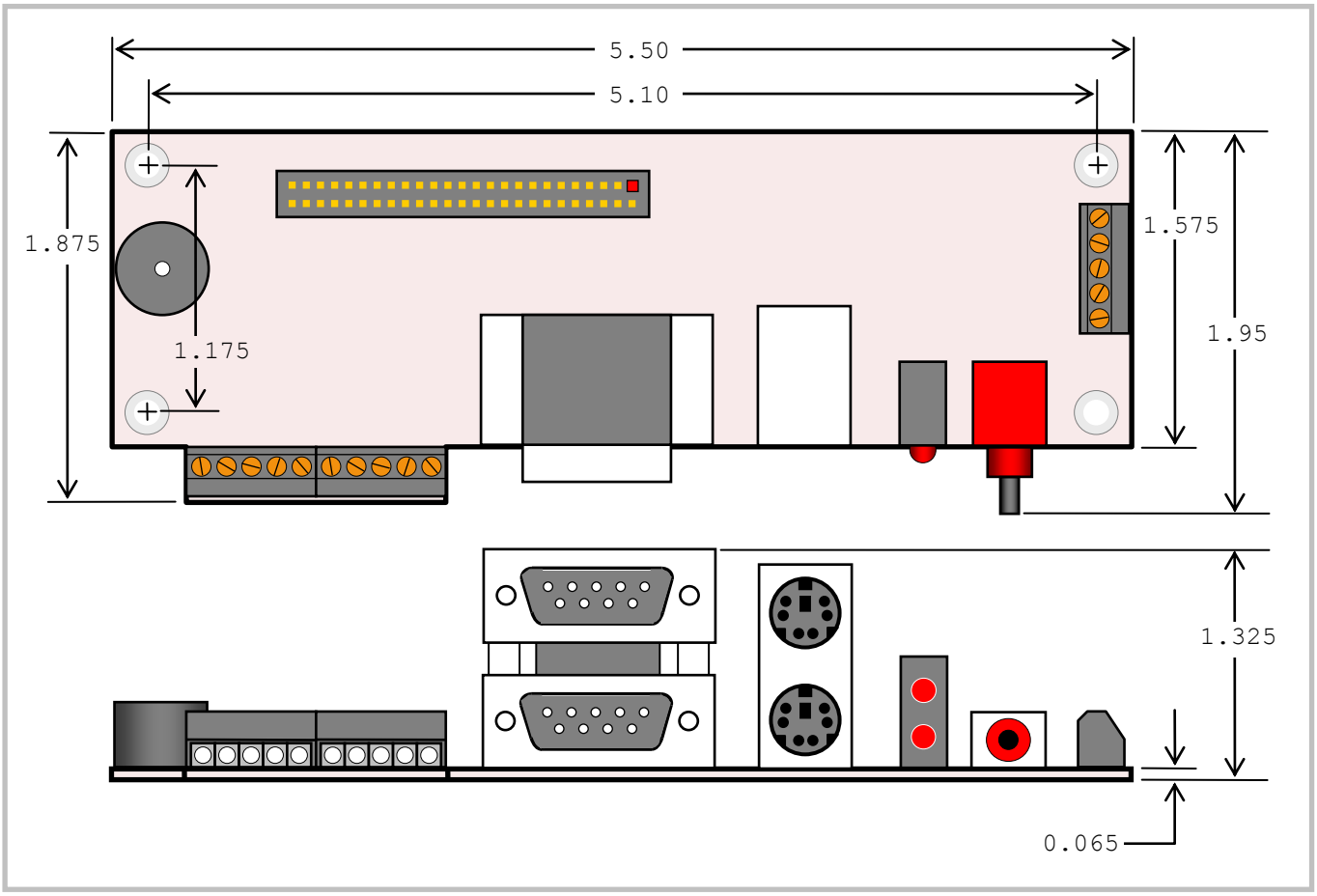

Figure 4. VL-CBR-5009 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The VL-EPICs-36 uses pass-through SUMIT (PCIe) and PC/104 (ISA) connectors so that expansion modules can be added to the top of the stack. A SUMIT expansion module with a PCIe x4 lane must be closest to the CPU board. Next on the stack would be an expansion module with a PCIe x1 lane. Above that, USB, SPI, SMBus and/or LPC SUMIT modules can be stacked. ISA modules must not be positioned between the VL-EPICs-36 and any SUMIT modules on the stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing. Four standoffs (B) must be used under the stack. These are secured with four male-female standoffs (C), threaded from the top side, which also serve as mounting struts for the SUMIT-PC/104 stack. Standoffs are secured to the top circuit board using pan head screws. See page 11 for dimensional details. Four standoffs and screws are available as part number VL-HDW-105. Note that the standoffs in this kit are 15.25 mm (0.60 inch), and must not be mixed with the 15.0 mm standoffs used for non-SUMIT boards.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack. Use caution when using the extractor tool not to damage any board components.

STANDOFF LOCATIONS

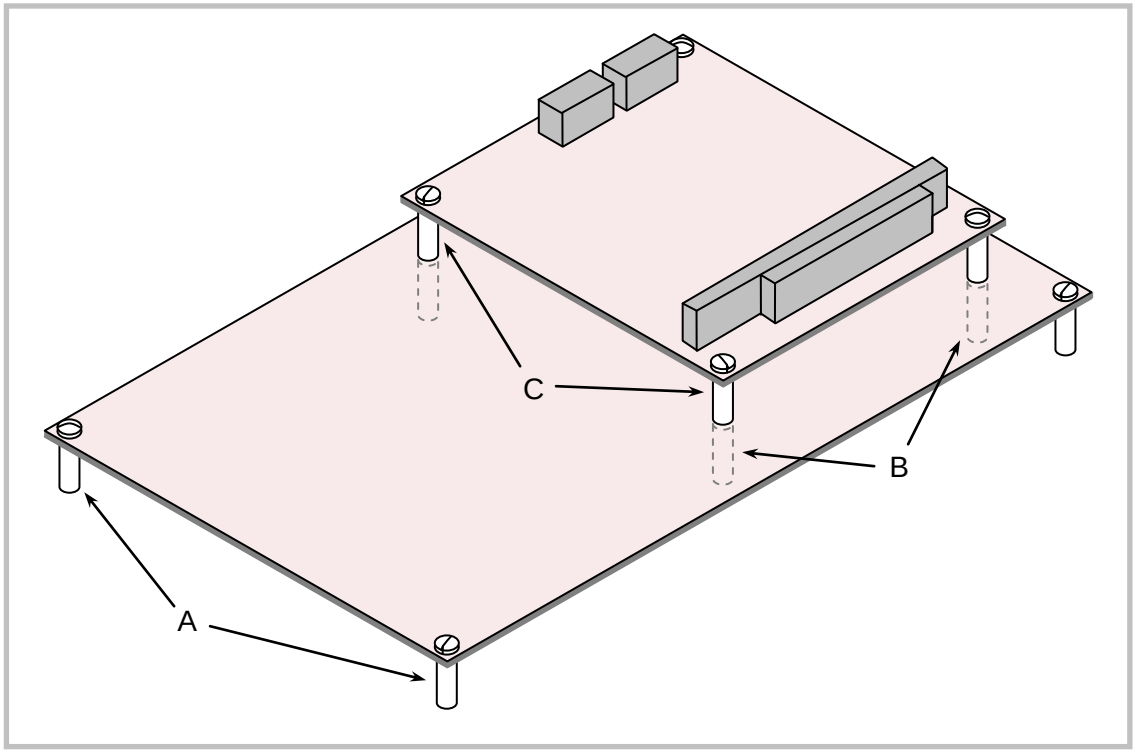

Figure 5. Standoff Locations

External Connectors

VL-EPICs-36 Connector Locations – Top

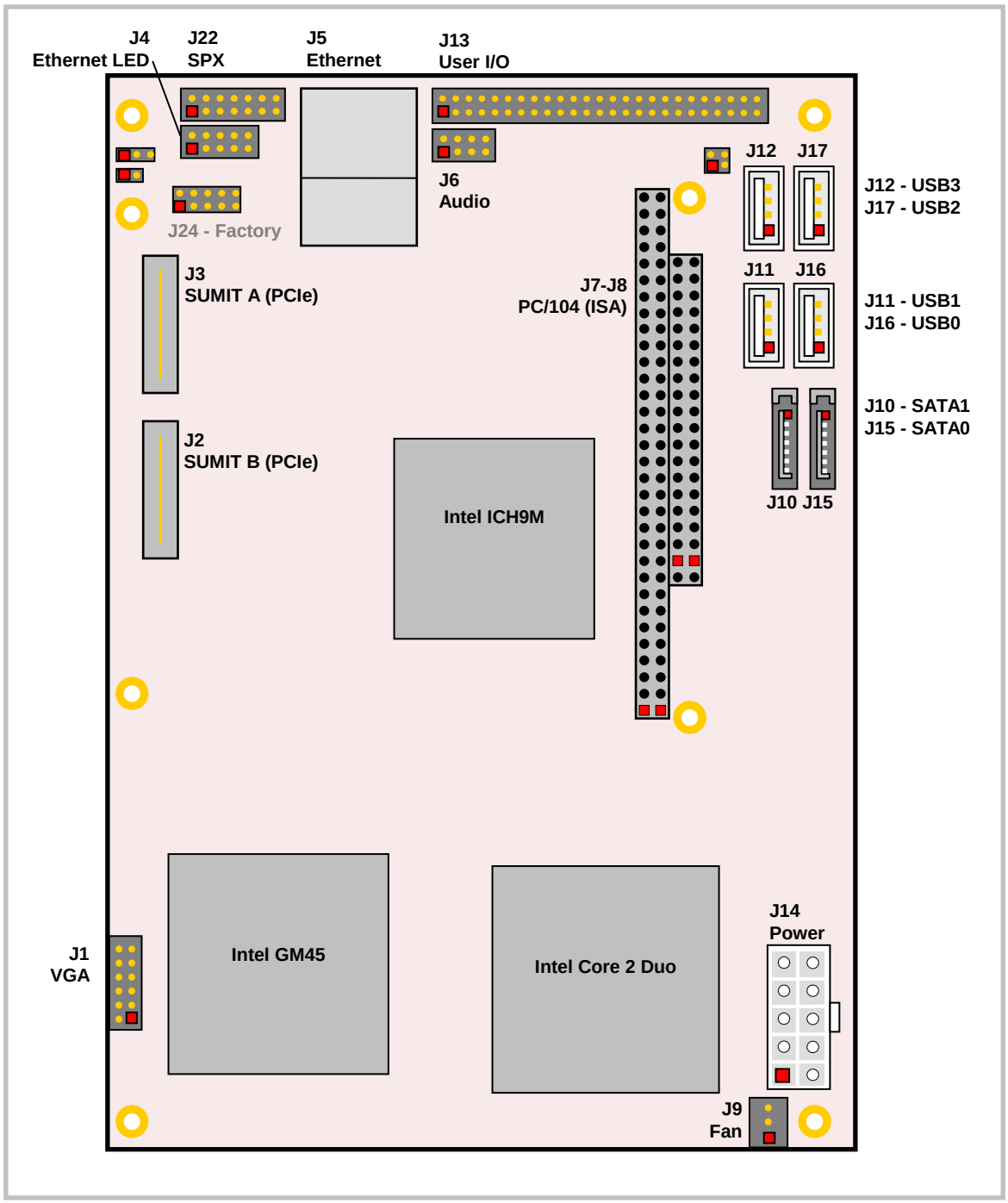

Figure 6. Connector Locations (Top)

VL-EPICS-36 CONNECTOR LOCATIONS – BOTTOM

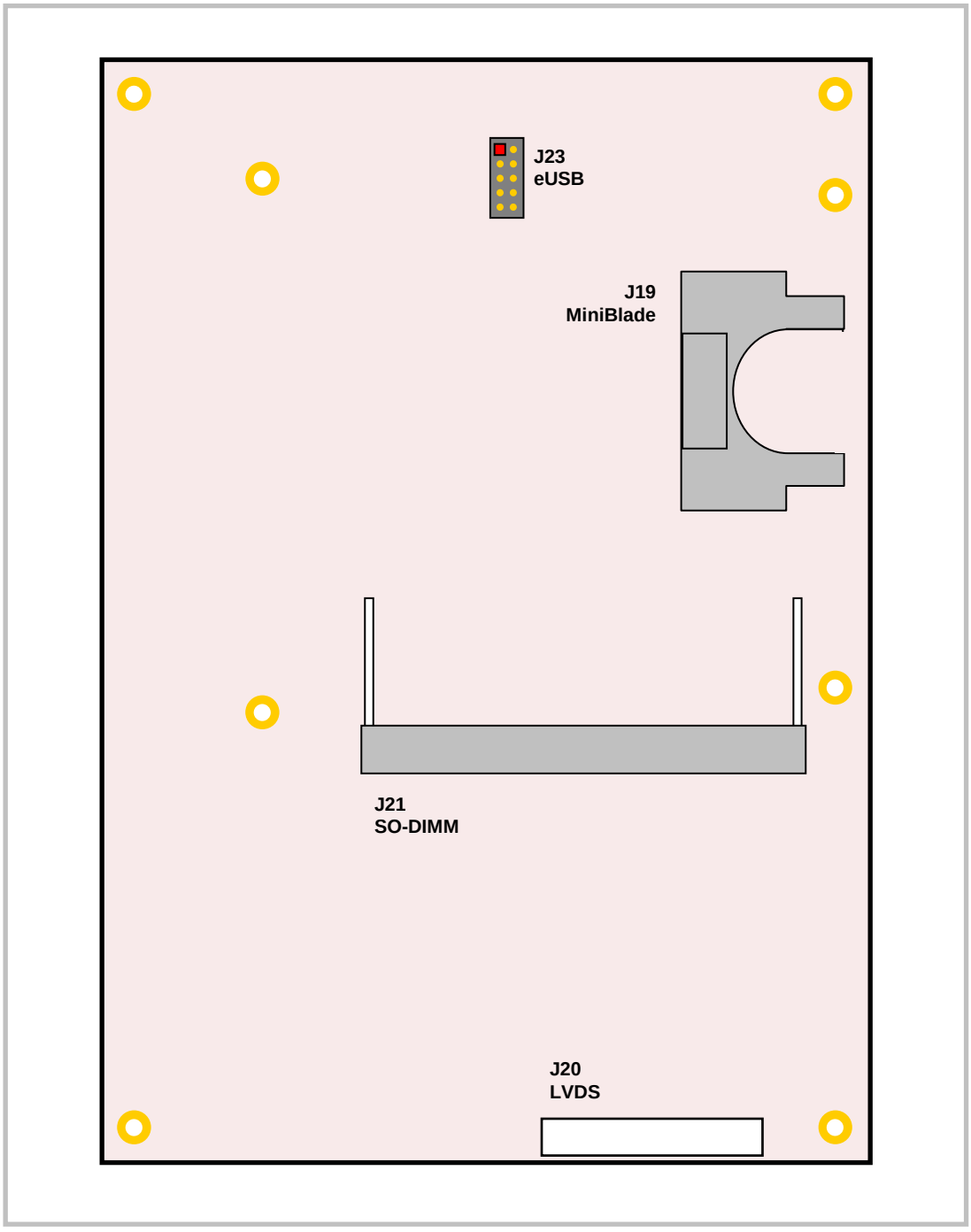

Figure 7. Connector Locations (Bottom)

VL-EPICs-36 Connector Functions and Interface Cables

Table 1 provides information about the function, mating connectors, and transition cables for VL-EPICs-36 connectors. Page numbers indicate where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Pin 1 Location[1] x coord.	Pin 1 Location[1] y coord.	Page
J1	SVGA Video Output	FCI 89361-712LF or FCI 89947-712LF	VL-CBR-1201	1' 12-pin 2mm IDC to 15-pin HD D-Sub VGA	-0.120	1.031	26
J2	SUMIT B – 2 PCIe x1 lanes	Samtec ASP-129637-01	—	—	0.052	4.115	29
J3	SUMIT A – 1 PCIe x1 lane, 4 USB, LPC, SPI, SMBus	Samtec ASP-129637-01	—	—	0.052	5.158	29
J4	Ethernet LED	—	—	—	1.174	5.517	31
J5	Gigabit Ethernet	RJ-45	—	—			31
J6	Audio	FCI 89947-708LF or FCI 89361-708LF	VL-CBR-0803	1' latching 8-pin 2mm to two 3.5mm stereo audio	1.914	5.887	32
J7-J8	PC/104	AMP 1375795-2	—	—	3.175[2]	2.496	33
J9	Fan	Molex 22-01-3027 or Molex 22-01-2025	Provided with assembly	—	3.823	-0.125	—
J10	SATA 1	Standard SATA	VL-CBR-0701 or VL-CBR-0702; VL-CBR-0401	500mm (19.75") 7-pin, straight-to-straight SATA data, friction or mechanical latching; ATX to SATA power adapter	3.968	4.265	34
J11	USB 1	Standard USB Type A	—	—	3.783	4.667	34
J12	USB 3	Standard USB Type A	—	—	3.783	5.387	34
J13	COM 1-4, PLED, keyboard, mouse, reset, speaker	FCI 89361-750LF	VL-CBR-5009	18" 2mm 50-pin to 50-pin IDC to breakout board VL-CBR-5009B	1.916	6.140	36
J14	Main Power Input	Molex 39-01-2100 Molex 39-00-0059 (10ea.)	VL-CBR-2022	6" ATX to EPIC power cable	3.946	0.289	20
J15	SATA 0	Standard SATA	VL-CBR-0701 or VL-CBR-0702; VL-CBR-0401	500mm (19.75") 7-pin, straight-to-straight SATA data, friction or mechanical latching; ATX to SATA power adapter	4.248	4.265	34
J16	USB 0	Standard USB Type A	—	—	4.098	4.667	34
J17	USB 2	Standard USB Type A	—	—	4.098	5.387	34
J19	MiniBlade	(MiniBlade)	(VL-F23 Series)	—	—	—	41
J20	LVDS	Molex 51146-2000 (housing), Molex 50641-8041 (pins)	VL-CBR-2010, or VL-CBR-2011, or VL-CBR-2012	18-bit TFT FPD using 20-pin Hirose, or 18-bit TFT FPD using 20-pin JAE, or 24-bit TFT FPD using 20-pin Hirose	1.501	0.062	27
J21	SO-DIMM	(DDR3 RAM)	—	—	—	—	22
J22	SPX	FCI 89361-714LF	VL-CBR-1401 or VL-CBR-1402	2mm 14-pin IDC, 2 or 4 SPX device cable	0.401	6.135	42
J23	eUSB	(eUSB)	(VL-F15 Series)	—	1.927	5.712	35

1. The PCB Origin is the mounting hole to the lower left. 2. Pin A1. 3. Pins J18 and J24 are for factory use only.

CONNECTOR LOCATIONS – VL-CBR-5009

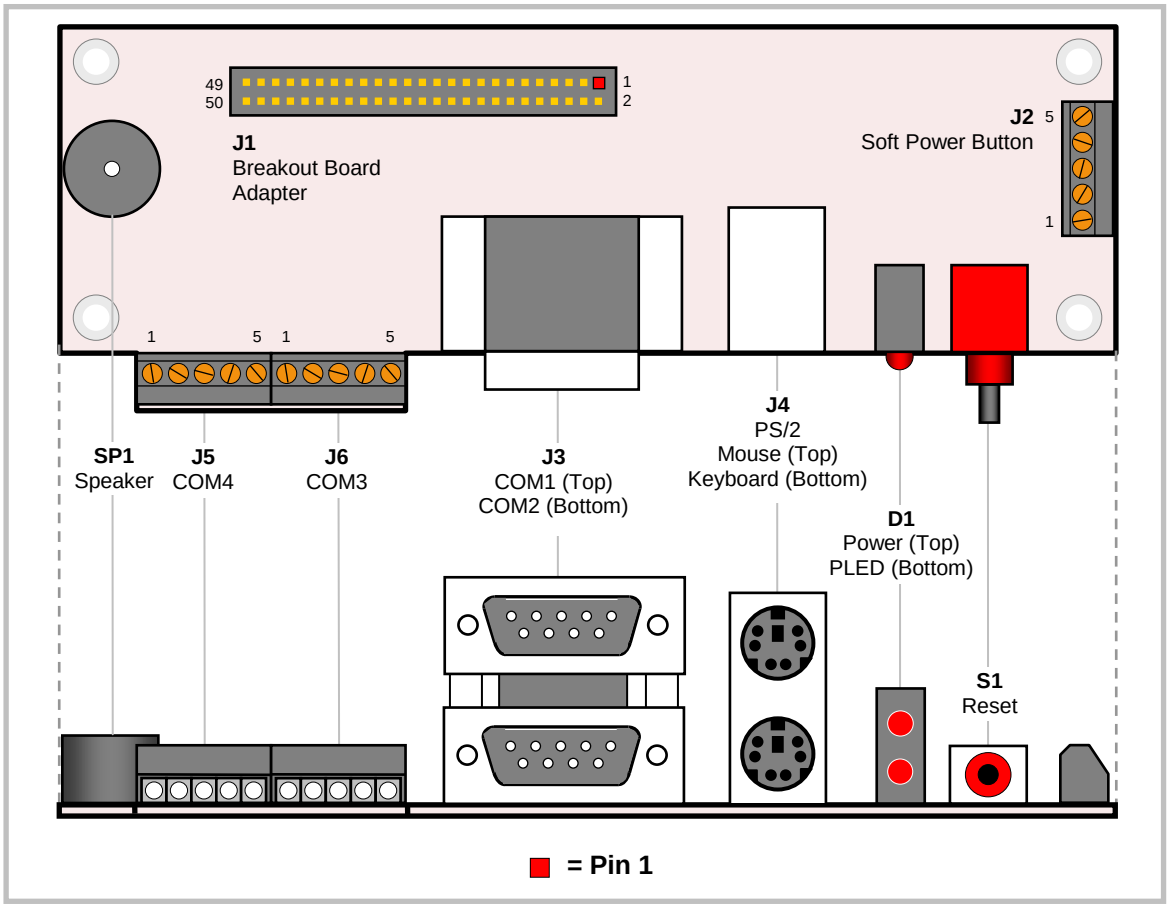

Figure 8. VL-CBR-5009 Connector Locations

VL-CBR-5009 CONNECTOR FUNCTIONS

Table 2: VL-CBR-5009 Connector Functions and Interface Cables

Connector / Component	Function	Part Number	Description
D1	Power and Programmable LEDs	Dialight 552-0211	LEDx2 T1 3/4 PC Mount Red/Red
J1	High Density Connector	FCI 98414-F06-50U	2mm, 50 pins, keyed, latching header
J2	Soft Power Button Input	Conta-Clip 10250.4	5 pin screw terminal
J3	COM1, COM2	Kycon K42-E9P/P-A4N	Dual stacked DB-9 male
J4	PS/2 Keyboard and Mouse	Kycon KMDG-6S/6S-S4N	Dual stacked PS/2 female
J5	COM4	Conta-Clip 10250.4	5 pin screw terminal
J6	COM3	Conta-Clip 10250.4	5 pin screw terminal
S1	Reset Button	E-Switch 800SP9B7M6RE	Right angle momentary switch
SP1	Speaker	Challenge Electronics DBX05	Miniature PC speaker

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION

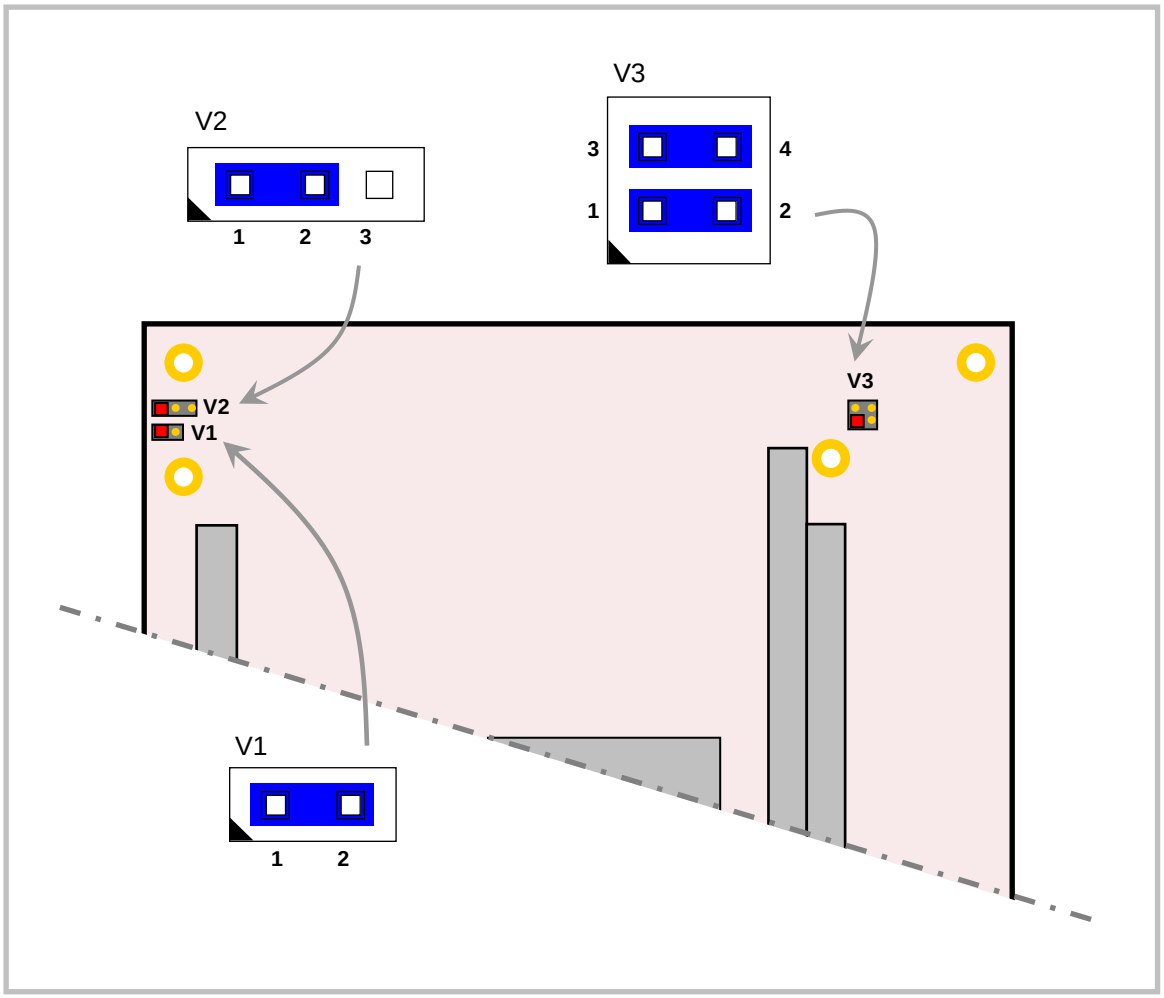

Figure 9. Jumper Block Locations

JUMPER SUMMARY

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**System BIOS Selector** In – Secondary BIOS selected Out – Primary BIOS selected The system BIOS is field-upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/komodosupport.asp for more information.	Out	23
V2[1-2-3]	**CMOS RAM and Real Time Clock Erase** [1-2] In – Normal [2-3] In – Erase CMOS RAM and Real-Time Clock	V2[1-2] In	22
V3[1-2]	**COM3 Rx End-point Termination** In – 120 Ohm termination active Out – No termination Places terminating resistor across COM3 RS-485 TXRX+/TXRX- or RS-422 RX+/RX- differential pair.	In	37
V3[3-4]	**COM4 Rx End-point Termination** In – 120 Ohm termination active Out – No termination Places terminating resistor across COM4 RS-485 TXRX+/TXRX- or RS-422 RX+/RX- differential pair.	In	37

Power Supply

Power Connectors

Main power is applied to the VL-EPICs-36 through an EPIC-style 10-pin polarized connector at location J14.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5VDC pins and all ground pins to prevent excess voltage drop.

Table 4: Main Power Connector Pinout

J14 Pin	Signal Name	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	+12VDC	Power Input
5	+3.3VDC	Power Input
6	NC	Not Connected
7	+5VDC	Power Input
8	+5VDC	Power Input
9	-12VDC	Power Input
10	GND	Ground

Note: The +3.3VDC, +12VDC and -12VDC inputs are required only for expansion modules that require these voltages.

Power Requirements

The VL-EPICs-36 requires +5 volts (±5%) for proper operation. The higher voltages required for the RS-232 ports are generated as needed on-board. Low-voltage supply circuits provide the many power rails required by the CPU and other on-board devices.

The exact power requirement of the VL-EPICs-36 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, driving long RS-232 lines at high speed can increase power demand, and USB devices can draw considerable power depending on the device.

POWER DELIVERY CONSIDERATIONS

The VL-EPICs-36 draws up to 27.5W (5.5A) as measured on a typical time averaging ammeter. The board can experience large, short-term current transients during operation, so care must be taken to provide robust power to the board. A good power delivery method eliminates such problems as voltage drop and lead inductance. Using the VersaLogic approved power supply (VL-PS200-ATX) and power cable (VL-CBR-2022) will ensure high quality power delivery to the board. Customers who design their own power delivery methods should take into consideration the guidelines below to ensure good power connections.

Also note that the 5V @ 4.8A (model S) or 3.2A (model E) typical operating current does not include any off-board power usage that may be fed through the VL-EPICs-36 power connector. PC/104 boards on the expansion site and USB devices plugged into the board will source additional 5V power through the VL- EPICs-36 power connector.

- Do not use wire smaller than 18 AWG. Use high quality UL 1007 compliant stranded wire.
- The length of the wire should not exceed 18".
- Avoid using any additional connectors in the power delivery system.
- The power and ground leads should be twisted together, or as close together as possible to reduce lead inductance.
- A separate conductor must be used for each of the power pins.
- All 5V pins and all ground pins must be independently connected between the power source and the power connector.
- Implement the remote sense feature on your power supply if it has one. Connect the remote sense lines in tandem with one of the power connector 5V and ground pins. This is done at the connector to compensate for losses in the power wires.

Use a high quality power supply that can supply a stable voltage while reacting to widely varying current draws.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 2.0V, contact the factory for a replacement (part number HB3/0-1). The life expectancy under normal use is approximately 10 years.

CPU

The Intel Core 2 Duo processor combines fast performance, using Intel's 45nm technology, with advanced power savings features. The P8400 model used on the VL-EPICs-36 has a maximum clock rate of 2.27 GHz and a front side bus speed of 1066 MHz, and features 3 MB of L2 cache. For more CPU information see the VL-EPICs-36 support page. The chipset features DDR3 SDRAM support, integrated LVDS, USB 2.0, SATA, and PCI Express, among other interfaces.

System RAM

MEMORY

The VL-EPICs-36 has one DDR3 SO-DIMM socket with the following characteristics:

- Storage Capacity — Up to 4 GB
- Voltage — 1.5V
- Type — DDR3 – VersaLogic VL-MM7 Series modules
  SSDDR3 – VL-MF7 Series modules; 1 GB or 2 GB RAM plus 8 GB SATA flash

SSDDR3 DUAL FUNCTION MEMORY AND SOLID STATE DRIVE

The VersaLogic VL-MF7 Series modules provide 1 or 2 GB of RAM plus 8 GB of flash storage. The solid state drive (SSD) can function as a bootable SATA drive or secondary storage device without claiming either of the SATA channels at connectors J10 or J15.

CMOS RAM

CLEARING CMOS RAM

You can move the V2 jumper to position [2-3] for a minimum of three seconds to erase the contents of the CMOS RAM and the Real-Time Clock. When clearing CMOS RAM:

1. Power off the VL-EPICs-36.
2. Install the jumper on V2[2-3] and leave it for four seconds.
3. Move the jumper to back to V2[1-2].
4. Power on the VL-EPICs-36.

CMOS Setup Defaults

The VL-EPICs-36 permits users to modify CMOS Setup defaults. This allows the system to boot up with user-defined settings from cleared or corrupted CMOS RAM, battery failure or battery-less operation. All CMOS setup defaults can be changed, except the time and date. CMOS Setup defaults can be updated with the BIOS Update Utility. See the General BIOS Information page for details.

Warning! If CMOS Setup default settings make the system unbootable and prevent the user from entering CMOS Setup, the system can be recovered by switching to the backup BIOS.

DEFAULT CMOS RAM SETUP VALUES

After CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

PRIMARY AND BACKUP BIOS

The Primary system BIOS is field upgradeable using the BIOS upgrade utility (see the VL-EPICs-36 Support Page for more information). Jumper VN[1-2] controls whether the system uses the Primary or Backup BIOS. By default the Primary BIOS is selected (jumper removed).

Real Time Clock

The VL-EPICs-36 features a year 2000-compliant, battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the Delete key during the early boot cycle) can be used to set the time and date of the real time clock.

Fan/Tachometer Monitor

The Super I/O chip on the VL-EPICs-36 contains a hardware monitor which includes a 16-bit fan tachometer register that can be read to obtain the speed of the fan on the VL-EPICs-36. When one byte of the 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second. The value FFFFh indicates that the fan is not spinning. For more information see the SMSC SCH3114 Super I/O Chip Datasheet.

FAN TACHOMETER READ CODE EXAMPLE

```
#include <stdio.h>
#include <conio.h>
#include <stdlib.h>
#include <graph.h>
#include <dos.h>

//Definitions
#define TRUE            1
#define FALSE           0
#define ESC             27
#define SIOINDEX        0x2E
#define SIODATA         0x2F
#define FANTACHREG      0x28
#define RLSREG          0x40
#define RTOFFSET        0X70
#define START           0x01

void main ()
{
  int baseIOHigh;
  int baseIOLow;
  int FTraw;
  int Bindex;
  int Bdata;
  double fanRPM;
  char keypressed = 0;

  _clearscreen( _GCLEARSCREEN );
  _settextposition(2,1);
  printf( "FANTACH DEMO...(press ESC to quit).\n" );

  /*        Set SIO Hardware Monitor IRQ and read in the HWM base address...     */
  outp( SIOINDEX, 0x55 );                  //Enter SIO config mode.
  outp( SIOINDEX, 0x07 );                  //Point to Logical Device Config reg.
  outp( SIODATA, 0x0A );                   //Select SMSC Runtime reg.
  outp( SIOINDEX, 0x60 );                  //Index High Byte of Runtime reg base address.
  baseIOHigh = inp( SIODATA );             //Read High Byte.
  outp( SIOINDEX, 0x61 );                  //Index Low Byte of Runtime reg base address.
  baseIOLow = inp( SIODATA ) + RTOFFSET;   //Read Low Byte and add offset to runtime reg base.
  outp( SIOINDEX, 0xAA );                  //Exit SIO Config mode
  Bindex = (baseIOHigh << 8) + baseIOLow;  //convert high and low bytes to 16-bit address.
  Bdata = Bindex + 1;

  /*        Start Hardware Monitoring...                                         */
  outp( Bindex, RLSREG );                  //Index Ready, Lock, Start Reg.
  outp( Bdata, inp( Bdata ) | START );     //Set bit 0 to start.
```

```
  while (keypressed != ESC)
  {
    if (kbhit())
    {
      keypressed = getch();
    }

    /*        Read FanTach1 LSB first, latches MSB.                              */
    outp( Bindex, FANTACHREG );            //Fantach 1 LSB
    FTraw = inp( Bdata );
    outp( Bindex, FANTACHREG + 1 );        //Fantach 1 MSB
    FTraw += inp( Bdata ) << 8;

    /* FTraw now contains the number of 90KHz pulses it took to find 5 tach edges.
       (5 edges = 2 tach pulses = 1 revolution)                                   */

    /*        Convert Raw to RPMs...
              RPM = 1 / (FTraw * 11.11uS / 2) * 60                               */
    fanRPM = FTraw * 0.00001111;
    fanRPM /= 2;
    fanRPM = 1/fanRPM;
    _settextposition(4,1);
    if ( fanRPM > 0 )
    {
      printf ( "FanTach 1: %5.0fRPMs        \n",fanRPM*60 );
      delay(100);
    }
    else
    {
      printf ( "FanTach 1: Stalled! \n" );
      delay(100);
    }
  }

  exit ( 0 );
}
```

Video Output (J1 SVGA, J20 LVDS)

An on-board video controller integrated into the chipset provides high performance video output for the VL-EPICs-36. The controller supports dual, simultaneous, independent video output.

CONFIGURATION

The video interface uses PCI interrupt INTA#. CMOS Setup is used to select the IRQ line routed to INTA#.

The VL-EPICs-36 uses shared memory architecture. This allows the video controller to use variable amounts of system DRAM for video RAM, up to 512 MB. The amount of RAM used for video is set with a CMOS Setup option.

The VL-EPICs-36 supports two types of video output, SVGA and LVDS flat panel display, which can be output simultaneously.

SVGA OUTPUT CONNECTOR (J1)

Adapter cable VL-CBR-1201 is available to translate the J1 connector into a standard 15-pin D-Sub SVGA connector. This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 5: Video Output Pinout

J1 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	RED	Red video	1
3	GND	Ground	7
4	GREEN	Green video	2
5	GND	Ground	8
6	BLU	Blue video	3
7	GND	Ground	5
8	HSYNC	Horizontal sync	13
9	GND	Ground	10
10	VSYNC	Vertical sync	14
11	CRT_SCL	DDC data clock line	15
12	CRT_SDA	DDC serial data line	12

LVDS Flat Panel Display Connector (J20)

The integrated LVDS flat panel display interface in the VL-EPICs-36 is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the four differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 112 MHz.

CMOS Setup provides several options for standard LVDS flat panel types. If these options do not match the requirements of the panel you are attempting to use, contact Support@VersaLogic.com for a custom video BIOS.

The 3.3V power provided to pins 19 and 20 of J20 is protected by a 1 Amp fuse.

Table 6: LVDS Flat Panel Display Pinout

J20 Pin	Signal Name	Function
1	GND	Ground
2	NC	Not Connected
3	LVDSA3	Diff. Data (+)
4	LVDSA3#	Diff. Data 3 (–)
5	GND	Ground
6	LVDSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (–)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (–)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (–)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (–)
17	GND	Ground
18	GND	Ground
19	+3.3V	Protected Power Supply
20	+3.3V	Protected Power Supply

COMPATIBLE LVDS PANEL DISPLAYS

The following flat panel displays are reported to work properly with the integrated graphics video controller chip used on the VL-EPICs-36.

Table 7: Compatible Flat Panel Displays

Manufacturer	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx141X01 series	14.1”	1024 x 768 18-bit	LVDS	TFT
Sharp	LQ121S1LG411	12.1”	800 x 600 18-bit	LVDS	TFT

CONSOLE REDIRECTION

The VL-EPICs-36 can be operated without using the onboard video output by redirecting the console to a serial communications port. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

Console redirection settings are configured on the Features tab of the CMOS Setup. The default setting (On Remote User Detect) causes the console not be redirected to the serial port unless a signal (a Ctrl-C character) is detected from the terminal. Console redirection can also be set to Always or Never.

Notes on console redirection:

- When console redirection is enabled, you can access CMOS Setup by typing Ctrl-C.
- The decision to redirect the console is made early in BIOS execution and cannot be changed later.
- The redirected console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control.

Null Modem

The following diagram illustrates a typical DB9 to DB9 RS-232 null modem adapter.

```
System 1     <-->  System 2
Name  Pin          Pin   Name
-----------------------------------
TX    3      <-->  2     RX
RX    2      <-->  3     TX
RTS   7      <-->  1     DCD
CTS   8
DSR   6      <-->  4     DTR
DCD   1      <-->  7     RTS
                   8     CTS
DTR   4      <-->  6     DSR
```

Pins 7 and 8 are shorted together on each connector. Unlisted pins have no connection.

PCI Express / SUMIT Connectors (J2-J3)

The SUMIT A and B connectors (J3 and J2, respectively) provide a subset of the PCI Express functionality, as shown in Table 8 and Table 9. See the SUMIT Specification for a complete description of the SUMIT interface.

Table 8: SUMIT A Connector Pinout

J3 Pin	Signal Name	Function	J3 Pin	Signal Name	Function
1	+5VSB	+5V power	2	+12V	+12V power
3	3.3V	+3.3V power	4	SMB/I2C_DATA	SMBus data
5	3.3V	+3.3V power	6	SMB/I2C_CLK	SMBus clock
7	EXPCD_REQ#	Express card request	8	SMB/I2C_ALERT#	SMBus interrupt line in
9	EXPCD_PRSNT#	Express card present	10	SPI/uWire_DO	SPI data out from master
11	USB_OC#0/1	USB overcurrent flag 0/1	12	SPI/uWire_DI	SPI data in to master
13	USB_OC#2/3	USB overcurrent flag 2/3	14	SPI/uWire_CLK	SPI clock
15	+5V	+5V power	16	SPI/uWire_CS0#	SPI chip select 0
17	USB3+	USB3 data +	18	SPI/uWire_CS1#	SPI chip select 1
19	USB3-	USB3 data –	20	Reserved	Do not use
21	+5V	+5V power	22	LPC_DRQ	LPC DMA request
23	USB2+	USB2 data +	24	LPC_AD0	LPC line 0
25	USB2-	USB2 data –	26	LPC_AD1	LPC line 1
27	+5V	+5V power	28	LPC_AD2	LPC line 2
29	USB1+	USB1 data +	30	LPC_AD3	LPC line 3
31	USB1-	USB1 data –	32	LPC_FRAME#	LPC frame
33	+5V	+5V power	34	SERIRQ#	Serial IRQ legacy
35	USB0+	USB0 data +	36	LPC_PRSNT#/GND	LPC card present
37	USB0-	USB0 data –	38	CLK_33MHz	33 MHz clock out
39	GND	Ground	40	GND	Ground
41	A_PETp0	Link A, lane 0 transmit +	42	A_PERp0	Link A, lane 0 receive +
43	A_PETn0	Link A, lane 0 transmit –	44	A_PERn0	Link A, lane 0 receive –
45	GND	Ground	46	APRSNT#/GND	Link A card present
47	PERST#	Reset	48	A_CLKp	Link A clock +
49	WAKE#	Wake on event signal	50	A_CLKn	Link A clock –
51	+5V	+5V power	52	GND	Ground

Table 9: SUMIT B Connector Pinout

J2 Pin	Signal Name	Function	J2 Pin	Signal Name	Function
1	GND	Ground	2	GND	Ground
3	B_PETp0	Link B, lane 0 transmit +	4	B_PERp0	Link B, lane 0 receive +
5	B_PETn0	Link B, lane 0 transmit –	6	B_PERn0	Link B, lane 0 receive –
7	GND	Ground	8	BPRSNT#/GND	Link B present
9	C_CLKp	Link C clock +	10	B_CLKp	Link B clock +
11	C_CLKn	Link C clock –	12	B_CLKn	Link B clock –
13	CPRSNT#/GND	Link C present	14	GND	Ground
15	C_PETp0	PCIe link C, lane 0 transmit +	16	C_PERp0	PCIe link C, lane 0 receive +
17	C_PETn0	PCIe link C, lane 0 transmit –	18	C_PERn0	PCIe link C, lane 0 receive –
19	GND	Ground	20	GND	Ground
21	C_PETp1	PCIe link C, lane 1 transmit +	22	C_PRTp1	PCIe link C, lane 1 transmit +
23	C_PETn1	PCIe link C, lane 1 transmit –	24	C_PERn1	PCIe link C, lane 1 transmit –
25	GND	Ground	26	GND	Ground
27	C_PETp2	PCIe link C, lane 2 transmit +	28	C_PERp2	PCIe link C, lane 2 transmit +
29	C_PETn2	PCIe link C, lane 2 transmit –	30	C_PERn2	PCIe link C, lane 2 transmit –
31	GND	Ground	32	GND	Ground
33	C_PETp3	PCIe link C, lane 3 transmit +	34	C_PERp3	PCIe link C, lane 3 transmit +
35	C_PETn3	PCIe link C, lane 3 transmit –	36	C_PERn3	PCIe link C, lane 3 transmit –
37	GND	Ground	38	GND	Ground
39	PERST#	Reset	40	WAKE#	Wake on event signal
41	Reserved	Should *not* be used.	42	Reserved	Do not use
43	+5V	+5V power	44	Reserved	Do not use
45	+5V	+5V power	46	3.3V	+3.3V power
47	+5V	+5V power	48	3.3V	+3.3V power
49	+5V	+5V power	50	3.3V	+3.3V power
51	+5V	+5V power	52	+5VSB	+5V power

Ethernet (Interface J5, LED J4)

The VL-EPICs-36 features an on-board Intel 82574IT Gigabit Ethernet controller, which provides a standard IEEE 802.3 Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications. The 82574IT provides one PCIe lane with sufficient bandwidth to support a 2.5 gigabits per second (GB/s) transfer rate.

BIOS CONFIGURATION

The Ethernet interface (J5) uses PCI interrupt INTB#. CMOS Setup screen is used to select the IRQ line routed to each PCI interrupt line.

ETHERNET CONNECTOR (J5)

A board-mounted RJ-45 connector is provided to make connection with a Category 5 or 6 Ethernet cable. The 82574IT Ethernet controller auto-negotiates connection speed. The interface uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

ETHERNET LED (J4)

Connector J4 provides an on-board Ethernet LED interface. The 3.3V power supplied to this connector is protected by a 1 Amp fuse.

Table 10: Ethernet LED Connector Pinout

J4 Pin	Signal Name	Function
1	+3.3V	Protected Power Supply
2	YEL	Yellow LED
3	ORN	Orange LED
4	GRN	Green LED
5	+3.3V	Protected Power Supply
6	NC	(not connected)
7	NC	(not connected)
8	NC	(not connected)
9	GND	Ground
10	NC	(not connected)

Audio (J6)

The audio interface on the VL-EPICs-36 is implemented using the IDT 92HD75B Audio Codec. This interface is compatible with Intel's High Definition (HD) Audio Interface and is Microsoft WLP 3/4 premium logo compliant, as defined in WLP 3.09. Drivers are available for most Windows-based operating systems. To obtain the most current versions, consult the VL-EPICs-36 support page.

J6 provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

SOFTWARE CONFIGURATION

The audio interface uses PCI interrupt INTA#. CMOS Setup is used to select the IRQ line routed to INTA#.

The audio controller can be disabled in CMOS Setup.

Table 11: Audio Connector Pinout

J6 Pin	Signal Name	Function
1	AUDOUTR	Audio Line-Out Right
2	GND	Ground
3	AUDOUTL	Audio Line-Out Left
4	GND	Ground
5	AUDINR	Audio Line-In Right
6	GND	Ground
7	AUDINL	Audio Line-In Left
8	GND	Ground

PC/104 (ISA) Expansion Bus (J7-J8)

VL-EPICs-36 has limited support of the PC/104 bus. Most PC/104 cards will work, but be sure to check the requirements of your PC/104 card against the list below.

PC/104 I/O SUPPORT

The ISA I/O ranges listed below are supported. The I/O ranges allocated to COM ports 1-4 are available to ISA when the on-board COM port function is disabled in CMOS Setup.

019h – 01Eh	03Ah – 03Bh	067h – 070h	0B6h – 0B7h	210h – 3BFh
022h – 023h	03Eh – 03Fh	078h – 07Fh	0BAh – 0BBh	3E0h – 4CFh
026h – 027h	043h – 04Dh	0A2h – 0A3h	0BEh – 0BFh	4D2h – 4FFh
02Ah – 02Bh	053h – 05Fh	0A6h – 0A7h	0D2h – 0DDh	580h – BFFh
032h – 033h	063h	0AAh – 0ABh	0E0h – 0EFh	D00h
036h – 037h	065h	0AEh – 0AFh	0F1h – 207h	

Available base I/O addresses for COM ports are: 220h, 228h, 238h, 338h, 3F8h, 2F8h, 3E8h, and 2E8h.

PC/104 MEMORY SUPPORT

Memory ranges supported:

- A0000h – B7FFFh
- D0000h – DFFFFh

IRQ SUPPORT

The following IRQs are available on the PC/104 bus:

- IRQ 3, IRQ 4, IRQ5, and IRQ 10

Each of the four IRQs must be enabled in CMOS Setup before they can be used on the ISA bus. Because ISA IRQ sharing is not supported, make sure that any IRQ channel used for an ISA device is not used elsewhere. For example, if ISA IRQ 4 is enabled, you must use a different IRQ for COM1.

DMA SUPPORT

The current revision of the board does not support PC/104 DMA.

SATA Interface (J10, J15)

The VL-EPICs-36 provides two serial ATA (SATA) ports, which communicate at a rate of up to 3.0 GB/s (SATA 2). The SATA connectors at locations J10 and J15 are standard 7-pin straight SATA connectors with friction latching. Power to SATA drives is supplied by the ATX power supply. Note that the standard SATA drive power connector is different than the common 4-pin Molex connector used on IDE drives. Most current ATX power supplies provide SATA connectors, and many SATA drives provide both types of power connectors. If the power supply you are using does not provide SATA connectors, adapters are available.

Table 12: SATA Port Pinout

J10 or J15 Pin	Signal Name	Function
1	GND	Ground
2	TX+	Transmit +
3	TX-	Transmit -
4	GND	Ground
5	RX-	Receive -
6	RX+	Receive +
7	GND	Ground

USB Interface (Multiple Connectors)

The VL-EPICs-36 includes ten USB ports, as shown below.

Table 13: USB Port Locations

Port	Connector	Type
USB0	J16	USB Type A
USB1	J11	USB Type A
USB2	J17	USB Type A
USB3	J12	USB Type A
USB4	J3	SUMIT A (USB0)
USB5	J3	SUMIT A (USB1)
USB6	J3	SUMIT A (USB2)
USB7	J3	SUMIT A (USB3)
USB8	J19	MiniBlade
USB9	J23	eUSB

The USB interface on the VL-EPICs-36 is UHCI (Universal Host Controller Interface) and EHCI (Enhanced Host Controller Interface) compatible, which provides a common industry software/hardware interface.

BIOS CONFIGURATION

The USB controller use a number of PCI interrupts. CMOS Setup is used to select the IRQ line routed to each PCI interrupt line.

EUSB INTERFACE (J23)

The VL-EPICs-36 includes one eUSB port, as shown below. The VersaLogic VL-F15 Series of eUSB SSD modules are available in sizes of 2 MB or 4 MB. Contact VersaLogic Sales to order.

Table 14: eUSB Port Locations

J23 Pin	Signal Name	Function
1	+5V	Protected Power Supply
2	NC	Not connected
3	D-	Data –
4	NC	Not connected
5	D+	Data +
6	NC	Not connected
7	GND	Ground
8	NC	Not connected
9	Key	Physical key
10	LED	SSD LED

Main I/O Connector (J13)

The 50-pin I/O connector (J13) incorporates the COM ports, PS/2 keyboard and mouse, programmable LED, reset button, soft power reset, and speaker interfaces. Table 15 illustrates the function of each pin. The 5.0V power lines provided to J13 are protected by a 1 Amp fuse.

Table 15: I/O Connector Pinout

J13 Pin	VL-CBR-5009 Connector	Pin	Signal	
1	**COM1**	1	Data Carrier Detect	
2	**J3**	6	Data Set Ready	
3	Top DB9	2	Receive Data	
4		7	Request to Send	
5		3	Transmit Data	
6		8	Clear to Send	
7		4	Data Terminal Ready	
8		9	Ring Indicator	
9		5	Ground	
10	**COM2**	10	Data Carrier Detect	
11	**J3**	15	Data Set Ready	
12	Bottom DB9	11	Receive Data	
13		16	Request to Send	
14		12	Transmit Data	
15		17	Clear to Send	
16		13	Data Terminal Ready	
17		18	Ring Indicator	
18		14	Ground	
	COM3		**RS-232**	**RS-232/422/485**
19	**J6**	1	Ground	Ground
20		5	RTS	TxD+
21		4	TXD	TxD-
22		–	Ground	Ground
23		2	RXD	RxD-
24		3	CTS	RxD+
25		–	Ground	Ground

J13 Pin	VL-CBR-5009 Connector	Pin	Signal	
	COM4		**RS-232**	**RS-232/422/485**
26	**J5**	1	Ground	Ground
27		5	RTS	TxD+
28		4	TXD	TxD-
29		–	Ground	Ground
30		2	RXD	RxD-
31		3	CTS	RxD+
32		–	Ground	Ground
33	**Mouse**	4	+5.0V (Protected)	
34	**J4**	1	Mouse Data	
35	Top	3	Ground	
36		5	Mouse Clock	
37	**PBRESET**	1	Pushbutton Reset	
38	**S1**	2	Ground	
39	**(Reserved)**	–	Ground	
40		–	Not connected	
41		–	Ground	
42		–	Not connected	
43	**Keyboard**	4	+5.0V (Protected)	
44	**J4**	1	Keyboard Data	
45	Bottom	3	Ground	
46		5	Keyboard Clock	
47	**PLED**	1	+5.0V (Protected)	
48	**D1**	2	Programmable LED	
49	**Speaker**	1	+5.0V (Protected)	
50	**SP1**	2	Speaker Drive	

Serial Ports

The VL-EPICs-36 features four on-board 16550-based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2K baud) serial ports. IRQ lines are chosen in CMOS Setup. COM ports can share interrupts with other COM ports, but not with other devices.

COM3 and COM4 can be operated in RS-232 4-wire, RS-422 or RS-485 modes. Additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 460k baud. IRQ lines are chosen in CMOS Setup.

Each COM port can be independently enabled, disabled, or assigned a different I/O base address in CMOS Setup.

COM Port Configuration

There are no configuration jumpers for COM1 and COM2 since they only operate in RS-232 mode. Use CMOS Setup to select between RS-232 4-wire, RS-422, and RS485 operating modes for COM3 and COM4.

Jumper V3[1-2] is used to enable the RS-422/485 termination resistor for COM3. Jumper V3[3-4] is used to enable the RS-422/485 termination resistor for COM4. The termination resistor should be enabled for RS-422 and the RS-485 endpoint station. It should be disabled for RS-232 and the RS-485 intermediate station.

If RS-485 mode is used, the differential twisted pair (TxD+/RxD+ and TxD-/RxD-) is formed by connecting both transmit and receive pairs together. For example, on VL-CBR-5009 connectors J6 and J5, the TxD+/RxD+ signal is formed by connecting pins 3 and 5, and the TxD-/RxD- signal is formed by connecting pins 2 and 4.

RS-485 Mode Line Driver Control

The VL-EPICs-36 features automatic RS-485 direction control for COM3 and COM4. The purpose of this function is to save the effort of RS-485 direction control in software. The direction control signal RTS is used to tri-state the transmitter when no other data is available, so that other nodes can use the shared lines.

RS-485 direction control is set using the Serial Port Mode parameters in CMOS Setup. To enable manual direction control, set the COM port mode to RS485 ManuFC; to enable auto direction control, set the parameter to RS485 AutoFC. Manual direction control is configured by asserting the RTS handshake line. Asserting the RTS handshake line puts the RS-485 port in transmit mode; de-asserting the line puts it in receive mode.

SERIAL PORT CONNECTORS

The pinouts of the DB9M connectors apply to the serial connectors on the VersaLogic breakout board VL-CBR-5009. These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 16: COM1-2 Pinout – VL-CBR-5009 Connector J3

COM1	COM2	
Top DB9 J3 Pin	Bottom DB9 J3 Pin	RS-232
1	10	DCD
2	11	RXD*
3	12	TXD*
4	13	DTR
5	14	Ground
6	15	DSR
7	16	RTS
8	17	CTS
9	18	RI

Table 17: COM3-4 Pinout – VL-CBR-5009 Connectors J5-6

COM3	COM4			
J6 Pin	J5 Pin	RS-232	RS-422	RS-485
1	1	Ground	Ground	Ground
2	2	RXD	RxD-	RxD-
3	3	CTS	RxD+	RxD+
4	4	TXD	TxD-	TxD-
5	5	RTS	TxD+	TxD+

PS/2 Mouse and Keyboard Interface

A standard PS/2 keyboard and mouse interface is accessible through connector J4 of the VersaLogic breakout board, VL-CBR-5009. The breakout board is connected to connector J13 of the VL-EPICs-36. The 5V power provided to the keyboard and mouse is protected by a 1 Amp fuse.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 18: PS/2 Mouse and Keyboard Pinout

VL-CBR-5009 J4 Top Pin	Signal	Description
1	MSDATA	Mouse Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	MSCLK	Mouse Clock
6	–	No Connection
VL-CBR-5009 J4 Bottom Pin	**Signal**	**Description**
1	KBDATA	Keyboard Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	KBCLK	Keyboard Clock
6	–	No Connection

Push-Button Reset

Connector J13 includes an input for a push-button reset switch. Shorting J13, pin 37 to ground causes the VL-EPICs-36 to reboot.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the VL-CBR-5009 breakout board.

Programmable and Power LEDs

Connector J13 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J13 pin 48; connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the VL-CBR-5009 breakout board.

To turn the LED on and off, set or clear bit D7 in I/O port 1D0h (or 1E0h). When changing the register, make sure not to alter the values of the other bits.

The following code examples show how to turn the LED on and off.

LED On

```
MOV    DX,1D0H
IN     AL,DX
OR     AL,80H
OUT    DX,AL
```

LED Off

```
MOV    DX,1D0H
IN     AL,DX
AND    AL,7FH
OUT    DX,AL
```

Note The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

Internal Speaker

A miniature 8 ohm speaker can be connected between J13 pin 50 (Speaker Drive) and pin 49 (+5.0V). A speaker is provided on the VL-CBR-5009 breakout board.

MiniBlade Socket (J19)

The MiniBlade socket on the VL-EPICs-36 incorporates one PCIe x1 lane, one USB port, and one SATA port. See the MiniBlade Specification for more information. The VL-F23 series of MiniBlade devices are available from VersaLogic in sizes of 1 MB, 2 MB, and 4 MB. Contact VersaLogic Sales to order.

Table 19: MiniBlade Socket Pinout

J19 Pin	Signal Name	Function
1	+3VSB	+3V standby power
3	USB3TX+	USB3 transmit+
5	USB3TX-	USB3 transmit-
7	+3.3V	+3.3V power
9	USB3RX-	USB3 receive-
11	USB3RX+	USB3 receive+
13	+3.3V	+3.3V power
15	GND	Ground
17	USB+	USB0 data +
19	USB–	USB0 data –
21	GND	Ground
23	A_PETp0	Link A, lane 0 transmit +
25	A_PETn0	Link A, lane 0 transmit –
27	BLADE_PRSNT#	MiniBlade present
29	A_PERp0	Link A, lane 0 receive +
31	A_PERn0	Link A, lane 0 receive –
33	GND	Ground
35	A_CLKp	Link A clock +
37	A_CLKn	Link A clock –
39	PCIe-PRSNT#	PCIe present

J19 Pin	Signal Name	Function
2	GND	Ground
4	SATA+	SATA transmit +
6	SATA-	SATA transmit –
8	+5V	+5V power
10	PERST#	PERST#
12	BLADE_REQ#	BLADE_REQ#
14	SDIO-D0	SDIO-D0
16	SDIO-D1	SDIO-D1
18	SDIO-D2	SDIO-D2
20	SDIO-D3	SDIO-D3
22	SDIO-D4	SDIO-D4
24	SDIO-D5	SDIO-D5
26	SDIO-D6	SDIO-D6
28	SDIO-D7	SDIO-D7
30	SDIO-DMD	SDIO-DMD
32	SDIO-CLK	SDIO Clock
34	+5V	+5V power
36	SATB–	SATA receive -
38	SATB	SATA receive +
40	GND	Ground

SPX™ Expansion Bus (J22)

Up to four serial peripheral expansion (SPX) devices can be attached to the VL-EPICs-36 at connector JN1 using the VL-CBR-1401 or VL-CBR-1402 cable. The SPX interface provides the standard serial peripheral interface (SPI) signals: SCLK, MISO, and MOSI, as well as four chip selects, SS0# to SS3#, and an interrupt input, SINT#.

The 5.0V power provided to pins 1 and 14 of JN1 is protected by a 1 Amp fuse.

Table 20: SPX Expansion Bus Pinout

J22 Pin	Signal Name	Function
1	V5_0	+5.0V (Protected)
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Serial Data In
5	GND	Ground
6	MOSI	Serial Data Out
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1
10	SS2#	Chip Select 2
11	SS3#	Chip Select 3
12	GND	Ground
13	SINT#	Interrupt Input
14	V5_0	+5.0V (Protected)

SPI is, in its simplest form, a three wire serial bus. One signal is a Clock, driven only by the permanent Master device on-board. The others are Data In and Data Out with respect to the Master. The SPX implementation adds additional features, such as chip selects and an interrupt input to the Master. The Master device initiates all SPI transactions. A slave device responds when its Chip Select is asserted and it receives Clock pulses from the Master.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. Please note that since this clock is divided from a 33 MHz PCI clock, the actual generated frequencies are not discrete integer MHz frequencies. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

VERSALOGIC SPX EXPANSION MODULES

VersaLogic offers a number of SPX modules that provide a variety of standard functions, such as analog input, digital I/O, CANbus controller, and others. These are small boards (1.2" x 3.775") that can mount on the PC/104 stack, using standard PC/104 stand-offs, or up to two feet away from the base board. For more information, contact VersaLogic at Info@VersaLogic.com.

SPI REGISTERS

A set of control and data registers are available for SPI transactions. The following tables describe the SPI control registers (SPICONTROL and SPISTATUS) and data registers (SPIDATA3-0).

SPICONTROL (READ/WRITE) CA8h (or C98h)

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 21: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge
D5-D4	SPILEN	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes. **SPILEN1 SPILEN0 Frame Length** 0 0 8-bit 0 1 16-bit 1 0 24-bit 1 1 32-bit
D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (1DDh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual
D2-D0	SS	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the base board will be directly controlled by these bits when MAN_SS = 1. **SS2 SS1 SS0 Slave Select** 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, J17 pin-8 0 1 0 SPX Slave Select 1, J17 pin-9 0 1 1 SPX Slave Select 2, J17 pin-10 1 0 0 SPX Slave Select 3, J17 pin-11 1 0 1 On-Board A/D Converter Slave Select 1 1 0 On-Board Digital I/O Ch 0-Ch 15 Slave Select 1 1 1 On-Board Digital I/O Ch 16-Ch 31 Slave Select

SPISTATUS (READ/WRITE) CA9h (or C99h)

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 22: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10 **Note:** The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts.
D5-D4	SPICLK	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPIDATA0 (READ/WRITE) CAAh (or C9Ah)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) CABh (or C9Bh)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) CACh (or C9Ch)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) CADh (or C9Dh)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit use the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.

6 Interrupt Configuration

The VL-EPICs-36 has the standard complement of PC-type interrupts. Up to eight IRQ lines can be allocated as needed to PCI devices. There are no interrupt configuration jumpers. All configuration is handled through CMOS Setup.

Table 23: Interrupt Configuration

● = default setting ○ = allowed setting

Source	IRQ															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	●															
Keyboard		●														
Slave PIC			●													
COM1				○	●	○		○								
COM2				●	○	○		○								
COM3				○	○	○		○								
COM4				○	○	○		○								
RTC									●							
Mouse													●			
Math Chip														●		
Pri. IDE															●	
PCI INTA#						○				○	○	●				
PCI INTB#						○				○	○	●				
PCI INTC#						○				○	○	●				
PCI INTD#						○				●	○	○				
PCI INTE#						○				●	○	○				
PCI INTF#						○				●	○	○				
PCI INTG#						○				●	○	○				
PCI INTH#						○				●	○	○				

PCI interrupt routings apply to legacy Programmable Interrupt Controller (PIC) mode. When the OS switches to Advanced PIC (APIC) mode, PCI devices use IRQs beyond IRQ 15.

Table 24: PCI Interrupt Settings

Source	PCI Interrupts							
	INTA#	INTB#	INTC#	INTD#	INTE#	INTF#	INTG#	INTH#
VGA Display	●							
High Definition Audio	●							
PCIe Port 1	●							
PCIe Port 2		●						
USB UHCI Port 1					●			
USB UHCI Port 2						●		
USB UHCI Port 3							●	
USB UHCI Port 4	●							
USB UHCI Port 5		●						
USB UHCI Port 6			●					
USB EHCI Port 1					●			
USB EHCI Port 2			●					
SATA Ports 0, 1 (non-AHCI)		●						
SATA Ports 0, 1, 4, 5 (AHCI)		●						
Sata Ports 4, 5 (non-AHCI)		●						
Intel 82574IT Ethernet		●						

Product Code Register

PRODCODE (Read/Write) CA0h (or C90h)

D7	D6	D5	D4	D3	D2	D1	D0
PLED	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Table 25: Product Code Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J13. 0 = Turns LED on 1 = Turns LED off
D6-D0	PC	**Product Code** — These bits are hard-coded to represent the product type. The VL-EPICs-36 always reads as 0000001. Other codes are reserved for future products. **PC6 PC5 PC4 PC3 PC2 PC1 PC0 Product Code** 0 0 0 0 1 0 0 VL-EPICs-36 These bits are read-only.

Revision Level Register

REVLEV (Read Only) CA1h (or C91h)

D7	D6	D5	D4	D3	D2	D1	D0
RL4	RL3	RL2	RL1	RL0	EXT	CUST	BETA

Table 26: Revision Level Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	RL	**FPGA Revision Level** — These bits are hard-coded to represent the FPGA revision. Contact VersaLogic Support for further information. These bits are read-only.
D2	EXT	**Extended Temperature** — Indicates operating temperature range. 0 = Standard temperature range 1 = Extended temperature range This bit is read-only.
D1	CUSTOM	**Custom Flag –** Indicates whether this is a custom FPGA. 0 = Standard 1 = Custom This bit is read-only.
D0	REV	**Beta Flag** — Indicates whether this is a Beta product. 0 = Standard 1 = Beta This bit is read-only.

Special Control Register

SCR (Read/Write) CA2h (or C92h)

D7	D6	D5	D4	D3	D2	D1	D0
BIOS_JMP	BIOS_OR	BIOS_SEL	Reserved	Reserved	Reserved	Reserved	Reserved

Table 27: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	BIOS_JMP	**System BIOS Selector Jumper Status —** Indicates the status of the system BIOS selector jumper at V1[1-2]. 0 = Jumper installed – backup system BIOS selected 1 = No jumper installed – primary system BIOS selected This bit is read-only.
D6	BIOS_OR	**BIOS Jumper Override —** Overrides the system BIOS selector jumper and selects the BIOS with BIOS_SEL. 0 = No BIOS override 1 = BIOS override
D5	BIOS_SEL	**BIOS Select —** Selects the system BIOS when BIOS_OR is set. 0 = Backup BIOS selected 1 = Primary BIOS selected
D4-D0	Reserved	These bits have no function.

Appendix A – References

CPU *Intel Core 2 Duo*	Intel Core 2 Duo Datasheet
Chipset *Intel GM45*	Mobile Intel 4 Series Chipset Datasheet
Ethernet Controller *Intel 82574IT Ethernet Controller*	Intel 8257IT Datasheet
PC/104 Interface	PC/104 Specification
SUMIT Interface	SUMIT Specification
General PC Documentation *The Programmer's PC Sourcebook*	Amazon.com
General PC Documentation *The Undocumented PC*	Amazon.com