

# MJE18008G, MJF18008G

## SWITCHMODE

### NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE/MJF18008G have an applications specific state-of-the-art die designed for use in 220 V line-operated SWITCHMODE Power supplies and electronic light ballasts.

#### Features

- Improved Efficiency Due to Low Base Drive Requirements:
  - ♦ High and Flat DC Current Gain  $h_{FE}$
  - ♦ Fast Switching
  - ♦ No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot-to-Lot
- Two Package Choices: Standard TO-220 or Isolated TO-220
- MJF18008, Case 221D, is UL Recognized at 3500 V<sub>RMS</sub>: File #E69369
- These Devices are Pb-Free and are RoHS Compliant\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	450	Vdc
Collector-Base Breakdown Voltage	$V_{CES}$	1000	Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current – Continuous	$I_C$	8.0	Adc
Collector Current – Peak (Note 1)	$I_{CM}$	16	Adc
Base Current – Continuous	$I_B$	4.0	Adc
Base Current – Peak (Note 1)	$I_{BM}$	8.0	Adc
RMS Isolation Voltage (Note 2) Test No. 1 Per Figure 22a Test No. 1 Per Figure 22b Test No. 1 Per Figure 22c (for 1 sec, R.H. < 30%, $T_A = 25^\circ\text{C}$ )	$V_{ISOL}$	<b>MJF18008</b> 4500 3500 1500	V
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ MJE18008 MJF18008	$P_D$	125 45	W W/ $^\circ\text{C}$
Derate above $25^\circ\text{C}$ MJE18008 MJF18008		1.0 0.36	
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case MJE18008 MJF18008	$R_{\theta JC}$	1.0 2.78	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

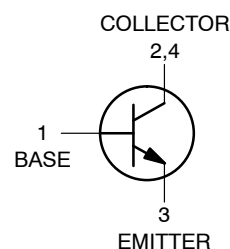
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
2. Proper strike and creepage distance must be provided.



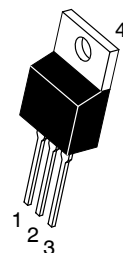
ON Semiconductor®

<http://onsemi.com>

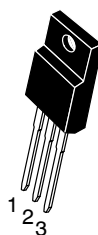
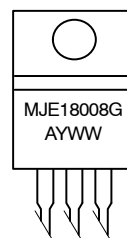
### POWER TRANSISTOR 8.0 AMPERES 1000 VOLTS 45 and 125 WATTS



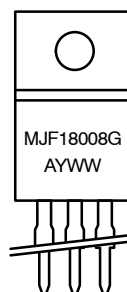
#### MARKING DIAGRAMS



TO-220AB  
CASE 221A-09  
STYLE 1



TO-220 FULLPACK  
CASE 221D  
STYLE 2  
UL RECOGNIZED



G = Pb-Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJE18008G, MJF18008G

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	450	–	–	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	100	μAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CE</sub> , V <sub>EB</sub> = 0)	I <sub>CES</sub>	–	–	100	μAdc
(T <sub>C</sub> = 125°C)		–	–	500	
(V <sub>CE</sub> = 800 V, V <sub>EB</sub> = 0)		–	–	100	
Emitter Cutoff Current (V <sub>EB</sub> = 9.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	100	μAdc

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.2 Adc) (I <sub>C</sub> = 4.5 Adc, I <sub>B</sub> = 0.9 Adc)	V <sub>BE(sat)</sub>	– –	0.82 0.92	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.2 Adc)	V <sub>CE(sat)</sub>	–	0.3	0.6	Vdc
(T <sub>C</sub> = 125°C)		–	0.3	0.65	
(I <sub>C</sub> = 4.5 Adc, I <sub>B</sub> = 0.9 Adc)		–	0.35	0.7	
(T <sub>C</sub> = 125°C)		–	0.4	0.8	
DC Current Gain (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	14	–	34	–
(T <sub>C</sub> = 125°C)		–	28	–	
(I <sub>C</sub> = 4.5 Adc, V <sub>CE</sub> = 1.0 Vdc)		6.0	9.0	–	
(T <sub>C</sub> = 125°C)		5.0	8.0	–	
(I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 1.0 Vdc)		11	15	–	
(T <sub>C</sub> = 125°C)		11	16	–	
(I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 5.0 Vdc)		10	20	–	

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	f <sub>T</sub>	–	13	–	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>ob</sub>	–	100	150	pF
Input Capacitance (V <sub>EB</sub> = 8.0 V)	C <sub>ib</sub>	–	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub> (see Figure 18)	(I <sub>C</sub> = 2.0 Adc I <sub>B1</sub> = 200 mAdc V <sub>CC</sub> = 300 V)	1.0 μs 3.0 μs	(T <sub>C</sub> = 125°C) (T <sub>C</sub> = 125°C)	V <sub>CE(dsat)</sub>	– – – – – – – –
	(I <sub>C</sub> = 5.0 Adc I <sub>B1</sub> = 1.0 Adc V <sub>CC</sub> = 300 V)	1.0 μs 3.0 μs	(T <sub>C</sub> = 125°C) (T <sub>C</sub> = 125°C)		5.5 11.5 3.5 6.5 11.5 14.5 2.4 9.0

### SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn–On Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 0.2 Adc, I <sub>B2</sub> = 1.0 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	– –	200 190	300 –	ns
Turn–Off Time		(T <sub>C</sub> = 125°C)	t <sub>off</sub>	– –	1.2 1.5	2.5 –	μs
Turn–On Time	(I <sub>C</sub> = 4.5 Adc, I <sub>B1</sub> = 0.9 Adc, I <sub>B2</sub> = 2.25 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	– –	100 250	180 –	ns
Turn–Off Time		(T <sub>C</sub> = 125°C)	t <sub>off</sub>	– –	1.6 2.0	2.5 –	μs

### SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 0.2 Adc, I <sub>B2</sub> = 1.0 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	– –	100 120	180 –	ns
Storage Time		(T <sub>C</sub> = 125°C)	t <sub>si</sub>	– –	1.5 1.9	2.75 –	μs
Crossover Time		(T <sub>C</sub> = 125°C)	t <sub>c</sub>	– –	250 230	350 –	ns
Fall Time	(I <sub>C</sub> = 4.5 Adc, I <sub>B1</sub> = 0.9 Adc, I <sub>B2</sub> = 2.25 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	– –	85 135	150 –	ns
Storage Time		(T <sub>C</sub> = 125°C)	t <sub>si</sub>	– –	2.0 2.6	3.2 –	μs
Crossover Time		(T <sub>C</sub> = 125°C)	t <sub>c</sub>	– –	210 250	300 –	ns

- Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
- Proper strike and creepage distance must be provided.

TYPICAL STATIC CHARACTERISTICS

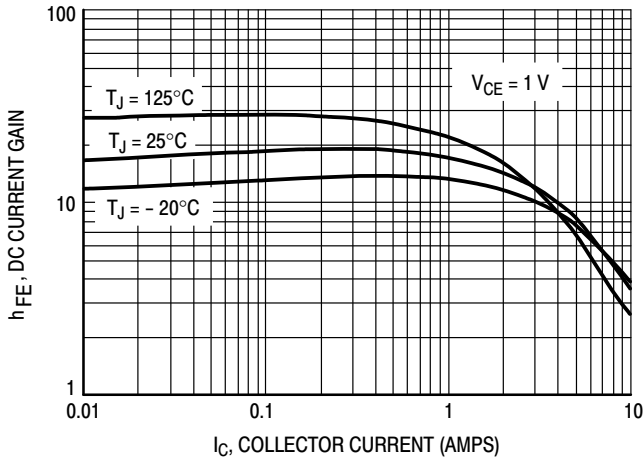


Figure 1. DC Current Gain @ 1 Volt

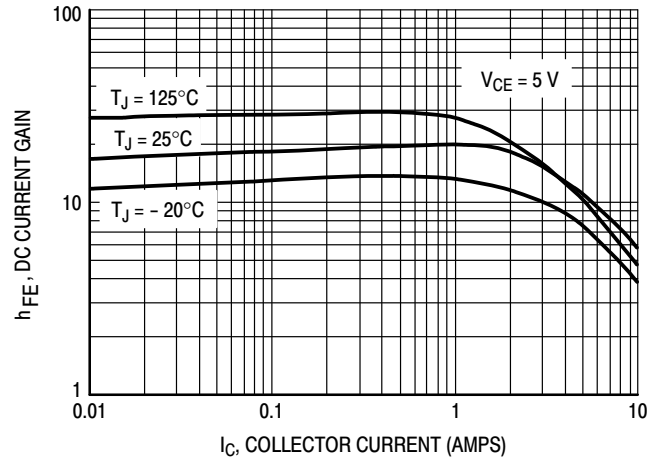


Figure 2. DC Current Gain @ 5 Volts

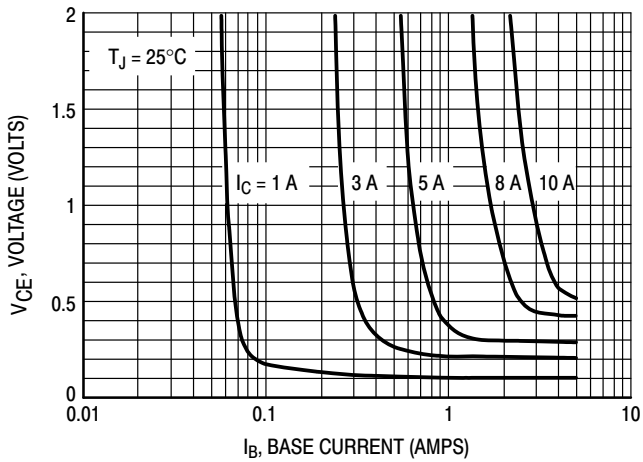


Figure 3. Collector Saturation Region

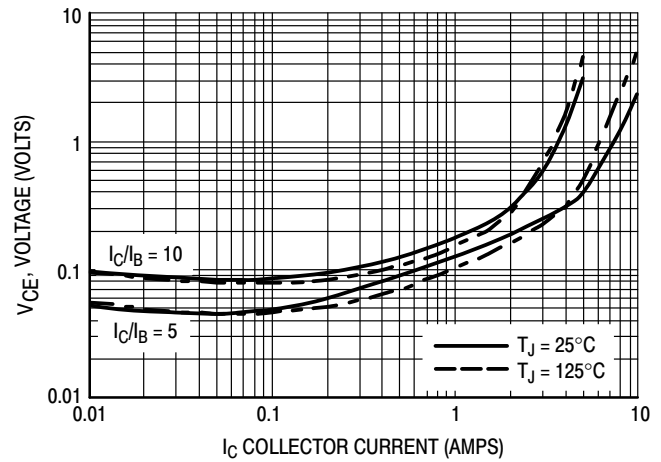


Figure 4. Collector-Emitter Saturation Voltage

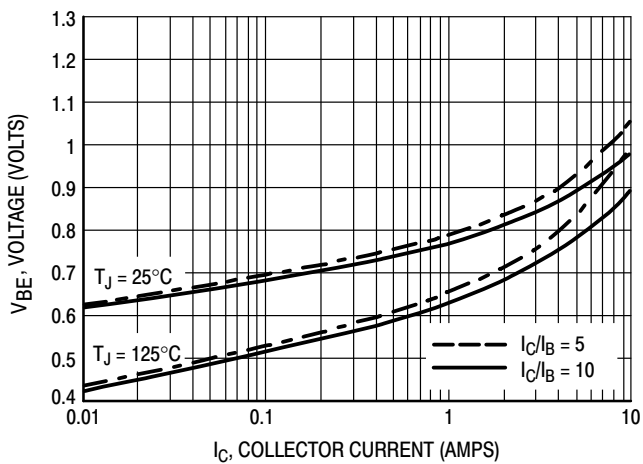


Figure 5. Base-Emitter Saturation Region

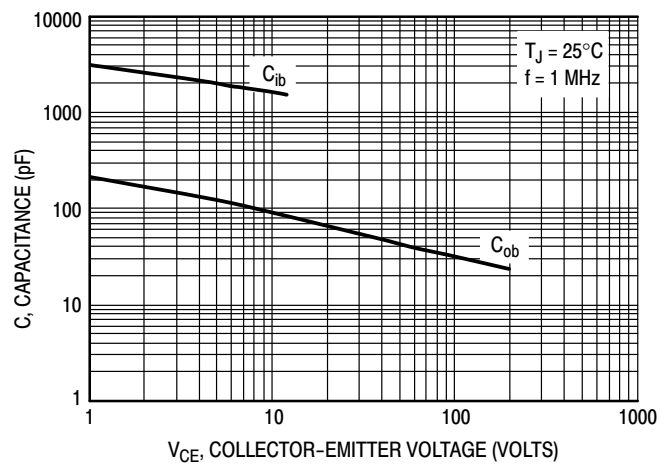


Figure 6. Capacitance

**TYPICAL SWITCHING CHARACTERISTICS**  
( $I_{B2} = I_C/2$  for all switching)

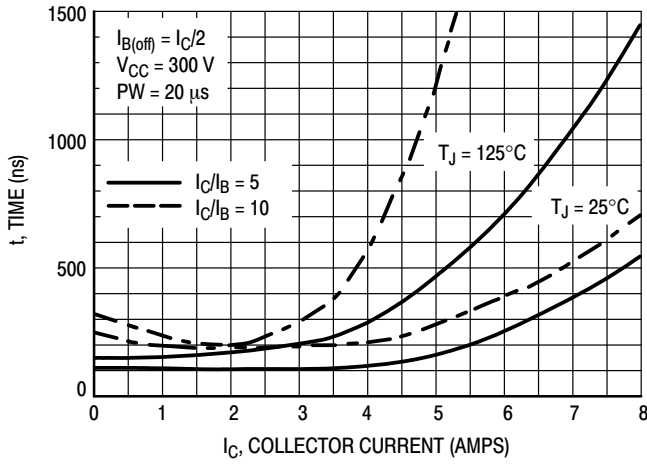


Figure 7. Resistive Switching,  $t_{on}$

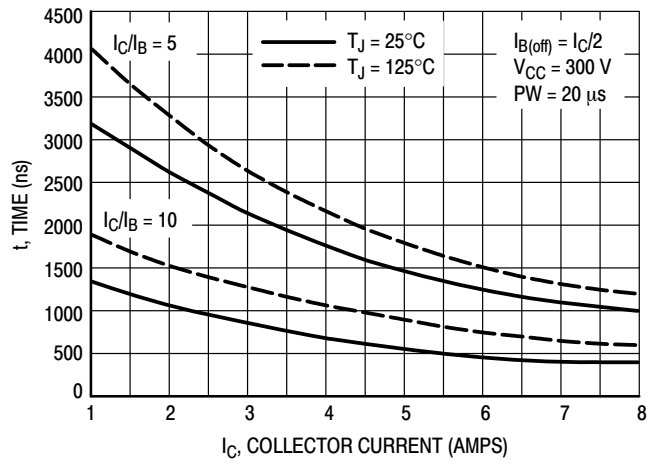


Figure 8. Resistive Switching,  $t_{off}$

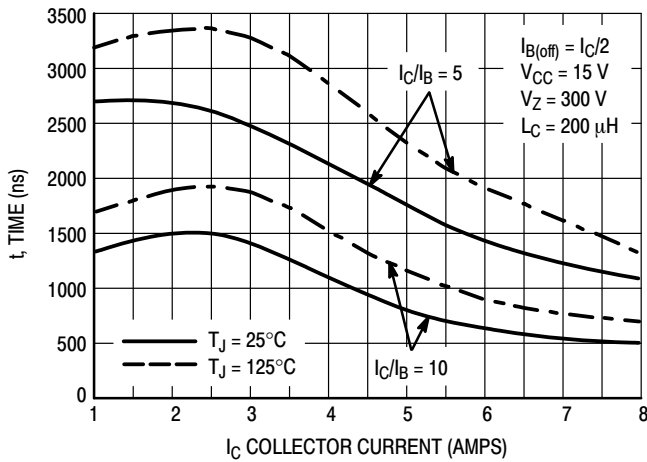


Figure 9. Inductive Storage Time,  $t_{si}$

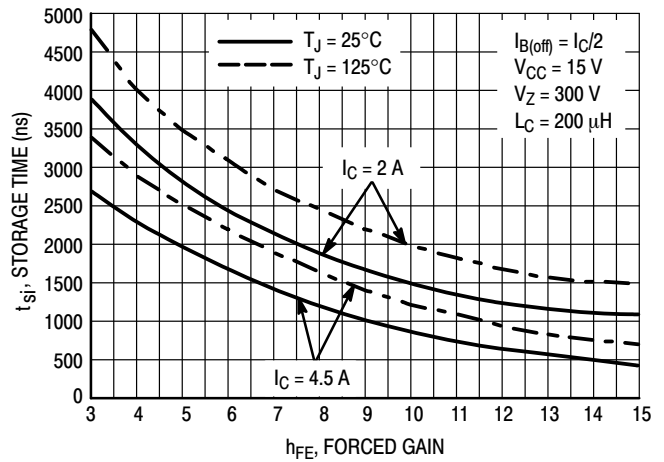


Figure 10. Inductive Storage Time,  $t_{si}(h_{FE})$

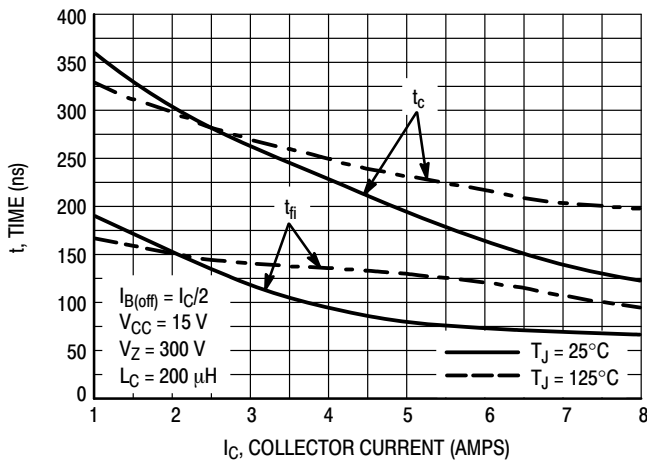


Figure 11. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 5$

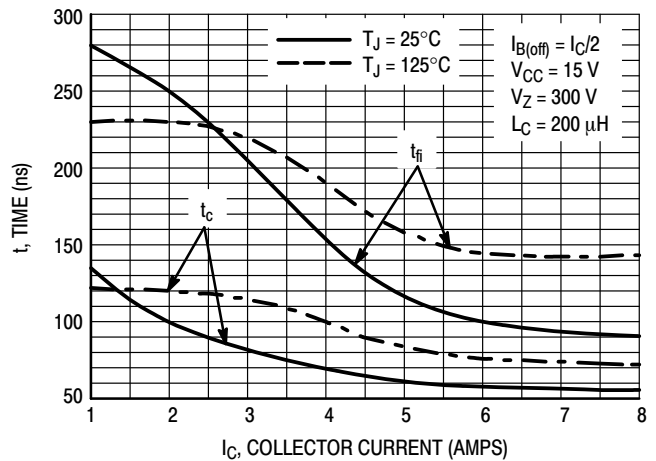


Figure 12. Inductive Switching,  $t_c$  and  $t_{fi}$   
 $I_C/I_B = 10$

**TYPICAL SWITCHING CHARACTERISTICS**  
( $I_{B2} = I_C/2$  for all switching)

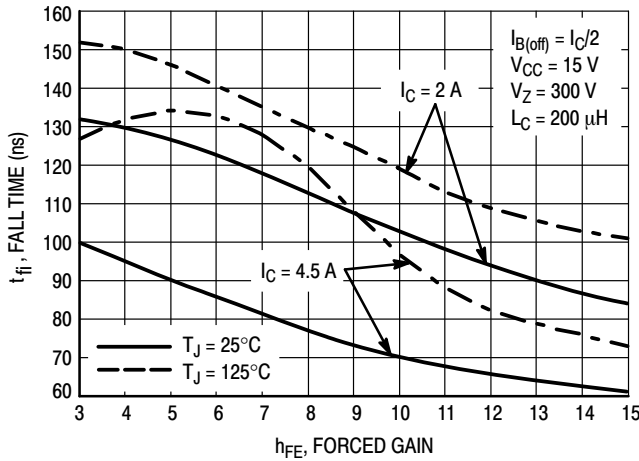


Figure 13. Inductive Fall Time

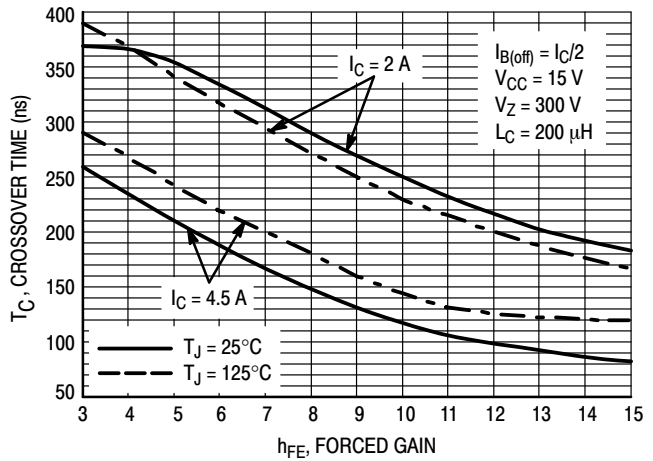


Figure 14. Inductive Crossover Time

**GUARANTEED SAFE OPERATING AREA INFORMATION**

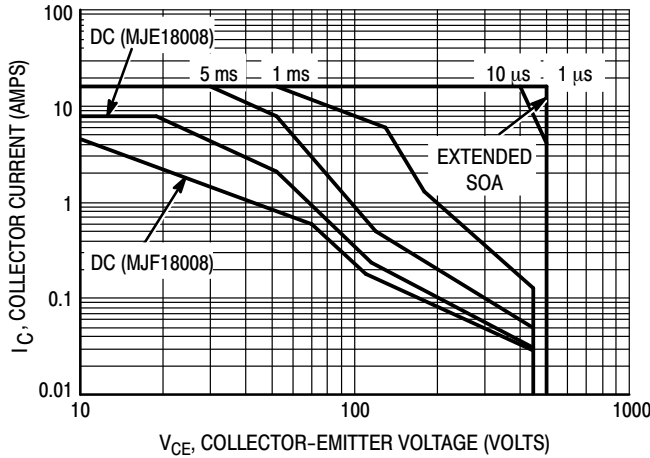


Figure 15. Forward Bias Safe Operating Area

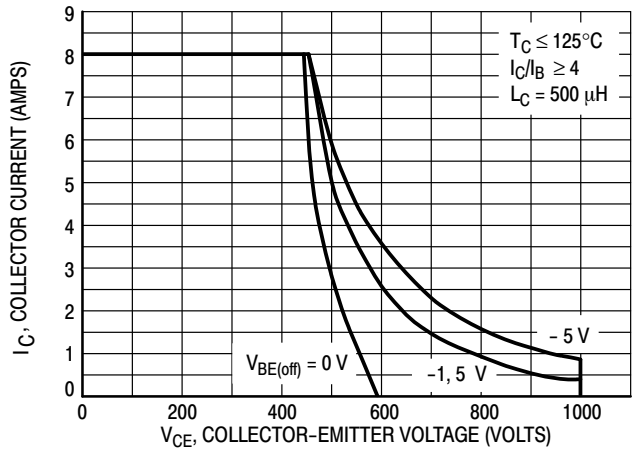


Figure 16. Reverse Bias Switching Safe Operating Area

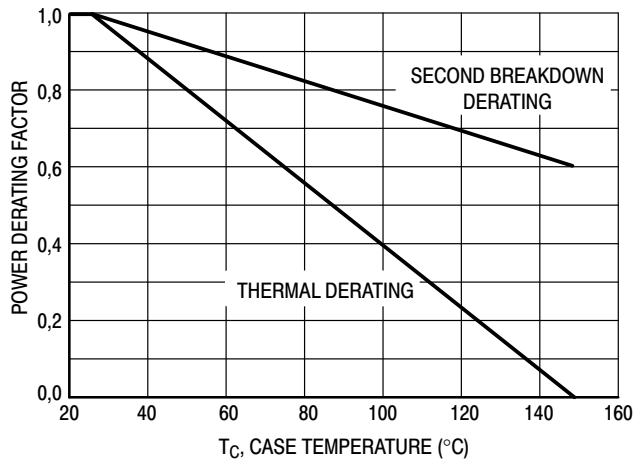


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$

limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_{J(pk)}$  may be calculated from the data in Figure 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.



# MJE18008G, MJF18008G

## TYPICAL THERMAL RESPONSE

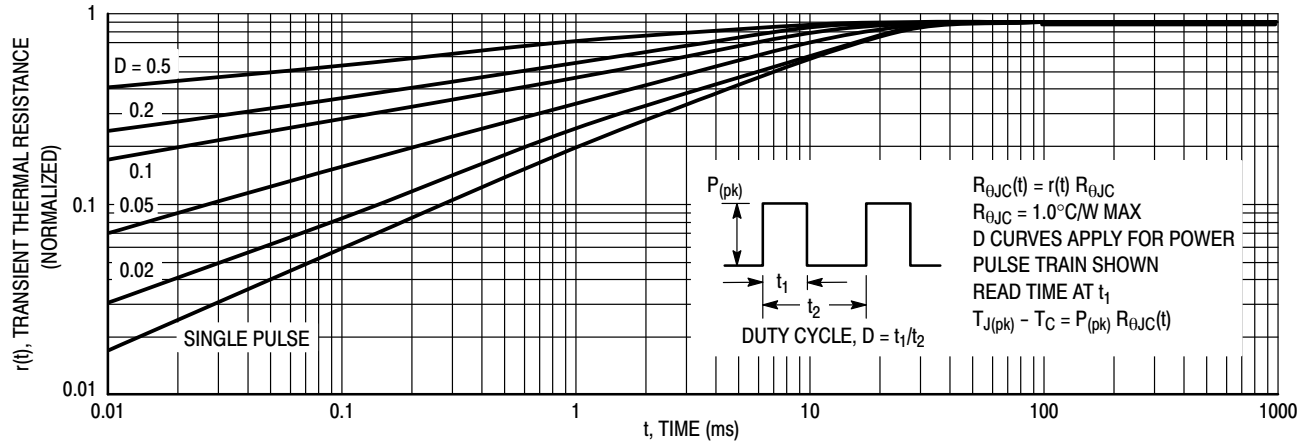


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for MJE18008

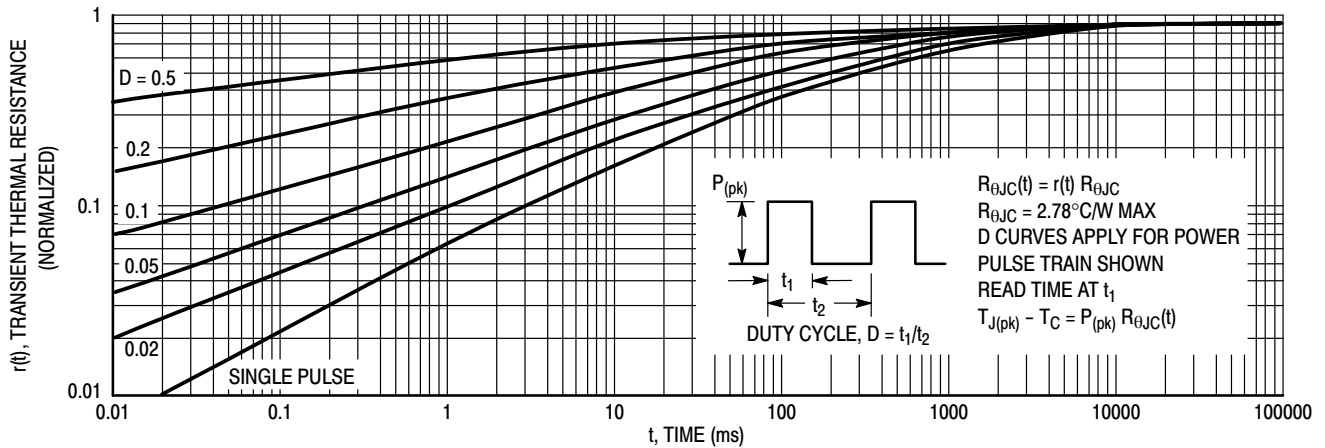


Figure 21. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for MJF18008

### ORDERING INFORMATION

Device	Package	Shipping
MJE18008G	TO-220AB (Pb-Free)	50 Units / Rail
MJF18008G	TO-220 (Fullpack) (Pb-Free)	50 Units / Rail

TEST CONDITIONS FOR ISOLATION TESTS\*

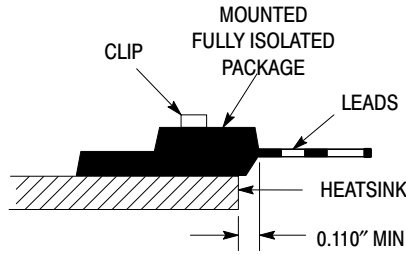


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

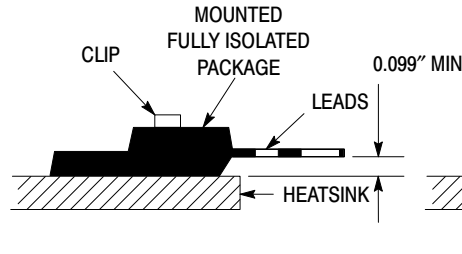


Figure 22b. Clip Mounting Position for Isolation Test Number 2

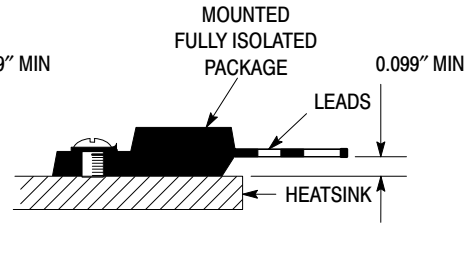


Figure 22c. Screw Mounting Position for Isolation Test Number 3

\*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION\*\*

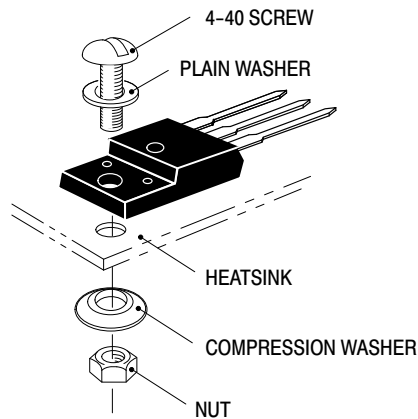


Figure 23a. Screw-Mounted

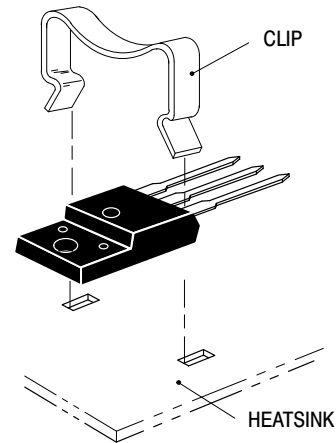


Figure 23b. Clip-Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

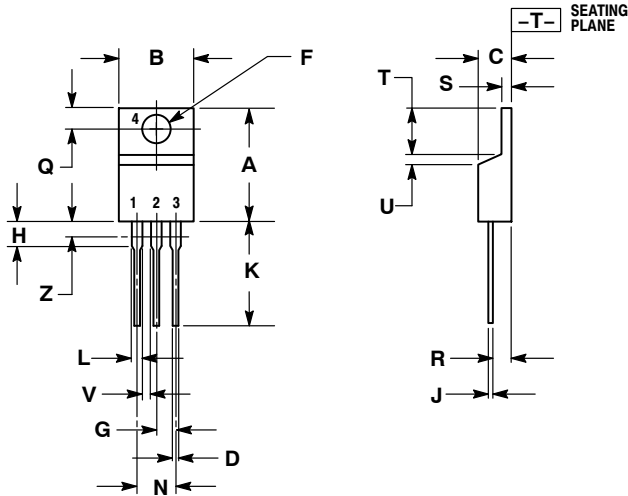
Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# MJE18008G, MJF18008G

## PACKAGE DIMENSIONS

### TO-220 CASE 221A-09 ISSUE AG

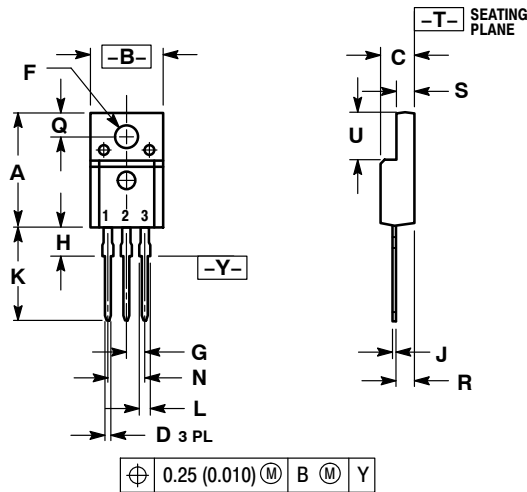


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 1:
- PIN 1. BASE
  - COLLECTOR
  - EMITTER
  - COLLECTOR


### TO-220 FULLPAK CASE 221D-03 ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH
  3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100	BSC	2.54	BSC
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200	BSC	5.08	BSC
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

- STYLE 2:
- PIN 1. BASE
  - COLLECTOR
  - EMITTER

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