

TOSHIBA Power MOS FET Module Silicon N&P Channel MOS Type (Four L²-π-MOSV in One)

MP4212

High Power High Speed Switching Applications H-Switch Driver

- 4-V gate drivability
- Small package by full molding (SIP 10 pin)
- High drain power dissipation (4-device operation)
: P_T = 4 W (T_a = 25°C)
- Low drain-source ON resistance: R_{DS} (ON) = 120 mΩ (typ.) (N-ch)
160 mΩ (typ.) (P-ch)
- High forward transfer admittance: |Y_{fs}| = 5.0 S (typ.) (Nch)
4.0 S (typ.) (Pch)
- Low leakage current: I_{GSS} = ±10 μA (max) (V_{GS} = ±16 V)
I_{DSS} = 100 μA (max) (V_{DS} = 60 V)
- Enhancement-mode: V_{th} = 0.8 to 2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Absolute Maximum Ratings (T_a = 25°C)

Characteristics		Symbol	Rating		Unit
			Nch	Pch	
Drain-source voltage		V _{DSS}	60	-60	V
Drain-gate voltage (R _{GS} = 20 kΩ)		V _{DGR}	60	-60	V
Gate-source voltage		V _{GSS}	±20	±20	V
Drain current	DC	I _D	5	-5	A
	Pulse	I _{DP}	20	-20	
Drain power dissipation (1-device operation, Ta = 25°C)		P _D	2.0		W
Drain power dissipation (4-device operation, Ta = 25°C)		P _{DT}	4.0		W
Single pulse avalanche energy (Note 1)		E _{AS}	129	273	mJ
Avalanche current		I _{AR}	5	-5	A
Repetitive avalanche energy (Note 2)	1-device operation	E _{AR}	0.2		mJ
	4-device operation	E _{ART}	0.4		
Channel temperature		T _{ch}	150		°C
Storage temperature range		T _{stg}	-55 to 150		°C

Note 1: Condition fo avalanche energy (single pulse) measurement

Nch: V_{DD} = 25 V, starting T_{ch} = 25°C, L = 7 mH, R_G = 25 Ω, I_{AR} = 5 A

Pch: V_{DD} = -25 V, starting T_{ch} = 25°C, L = 14.84 mH, R_G = 25 Ω, I_{AR} = -5 A

Note 2: Repetitive rating; pulse width limited by maximum channel temperature

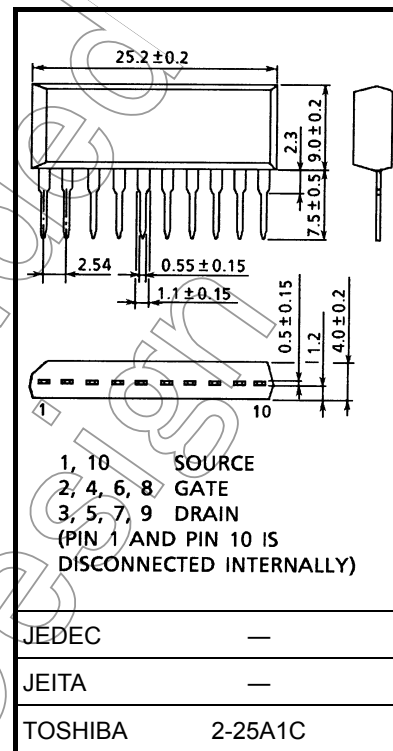
Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

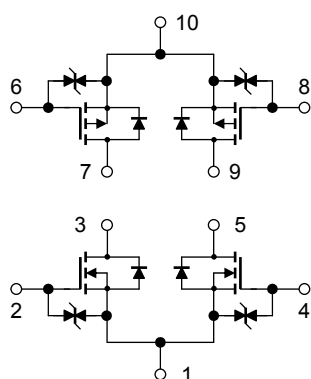
Industrial Applications

Unit: mm



Weight: 2.1 g (typ.)

Array Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance from channel to ambient (4-device operation, $T_a = 25^\circ\text{C}$)	$\Sigma R_{th}(\text{ch-a})$	31.2	$^\circ\text{C/W}$
Maximum lead temperature for soldering purposes (3.2 mm from case for $t = 10\text{ s}$)	T_L	260	$^\circ\text{C}$

Electrical Characteristics ($T_a = 25^\circ\text{C}$) (Nch MOS FET)

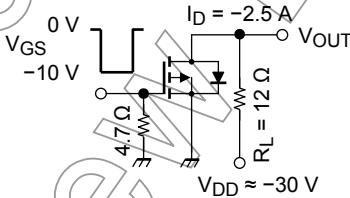
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	—	—	100	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}$, $V_{GS} = 0\text{ V}$	60	—	—	V
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$	0.8	—	2.0	V
Drain-source ON resistance	$R_{DS(ON)}$	$V_{GS} = 4\text{ V}$, $I_D = 2.5\text{ A}$	—	0.21	0.32	Ω
		$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$	—	0.12	0.16	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10\text{ V}$, $I_D = 2.5\text{ A}$	3.0	5.0	—	S
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	—	370	—	pF
Reverse transfer capacitance	C_{rss}		—	60	—	pF
Output capacitance	C_{oss}		—	180	—	pF
Switching time	Rise time		—	18	—	ns
	Turn-on time		—	25	—	
	Fall time		—	55	—	
	Turn-off time		—	170	—	
Total gate charge (Gate-source plus gate-drain)	Q_g	$V_{DD} \approx 48\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$	—	12	—	nC
Gate-source charge	Q_{gs}		—	8	—	nC
Gate-drain ("miller") charge	Q_{gd}		—	4	—	nC

Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	5	A
Pulse drain reverse current	I_{DRP}	—	—	—	20	A
Diode forward voltage	V_{DSF}	$I_{DR} = 5 \text{ A}$, $V_{GS} = 0 \text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 5 \text{ A}$, $V_{GS} = 0 \text{ V}$	—	70	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 50 \text{ A}/\mu\text{s}$	—	0.1	—	μC

Electrical Characteristics (Ta = 25°C) (Pch MOS FET)

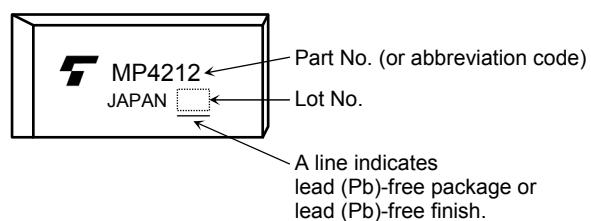
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-off current	I_{DSS}	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0 \text{ V}$	—	—	-100	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -10 \text{ mA}$, $V_{GS} = 0 \text{ V}$	-60	—	—	V
Gate threshold voltage	V_{th}	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$	-0.8	—	-2.0	V
Drain-source ON resistance	$R_{DS(ON)}$	$V_{GS} = -4 \text{ V}$, $I_D = -2.5 \text{ A}$	—	0.24	0.28	Ω
		$V_{GS} = -10 \text{ V}$, $I_D = -2.5 \text{ A}$	—	0.16	0.19	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -10 \text{ V}$, $I_D = -2.5 \text{ A}$	2.0	4.0	—	S
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	—	630	—	pF
Reverse transfer capacitance	C_{rss}		—	95	—	pF
Output capacitance	C_{oss}		—	290	—	pF
Switching time	Rise time	t_r	—	25	—	ns
	Turn-on time	t_{on}	—	45	—	
	Fall time	t_f	—	55	—	
	Turn-off time	t_{off}	—	200	—	
Total gate charge (gate-source plus gate-drain)		Q_g	—	22	—	nC
Gate-source charge		Q_{gs}	—	16	—	nC
Gate-drain ("miller") charge		Q_{gd}	—	6	—	nC



Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

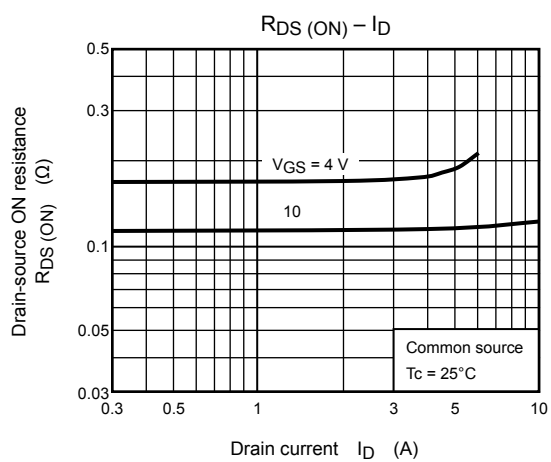
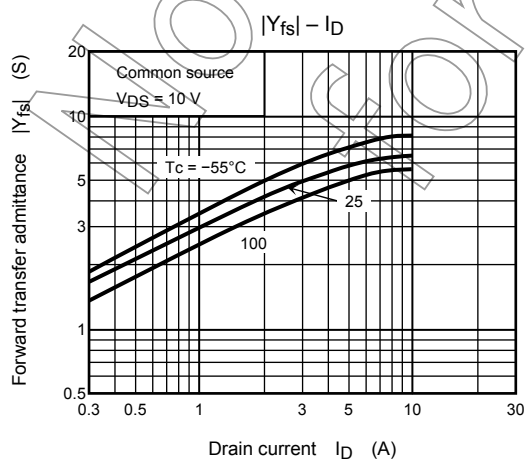
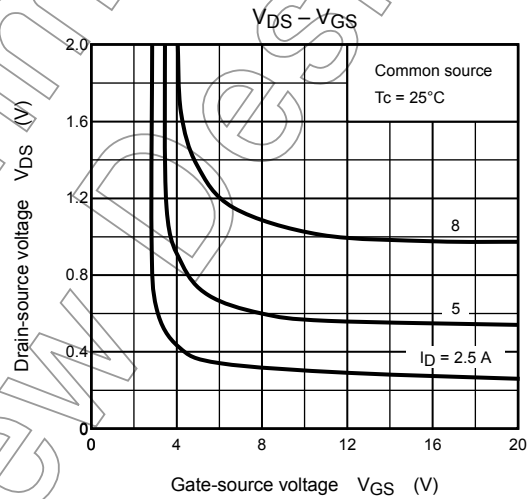
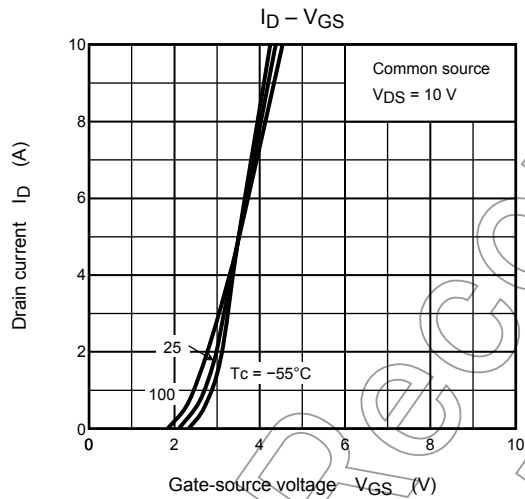
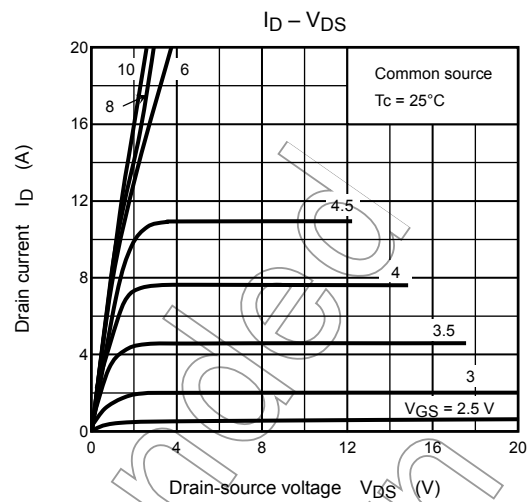
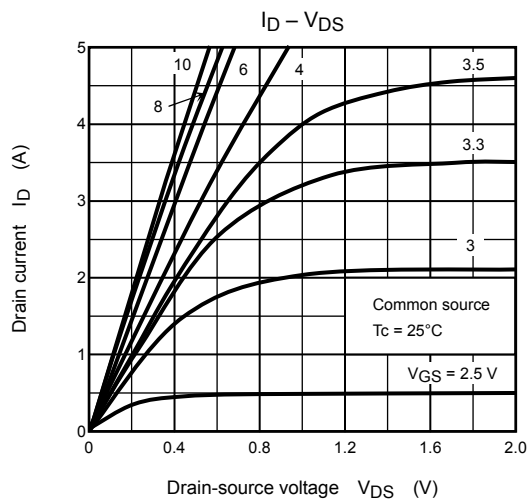
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	-5	A
Pulse drain reverse current	I_{DRP}	—	—	—	-20	A
Diode forward voltage	V_{DSF}	$I_{DR} = -5 \text{ A}$, $V_{GS} = 0 \text{ V}$	—	—	1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = -5 \text{ A}$, $V_{GS} = 0 \text{ V}$	—	80	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 50 \text{ A}/\mu\text{s}$	—	0.1	—	μC

Marking

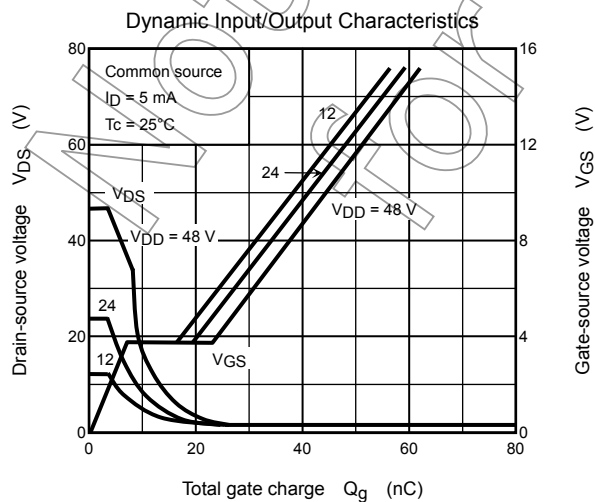
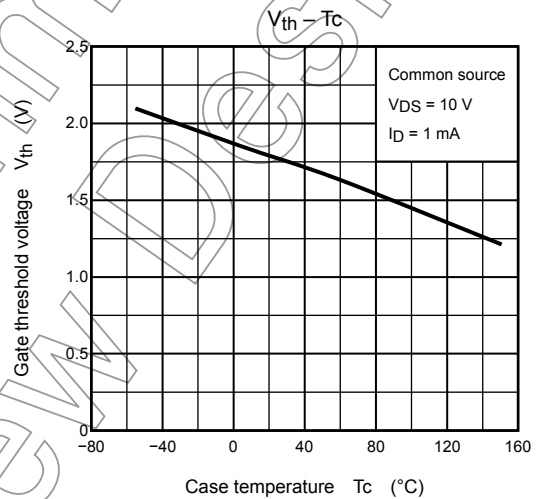
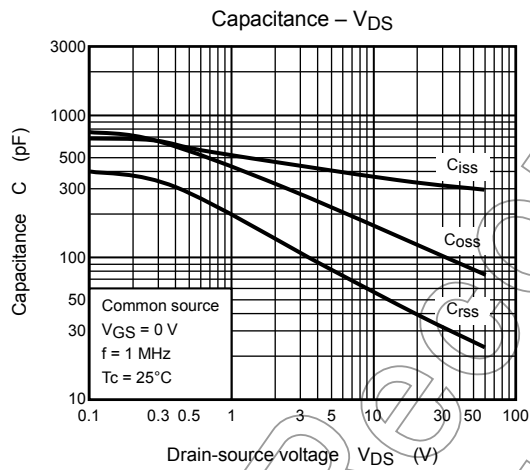
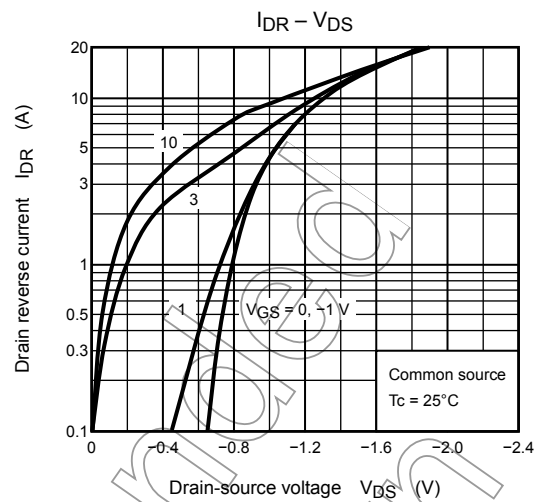
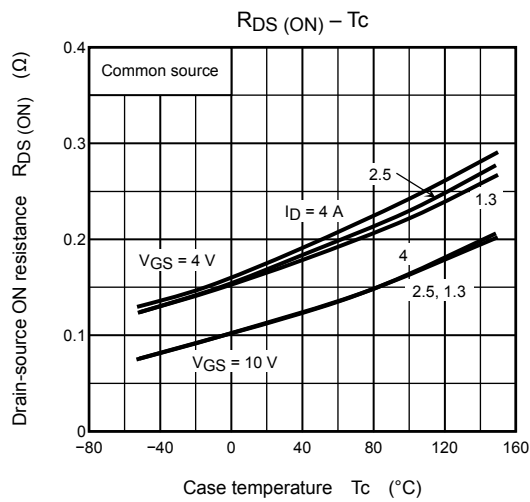


Not Recommended
for New Design

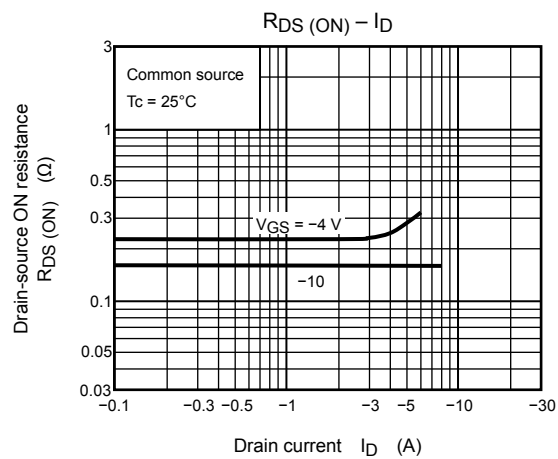
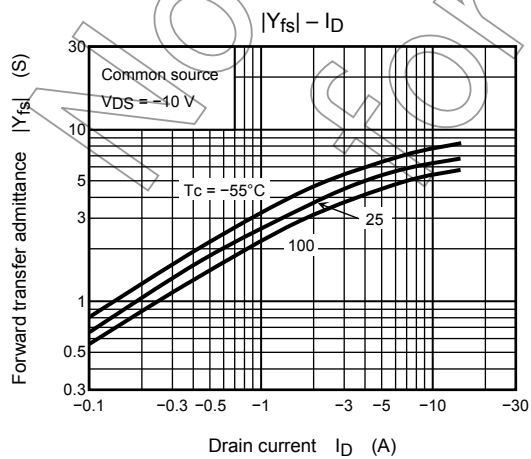
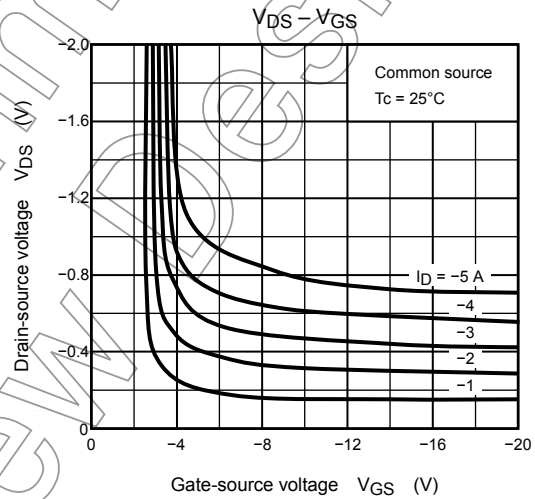
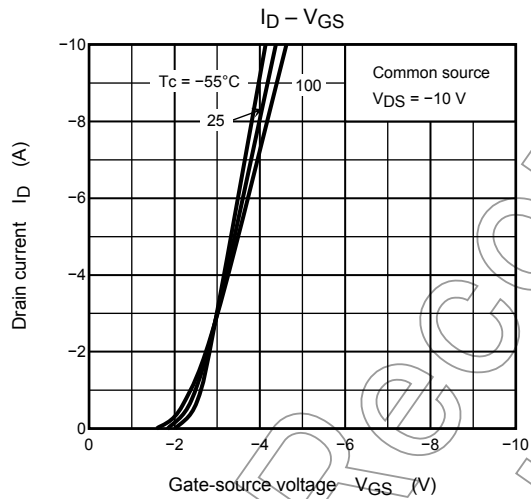
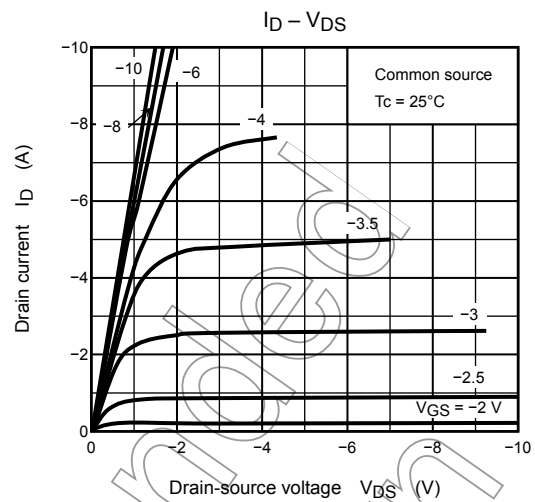
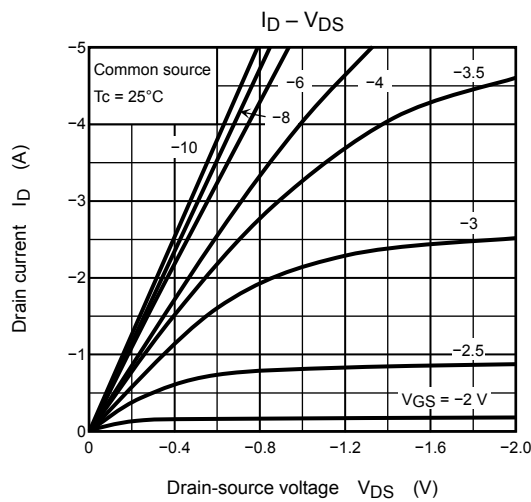
Nch MOS FET



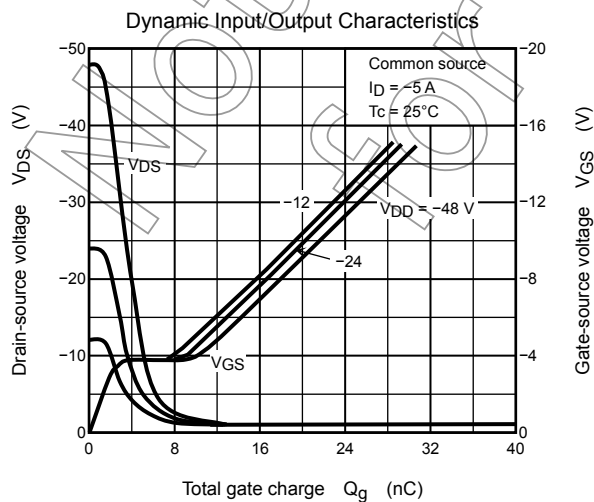
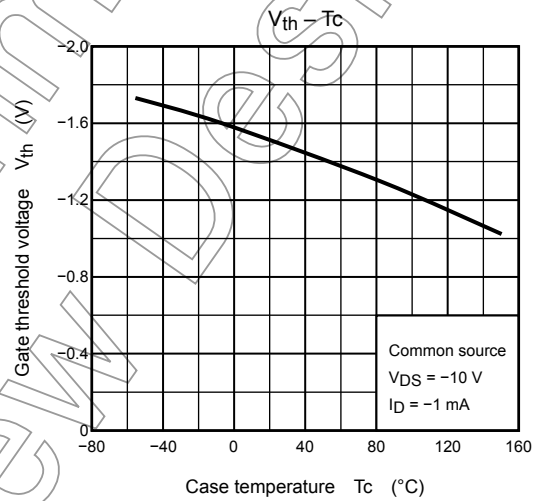
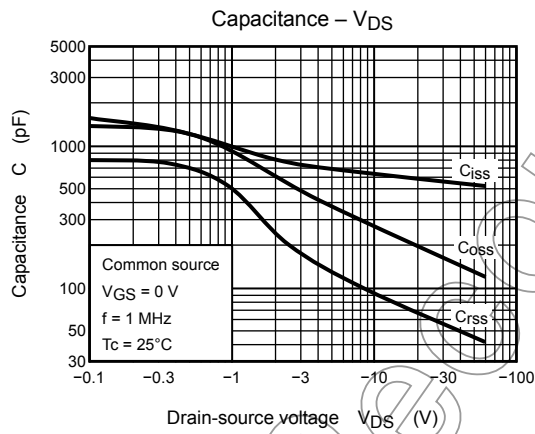
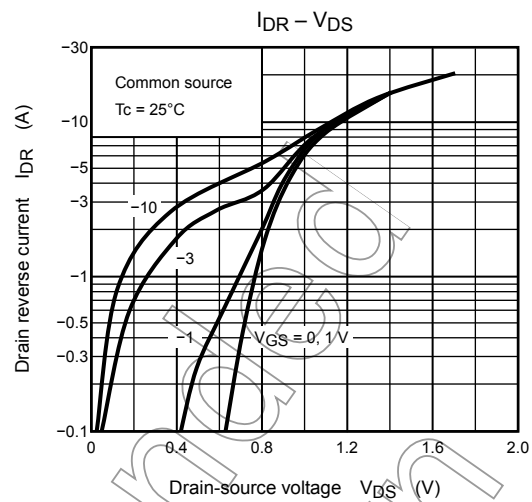
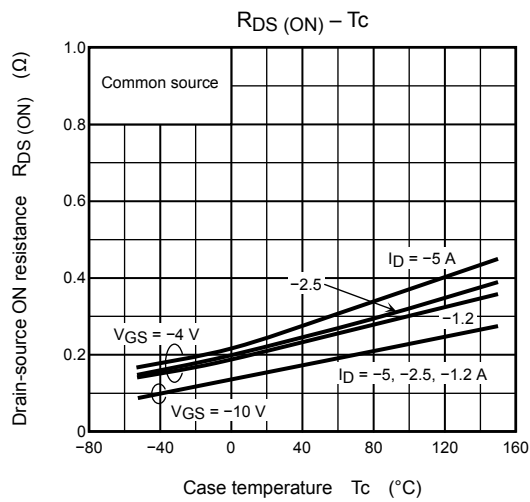
Nch MOS FET

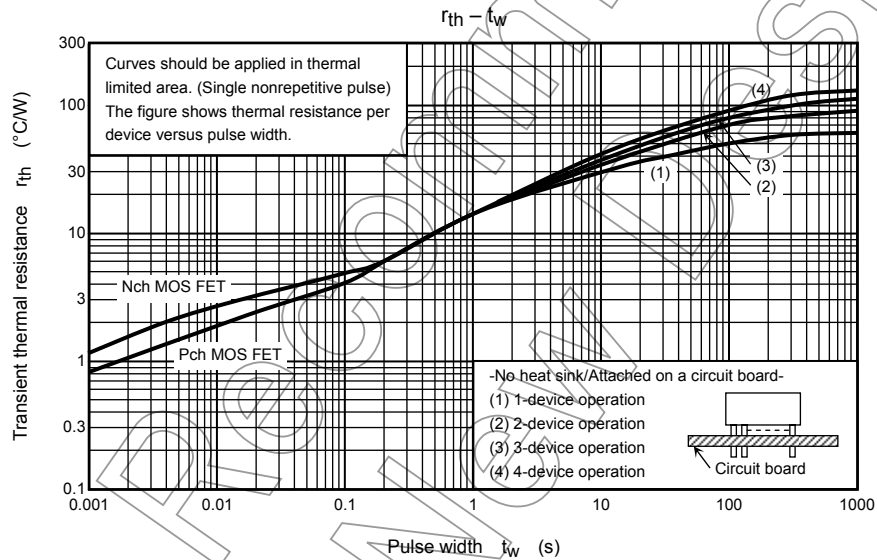
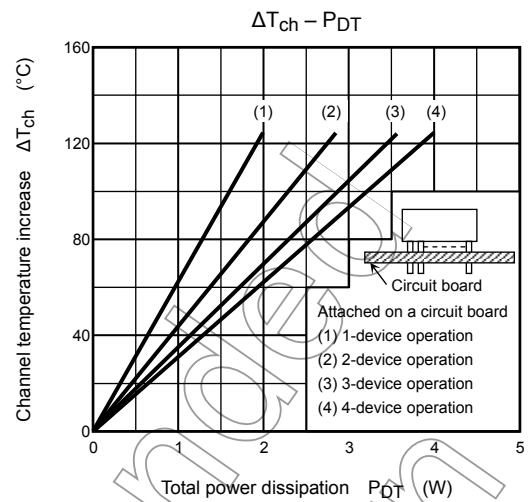
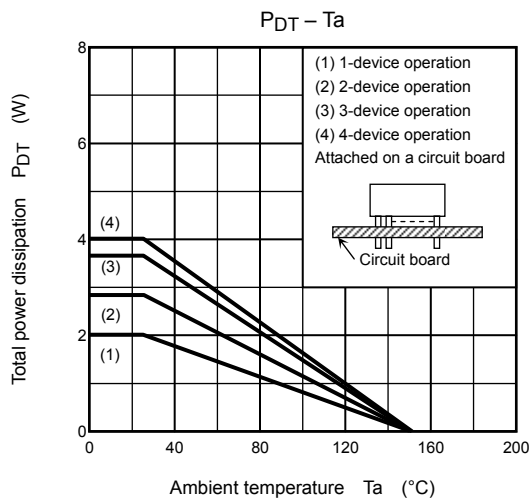


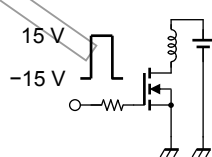
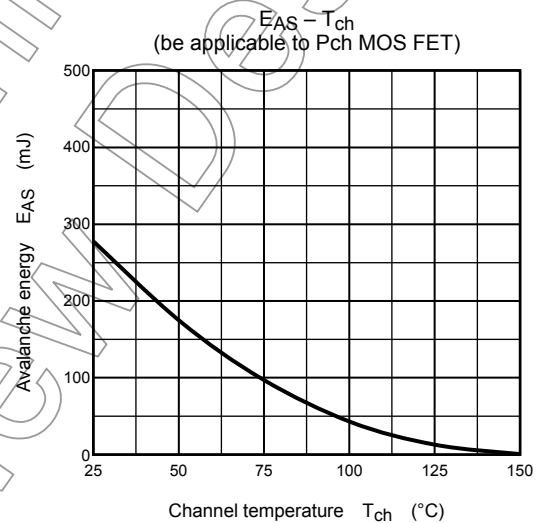
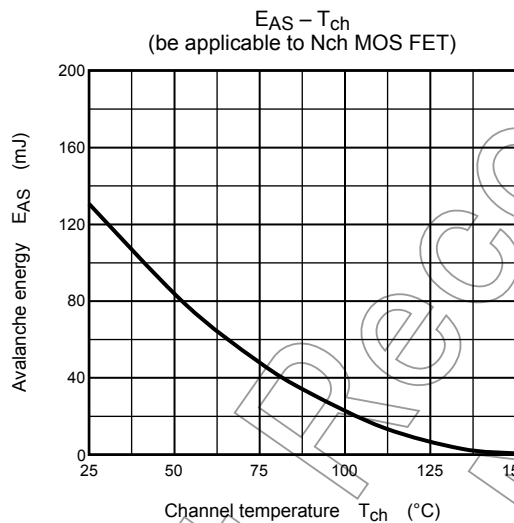
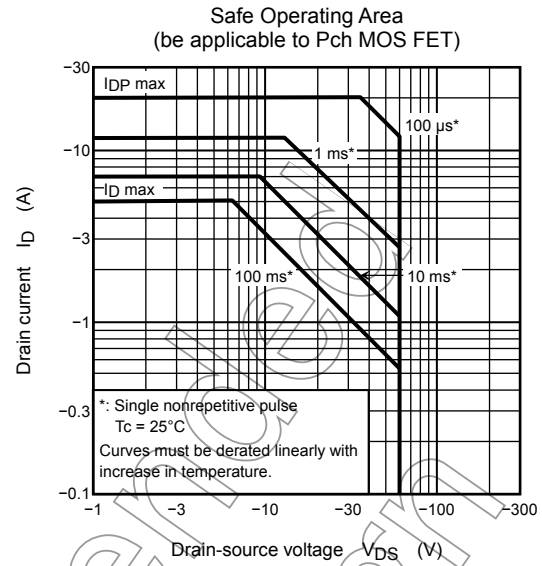
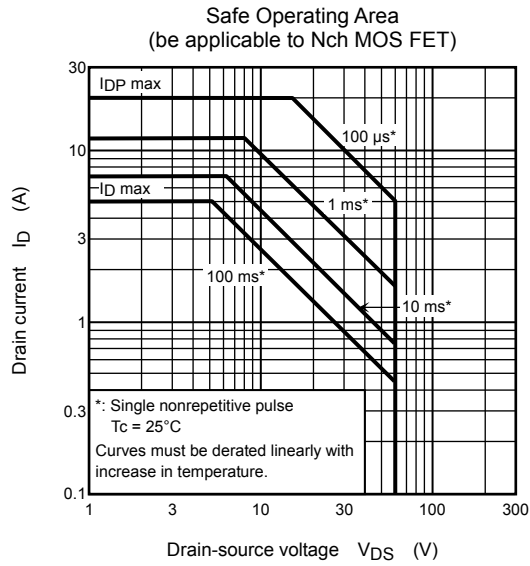
Pch MOS FET



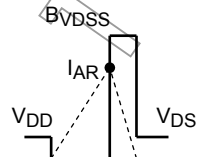
Pch MOS FET







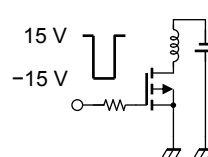
TEST CIRCUIT



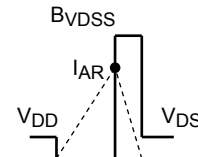
TEST WAVE FORM

Peak $I_{AR} = 5\text{ A}$, $R_G = 25\ \Omega$
 $V_{DD} = 25\text{ V}$, $L = 7\text{ mH}$

$$E_{AS} = \frac{1}{2} L \cdot I^2 \cdot \left(\frac{B_{VDS}}{B_{VDS} - V_{DD}} \right)$$



TEST CIRCUIT



TEST WAVE FORM

Peak $I_{AR} = -5\text{ A}$, $R_G = 25\ \Omega$
 $V_{DD} = -25\text{ V}$, $L = 14.84\text{ mH}$

$$E_{AS} = \frac{1}{2} L \cdot I^2 \cdot \left(\frac{B_{VDS}}{B_{VDS} - V_{DD}} \right)$$

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20070701-EN

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