1/4.5-Inch 1.6Mp CMOS Digital Image Sensor

MT9M032

For the latest data sheet, refer to Micron's Web site: www.micron.com/imaging

Features

- DigitalClarity® CMOS imaging technology
- Maximum frame rate (1284H x 812V/60 fps at 99 MHz)
- Superior low-light performance
- Low dark current
- Global reset release (GRR), which starts the exposure of all rows simultaneously
- Simple two-wire serial interface
- Programmable controls: gain, frame rate, frame size, exposure
- Horizontal and vertical mirror image
- Automatic black level calibration
- On-chip phase-locked loop (PLL) oscillator
- Bulb exposure mode for arbitrary exposure times
- Snapshot mode to take frames on demand
- Parallel data output
- Electronic rolling shutter (ERS), progressive scan
- Arbitrary image decimation with anti-aliasing
- Programmable I/O slew rate
- Programmable power-down mode (mode A or mode B)
- Xenon and LED flash support with fast exposure adaptation
- Flexible support for external auto focus, optical zoom, and mechanical shutter

Ordering Information

Table 1: Available Part Numbers

Part Number	Description
MT9M032C12STCES	48-pin Pb-free CLCC/color
MT9M032C12STMUES	48-pin Pb-free CLCC/mono/ parallel
MT9M032C12STMUHES	48-pin Pb-free CLCC/mono/ parallel headboard
MT9M032C12STCHES	48-pin Pb-free CLCC/color/ parallel headboard
MT9M032C12STCDES	48-pin Pb-free color demo kit
MT9M032C12STMUDES	48-pin Pb-free mono demo kit

Table 2: Key Performance Parameters

Parameter		Value
Optical format		1/4.5-inch (4:3)
Active imager size		3.24mm(H) x 2.41mm(V)
Active pixels		1472H x 1096V
Pixel size		2.2 x 2.2µm
Color filter array		RGB Bayer pattern, mono
Shutter type		Global reset release (GRR) (snapshot only), electronic rolling shutter (ERS)
Maximum data rate/ master clock		99 Mp/s / 49.5 MHz
Frame rate	1440H x 1080V	Programmable up to 30 fps
	1280H x 720V	Programmable up to 60 fps
ADC resolution		12-bit, on-chip
Responsivity		1.4 V/lux-sec (550nm) 2.1 V/lux-sec (monochrome)
Dynamic range		70.1dB
SNR_{MAX}		38.1dB
Supply voltage	Digital	1.7–1.9V
	I/O	2.6–3.1V
	PLL	2.6–3.1V
	Analog	2.6–3.1V
Power consumption		364.6mW at 2.8V
Operating temperature		–30°C to +70°C
Packaging		48-pin CLCC

Applications

- High definition surveillance camera
- High speed surveillance camera
- ePTZ camera

General Description

The Micron® Imaging MT9M032 is a 1/4.5-inch format CMOS active-pixel digital image sensor with a pixel array of 1472H x 1096V. The default active imaging array size is 1440 x 1080. It incorporates sophisticated on-chip camera functions such as windowing, mirroring, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The MT9M032 digital image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

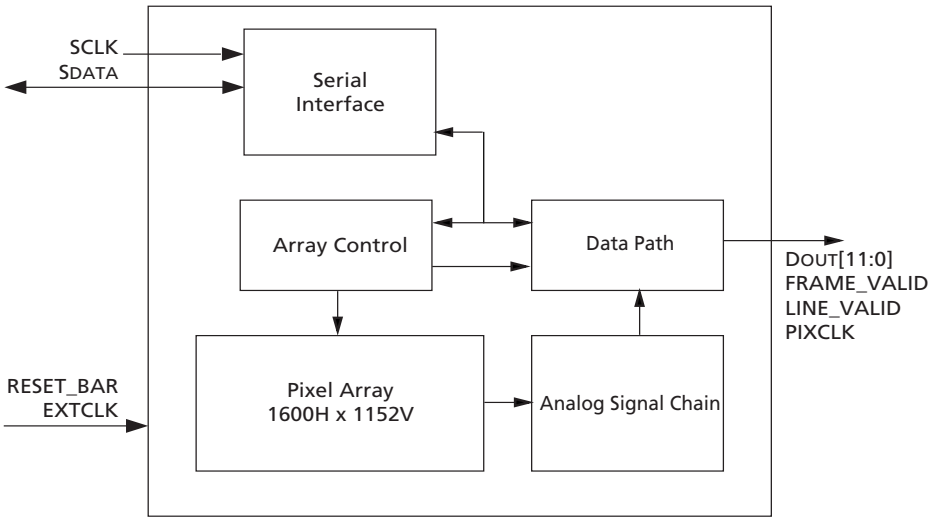
Functional Overview

The MT9M032 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 8 and 16.5 MHz.

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.6Mp active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light.

The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 99 Mp/s, in addition to frame and line synchronization signals in parallel mode corresponding to a pixel clock rate of 99 MHz. Figure 1 shows the block diagram of the sensor.

Figure 1: Block Diagram – Parallel Output



The pixel array contains optically active and light-shielded (dark) pixels. The dark pixels are used to provide data for on-chip offset correction algorithms (black level control).

The sensor contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers can be accessed through a two-wire serial interface.

The output from the sensor (MT9M032C12STC) is a Bayer pattern; alternate rows are a sequence of either green and red pixels or blue and green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

A flash strobe output signal is provided to allow an external xenon or LED light source to synchronize with the sensor exposure time and to support the provision of an external mechanical shutter.

Signal Descriptions

Table 3 provides signal descriptions for the MT9M032.

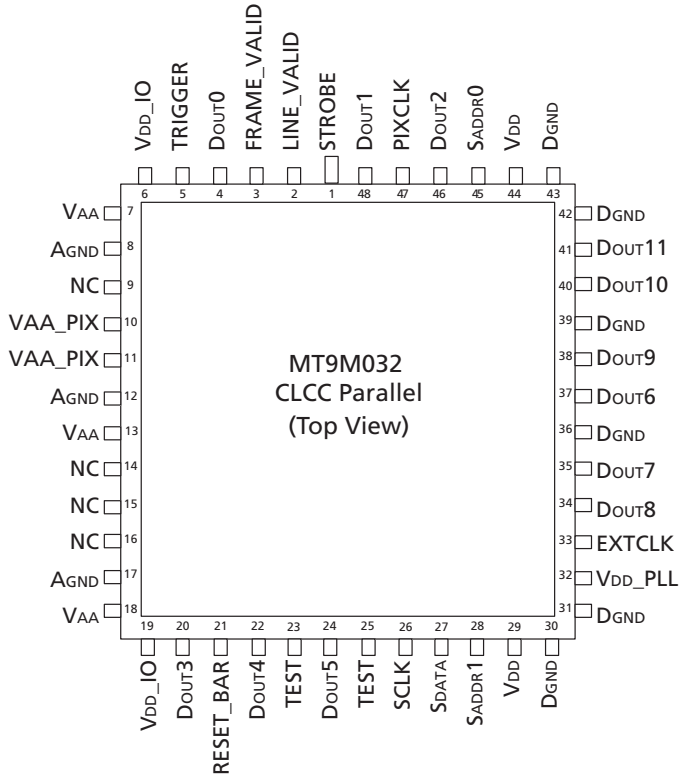
Table 3: Signal Descriptions

Pin Numbers	Name	Type	Description
26	SCLK	Input	Serial clock. Pull to VDD_IO with a 1.5kΩ resistor (depending on bus loading).
21	RESET_BAR	Input	Master reset signal, active LOW.
33	EXTCLK	Input	Input clock signal 8–49.5 MHz.
5	TRIGGER	Input	Snapshot trigger. Used to trigger one frame of output in snapshot modes.
23, 25	TEST	Input	Enables manufacturing test modes. Tie to digital GND for functional operation.
45	SADDR0	Input	Serial address. Pull to VDD_IO or DGND to set serial address.
28	SADDR1	Input	Serial address. Pull to VDD_IO or DGND to set serial address.
27	SDATA	I/O	Serial data. Pull to VDD_IO with a 1.5kΩ resistor (depending on bus loading).
1	STROBE	Output	Snapshot strobe. Driven HIGH when all pixels are exposing in snapshot modes.
4	DOUT[0]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
48	DOUT[1]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
46	DOUT[2]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
20	DOUT[3]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
22	DOUT[4]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
24	DOUT[5]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
37	DOUT[6]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
35	DOUT[7]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
34	DOUT[8]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
38	DOUT[9]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
40	DOUT[10]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
41	DOUT[11]	Output	Pixel data. Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
47	PIXCLK	Output	Pixel clock. Used to qualify the LINE_VALID (LV), FRAME_VALID (FV), and DOUT(11:0). These outputs should be captured on the falling edge of this signal.
3	FRAME_VALID	Output	Frame valid. Qualified by PIXCLK. Driven HIGH during active pixels and horizontal blanking of each frame and LOW during vertical blanking.
2	LINE_VALID	Output	Line valid output. Qualified by PIXCLK. Driven HIGH with active pixels of each line and LOW during horizontal blanking periods. External pull-down resistor to DGND (typical 10kΩ–100kΩ) required for proper initialization sequence.
29, 44	VDD	Supply	Digital power 1.8V nominal.

Table 3: Signal Descriptions (continued)

Pin Numbers	Name	Type	Description
10, 11	VAA_PIX	Supply	Pixel array power 2.8V nominal.
7, 13, 18	VAA	Supply	Analog power 2.8V nominal.
32	VDD_PLL	Supply	PLL power 2.8V nominal.
6, 19	VDD_IO	Supply	I/O power supply 2.8V nominal.
30, 31, 36, 39, 42, 43	DGND	Supply	Digital ground.
8, 12, 17	AGND	Supply	Analog ground.
9, 14, 15, 16	NC	–	No connect.

Figure 2: 48-Pin CLCC 10 x 10 Package Pinout Diagram (Top View)

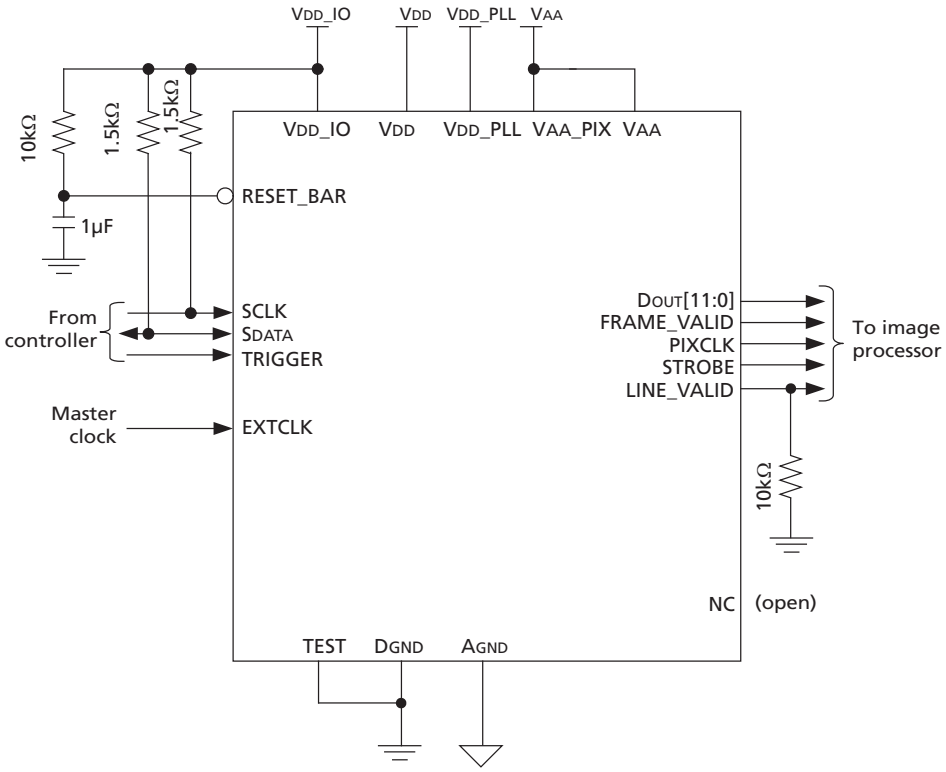


Typical Connections

Figure 3 shows typical connections for the MT9M032 sensor. For low-noise operation, the MT9M032 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled from ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9M032 also supports different digital core (VDD/DGND) and I/O power (VDD_IO/DGND) power domains that can be at different voltages. PLL requires a clean power source (VDD_PLL).

Figure 3: Typical Configuration



Notes:
1. Typical connection shows only one scenario out of multiple possible variations for this sensor.
2. All inputs must be configured with VDD_IO.
3. VAA and VAA_PIX must be tied together.

Pixel Array Structure

The MT9M032 pixel array consists of a 1600-column by 1152-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array, looking at the sensor, as shown in Figure 4.

The array consists of a 1440-column by 1080-row active region in the center representing the default output image resolution, surrounded by a boundary region (also active), surrounded by a border of dark pixels (see Table 4 and Table 5). The boundary region can be used to avoid edge effects when doing color processing, while the optically black column and rows can be used to monitor the black level.

Table 4: Pixel Type by Column

Column	Pixel Type
0–15	Active boundary (16)
16–1455	Active image (1440)
1456–1471	Active boundary (16)
1472–1599	Black (128)

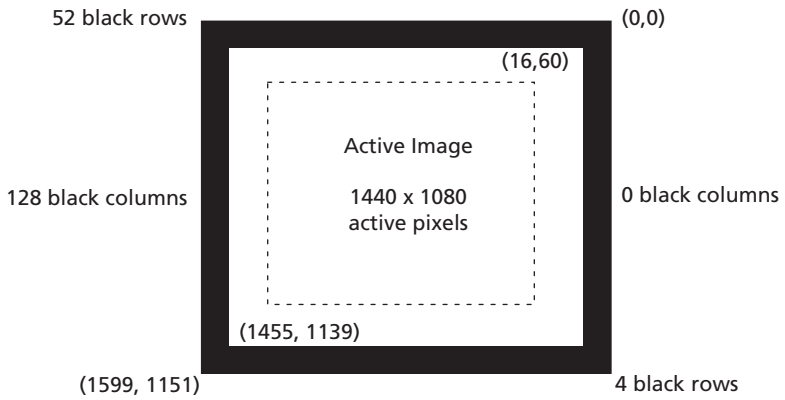
Table 5: Pixel Type by Row

Row	Pixel Type
0–51	Black (52)
53–59	Active boundary (8)
60–1139	Active image (1080)
1140–1147	Active boundary (8)
1148–1151	Black (4)

Default Readout Order

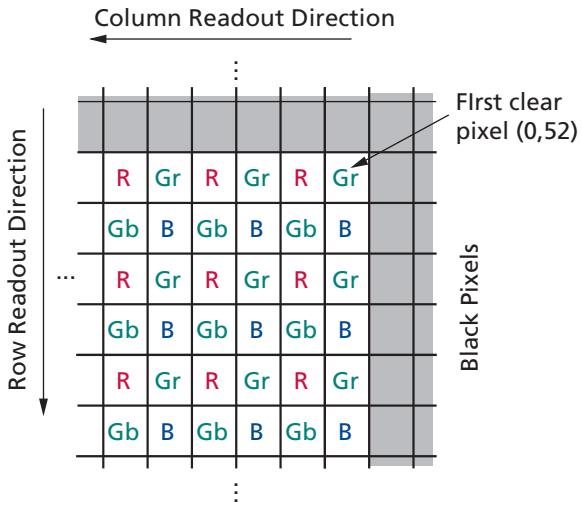
By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 4). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (16,60).

Figure 4: Pixel Array Description



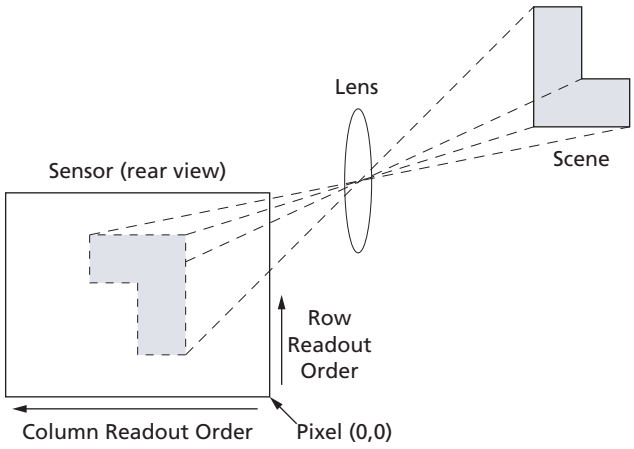
Sensor pixels are output in a Bayer pattern format consisting of four "colors"—GreenR, GreenB, Red, and Blue (Gr, Gb, R, B)—representing three filter colors. When no mirror modes are enabled, even-numbered rows contain alternate greenR and red pixels; odd-numbered rows contain alternate blue and greenB pixels. Even-numbered columns contain greenR and blue pixels; odd-numbered columns contain red and greenB pixels. The GreenR and GreenB pixels have the same color filter, but they are treated as separate colors by the data path and analog signal chain.

Figure 5: Pixel Color Pattern Detail (Top Right Corner)



When the sensor is imaging, the active surface of the sensor faces the scene, as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced, as shown in Figure 5.

Figure 6: Imaging a Scene

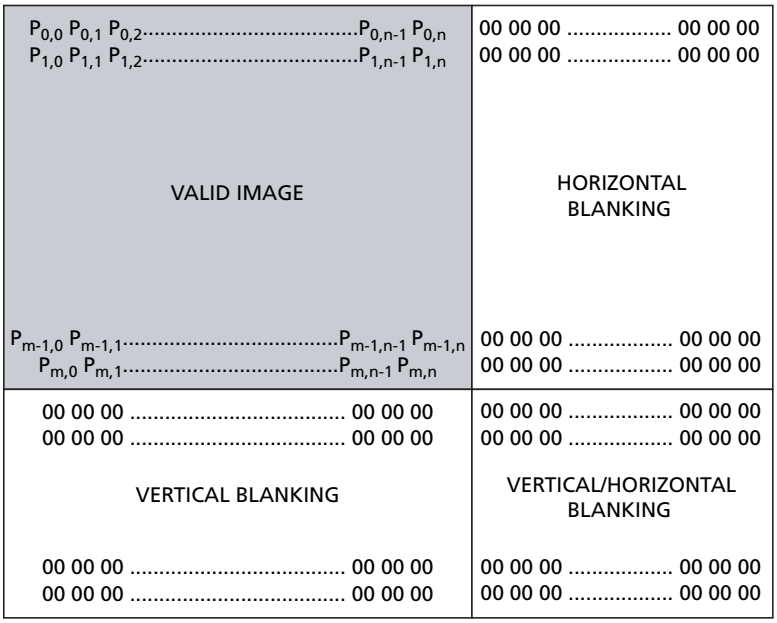


Output Data Format

Parallel Pixel Data Interface

MT9M032 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 7. The amount of horizontal blanking and vertical blanking is programmable; LV is HIGH during the shaded region of the figure. FV timing is described in the next section.

Figure 7: Spatial Illustration of Image Readout



Serial Bus Description

Registers are written to and read from the MT9M032 through the two-wire serial interface bus. The MT9M032 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9M032 through the serial data (SDATA) line. The SDATA line is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can pull the SDATA line LOW—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial defines several different transmission codes, as shown in the following sequence:

1. a start bit
2. the slave device 8-bit address
3. an (a no) acknowledge bit
4. an 8-bit message
5. a stop bit

Sequence

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request is a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a WRITE should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9M032 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the WRITE request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is automatically incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A “0” in the LSB (least significant bit) of the address indicates write mode (0xB8), and a “1” indicates read mode (0xB9).

The two-wire serial interface device addresses consists of 7 bits. For the MT9M032 sensor, the device is fixed at [1011100].

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

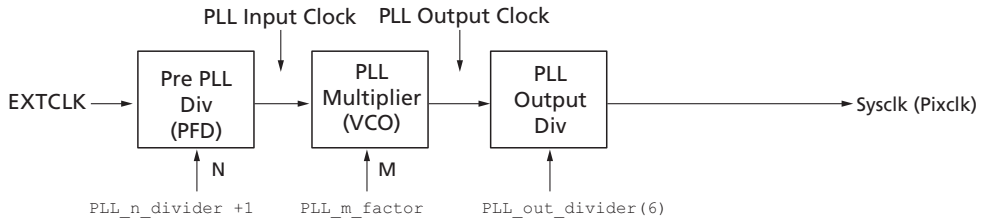
Features

PLL-Generated Master Clock

The PLL can generate a PIXCLK clock signal whose frequency is up to 99 MHz (input clock from 8–16.5 MHz). The PLL-generated clock can be controlled by programming the appropriate register. It is possible to bypass the PLL and use EXTCLK as master clock. By default, the PLL is powered up.

The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and PLL output divider stage to generate the output clock. The clocking structure is shown in Figure 8. PLL control can be programmed to generate desired pixel clock frequency.

Figure 8: PLL-Generated Master Clock



Note: The PLL control registers must be programmed while the sensor is in the software standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is undefined.

PLL Setup

To use the PLL:

1. Bring the MT9M032 up as normal, ensure that ^{f}EXTCLK is between 8 and 16.5 MHz.
2. Set PLL out divider to 7. (Power-up default PLL out divider setting is 6.)
3. Set PLL_m_factor and PLL_n_divider based on the desired input (^{f}EXTCLK) and output (^{f}PIXCLK) frequencies.
   Using this formula:
   ^{f}PIXCLK = ^{f}VCO/7
   where
   ^{f}VCO = (^{f}EXTCLK x M) / N
   M = PLL_m_factor,
   N = (PLL_n_divider + 1)
   Example of PLL setting:
   ^{f}EXTCLK = 13.5 MHz
   PLL_m_factor = 0x9A (154), PLL_n_divider = 0x02
   ^{f}PIXCLK = 99 MHz
4. Wait 1ms to ensure that the VCO has locked.
5. Set R0x10 = 0x0053
6. Delay = 1ms
7. Enable parallel data output
8. Delay = 1ms

Table 6: Frequency Parameters

Parameter	Equation	Min	Max	Unit
PLL_n_divider	–	0	63	
PLL_m_factor	–	16	255	
^{f}EXTCLK	–	8	16.5	MHz
^{f}PFD	^{f}EXTCLK /(PLL_n_divider+1)	2	24	MHz
^{f}VCO	^{f}EXTCLK * PLL_m_factor/ (PLL_n_divider+1)	320	693	MHz

Maintaining a Constant Frame Rate

Maintaining a constant frame rate while continuing to have the ability to adjust certain parameters is often desired. This is not always possible, however, since register updates are synchronized to the read pointer, and the shutter pointer for a frame is usually active during the readout of the previous frame. Therefore, any register changes that could affect the row time or the set of rows sampled causes the shutter pointer to start over at the beginning of the next frame.

By default, the following register fields cause a "bubble" in the output rate (the vertical blank increases for one frame) if they are written in continuous mode, even if the new value would not change the resulting frame rate:

- Row_Start
- Row_Size
- Column_Size
- Horizontal_Blank
- Vertical_Blank
- Shutter_Delay
- Mirror_Row

The size of this bubble is (SW × ^{t}ROW), calculating the row time according to the new settings.

The Shutter_Width_Lower and Shutter_Width_Upper fields may be written without causing a bubble in the output rate under certain circumstances. Since the shutter sequence for the next frame often is active during the output of the current frame, this would not be possible without special provisions in the hardware. Writes to these registers take effect two frames after the frame they are written, which enables the shutter width to increase without interrupting the output or producing a corrupt frame (as long as the change in shutter width does not affect the frame time).

Synchronizing Register WRITEs to Frame Boundaries

Changes to most register fields that affect the size or brightness of an image take effect on the frame after the one during which they are written. To ensure that a register update takes effect on the next frame, the WRITE operation must be completed after the leading edge of FV and before the trailing edge of FV.

As a special case, in snapshot modes (see below), register WRITEs that occur after FV but before the next trigger will take effect immediately on the next frame, as if there had been a restart. However, if the trigger for the next frame in ERS snapshot mode occurs during FV, register WRITEs take effect as with continuous mode.

Additional control over the timing of register updates can be achieved by using synchronize_changes. If this bit is set, WRITEs to certain register fields that affect the brightness of the output image do not take effect immediately. Instead, the new value is remembered internally. When synchronize_changes is cleared, all the updates simultaneously take effect on the next frame (as if they had all been written the instant synchronize_changes was cleared). Fields not identified as being frame-synchronized or affected by synchronize_changes are updated immediately after the register write is completed. The effect of these registers on the next frame can be difficult to predict if they affect the shutter pointer.

Restart

To restart the MT9M032 at any time during the operation of the sensor, write a "1" to the restart register (R0x0B[0] = 1). This has two effects: first, the current frame is interrupted immediately. Second, any writes to frame-synchronized registers and the shutter width registers take effect immediately, and a new frame starts (in continuous mode). Register updates being held by synchronize_changes do not take effect until that bit is cleared. The current row and one following row complete before the new frame is started, so the time between issuing the restart and the beginning of the next frame can vary by about ^{t}ROW.

If pause_restart is set, rather than immediately beginning the next frame after a Restart in continuous mode, the sensor pauses at the beginning of the next frame until pause_restart is cleared. This can be used to achieve a deterministic time period from clearing the pause_restart bit to the beginning of the first frame, meaning that the controller does not need to be tightly synchronized to LV or FV.

Note: When pause_restart is cleared, be sure to leave the Restart register set to "1" for proper operation. The restart bit will be cleared automatically by the device.

Window Size

The output image window of the pixel array (the FOV) is programmable and defined by four register fields. Column_start and row_start define the X and Y coordinates of the upper left corner of the FOV. Column_size defines the width of the FOV, and row_size defines the height of the FOV in array pixels.

The column_start and row_start fields must be set to an even number. The column_size and row_size fields must be set to odd numbers (resulting in an even size for the FOV). The row_start register should be set no lower than 12 if either manual_BLC is cleared or show_dark_rows is set. The width of the output image, W, is *column_size + 1* and height, H, is *row_size + 1*. In default, a full resolution image size of 1440 x 1080 in output.

Image Acquisition Modes

The MT9M032 supports two image acquisition modes (shutter types): electronic rolling shutter (ERS), and global reset release (GRR).

Electronic Rolling Shutter

The ERS modes take pictures by scanning the rows of the sensor. On the first scan, each row is released from reset, starting the exposure. On the second scan, the row is sampled, processed, and returned to the reset state. The exposure for any row is therefore the time between the first and second scans. Each row is exposed for the same duration, but at slightly different point in time, which can cause a shear in moving subjects.

Whenever the mode is changed to an ERS mode (even from another ERS mode), and before the first frame following reset, there is an anti-blooming sequence where all rows are placed in reset. This sequence must complete before continuous readout begins.

This delay is:

$^{t}ALLRESET = 16 \times 1096 \times {}^{t}ACLK$ (where $^{t}ACLK$ is $2 * {}^{t}PIXCLK$)

Global Reset Release

The GRR modes attempt to address the shearing effect by starting exposures of all rows at the same time. Instead of the first scan used in ERS mode, the reset to each row is released simultaneously. The second scan occurs as normal, so the exposure time for each row would different. Typically, an external mechanical shutter would be used to stop the exposure of all rows simultaneously.

In GRR modes, there is a startup overhead before each frame as all rows are initially placed in the reset state (^{t}ALLRESET). Unlike ERS mode, this delay always occurs before each frame. However, it occurs as soon as possible after the preceding frame, so typically the time from trigger to the start of exposure does not include this delay. To ensure that this is the case, the first trigger must occur no sooner than ^{t}ALLRESET after the previous frame is read out.

Spectral Characteristics

Figure 9: Typical Color Spectral Characteristics

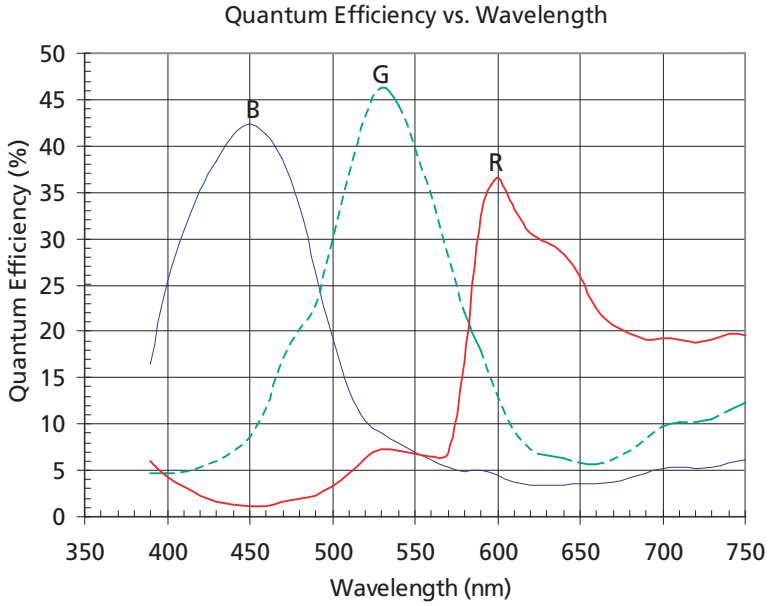
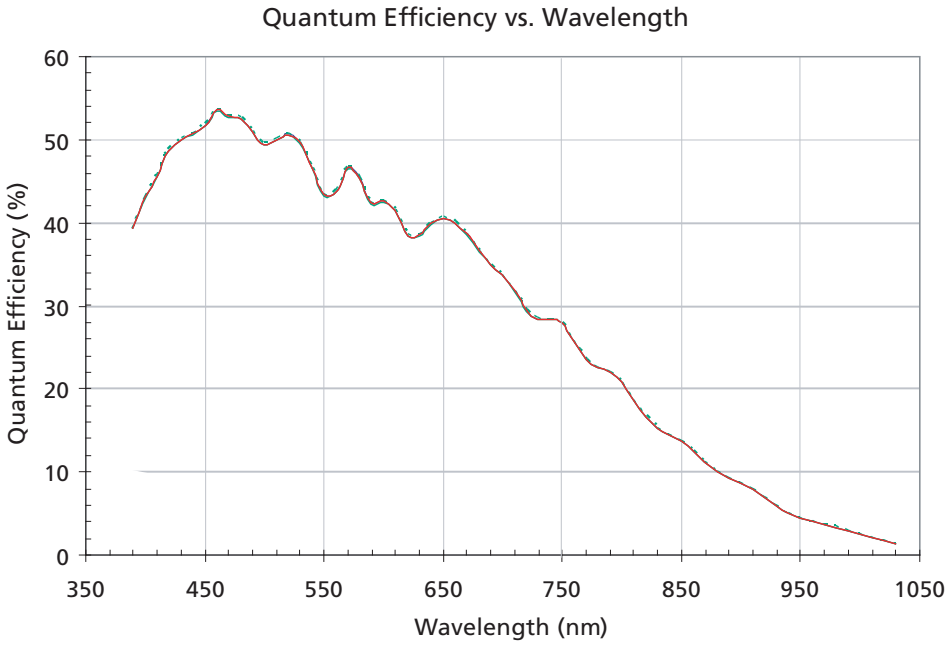


Figure 10: Typical Monochrome Spectral Characteristics



DC Electrical Characteristics

Table 7: DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.9	V
V_{DD_IO}	I/O digital voltage		2.6	2.8	3.1	V
V_{AA}	Analog voltage		2.6	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.6	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.6	2.8	3.1	V
V_{IH}	Input HIGH voltage	V_{DD_IO} = 2.8V				V
V_{IL}	Input LOW voltage	V_{DD_IO} = 2.8V				V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	–	<10		µA
V_{OH}	Output HIGH voltage	At specified I_{OH}				V
V_{OL}	Output LOW voltage	At specified I_{OL}				V
I_{OH}	Output HIGH current	At specified V_{OH}				mA
I_{OL}	Output LOW current	At specified V_{OL}		–		mA
I_{OZ}	Tri-state output leakage current	V_{IN} = V_{DD_IO} or GND	–			µA
I_{DD}	Digital operating current	Streaming, full resolution	–	28.0		mA
I_{DD_IO}	I/O digital operating current	Streaming, full resolution	–	27.3		mA
I_{AA}	Analog operating current	Streaming, full resolution	–	65.0		mA
I_{AA_PIX}	Pixel supply current	Streaming, full resolution	–	5.6		mA
I_{DD_PLL}	PLL supply current	Streaming, full resolution	–	3.0		mA
I_{STBY_A1}	Soft standby current	Clock off	–	0.21	–	mA
I_{STBY_B1}	Soft standby current	Clock off	–	32.31	–	mA
I_{STBY_A1}	Soft standby current	Clock off	–	0.21	–	mA
I_{STBY_B1}	Soft standby current	Clock off	–	28.41	–	mA

Table 8: Power Consumption - Parallel
at 30 fps, full resolution, 25°C

Symbol	Parameter	Typ Current (mA)	Typ Voltage (V)	Power Parallel (mW)
P_{VDD}	Digital operating power	28.0	1.8	50.4
P_{VDDIO1}	I/O digital operating power	7.7	2.8	21.6
P_{VDDIO2} (parallel)	I/O power parallel	19.6	2.8	86.5
P_{VAA}	Analog operating power	65.0	2.8	182.0
P_{VAAPIX}	PLL supply power	5.6	2.8	15.7
P_{VDDPLL}	PLL supply power	3.0	2.8	8.4
P_{TOTAL}	Total power			364.6

Absolute Maximum Ratings

Caution Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 9: Absolute Maximum Values

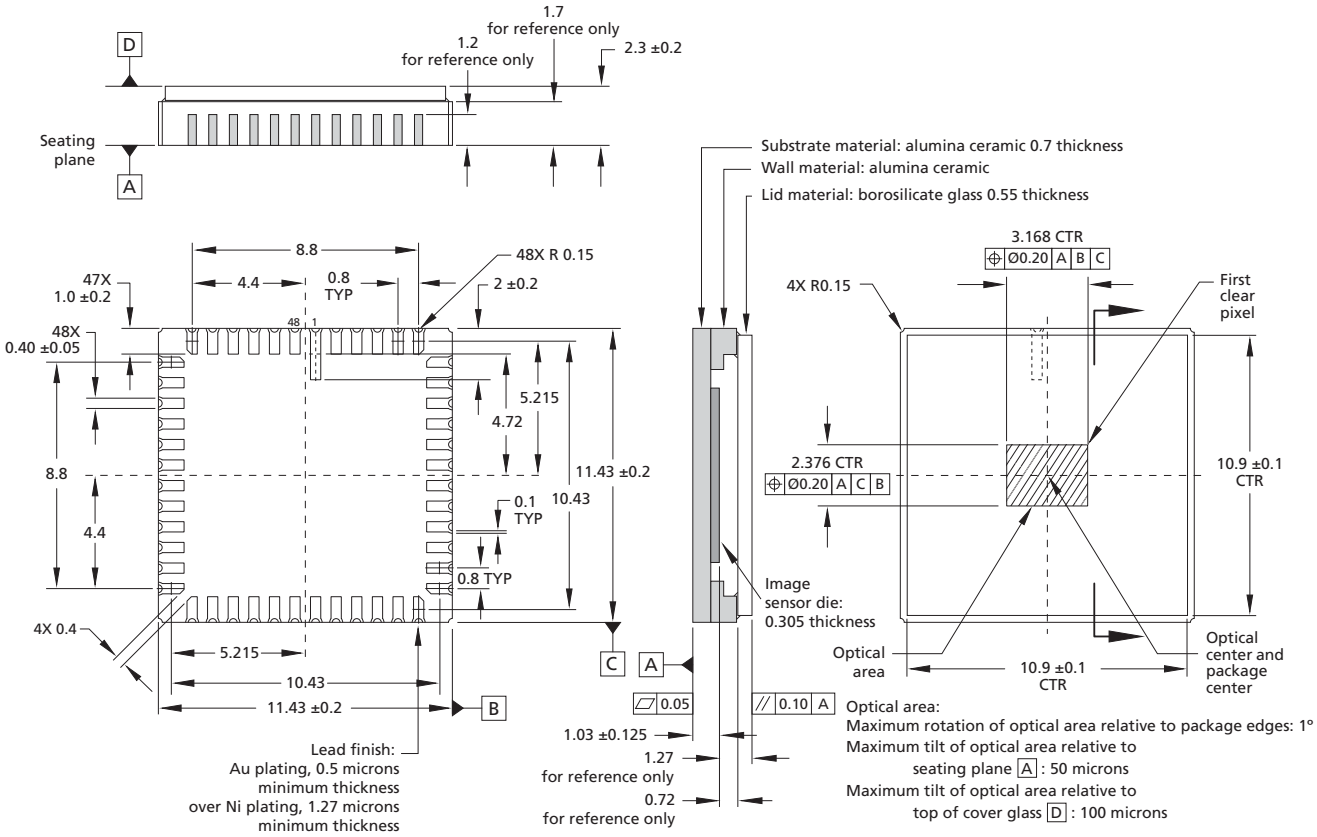
Symbol	Parameter	Condition	Min	Max	Unit
V_{DD_MAX}	Core digital voltage		–0.3	1.9	V
$V_{DD\_IO\_MAX}$	I/O digital voltage		–0.3	3.1	V
V_{AA_MAX}	Analog voltage		–0.3	3.1	V
$V_{AA\_PIX\_MAX}$	Pixel supply voltage		–0.3	3.1	V
$V_{DD\_PLL\_MAX}$	PLL supply voltage		–0.3	3.1	V
V_{IN_MAX}	Input HIGH voltage		–0.3	V_{DD_IO} + 0.3	V
I_{DD_MAX}	Digital operating current	Worst case current			mA
$I_{DD\_IO\_MAX}$	I/O digital operating current	Worst case current			mA
I_{AA_MAX}	Analog operating current	Worst case current			mA
$I_{AA\_PIX\_MAX}$	Pixel supply current	Worst case current			mA
$I_{DD\_PLL\_MAX}$	PLL supply current	Worst case current			mA
T_{OP}	Operating temperature	Measure at junction	–30	70	°C
T_{STG}	Storage temperature		–40	85	°C

Notes: 1. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Package Dimensions

The 48-pin CLCC package mechanical drawing is illustrated in Figure 11. The optical center is aligned with the package center as origin.

Figure 11: 48-Pin CLCC Package Outline



Notes: 1. All dimensions in millimeters.

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