NIS5101

Inrush Limiter/Circuit Breaker

The NIS5101 combines the control function and power FET into a single IC that saves design time and reduces the number of components required for a complete hot swap application. It is designed to allow safe insertion and removal of electronic equipment to −48 V backplanes. This chip features simplicity of use combined with an integrated solution.

The NIS5101 includes user selectable undervoltage and overvoltage lockout levels. It also has adjustable current limiting that can be reduced from the maximum level with a single resistor. Operation at the maximum current level requires no extra external components. An internal temperature shutdown circuit greatly increases the reliability of this device.

Features

- Integrated Power Device
- 100 V Operation
- Thermal Limit Protection
- Adjustable Current Limit
- No External Current Shunt Required
- Undervoltage and Overvoltage Lockouts
- 6.5 A Continuous Operation
- UIS Rated
- Main/Mirror MOSFET Current Ratio 820:1
- Pb−Free Packages are Available

Typical Applications

- VoIP (Voice over Internet Protocol) Servers
- −48 V Telecom Systems
- +24 V Wireless Base Station Power
- Central Office Switching
- Electronic Circuit Breaker

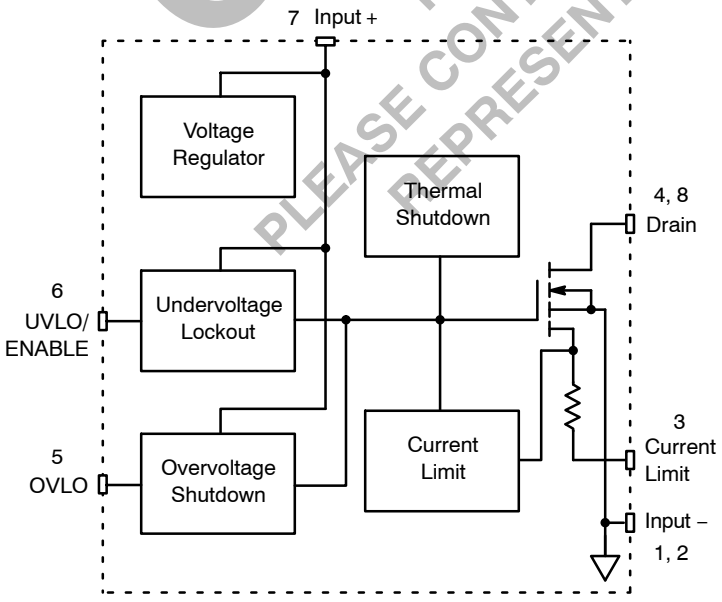
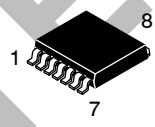


Figure 1. Block Diagram

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



S−PAK
EX SUFFIX
CASE 553AA

X = 1 for Thermal Latch or
2 for Thermal Auto−retry
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NIS5101E1T1	S−PAK Latch Off	2000 Units/Reel
NIS5101E1T1G	S−PAK Latch Off (Pb−Free)	2000 Units/Reel
NIS5101E2T1	S−PAK Auto−Retry	2000 Units/Reel
NIS5101E2T1G	S−PAK Auto−Retry (Pb−Free)	2000 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 2	Input −	Negative input voltage to the device. This is used as the internal reference for the IC.
3	Current Limit	This pin is shorted to the Input − pin for maximum current limit setting. If a reduced current limit level is desired, a series resistor is added between this pin and the Input − pin.
4, 8	Drain	Drain of power FET, which is also the switching node for the load.
5	OVLO	The overvoltage shutdown point is programmed by a resistor from this pin to the Input + supply.
6	UVLO/ENABLE	A resistor from Input + to the UVLO pin adjusts the voltage at which the device will turn on. An open drain device can be connected to this pin, which will inhibit operation, when in its low impedance state.
7	Input +	Positive input voltage to the device.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, Operating (Input + to Input −) Transient (1 second) Steady−State	V_{in}	 −0.3 to 110 −0.3 to 100	V
Drain Voltage, Operating (Drain to Input −) Transient (1 second) Steady−State	V_{DD}	 −0.3 to 110 −0.3 to 100	V
Drain Current, Continuous (T_A = 25°C, 2.0 in^2 Cu, double−sided board, 1 oz.)	I_{Davg}	6.5	A
Operating Temperature Range	T_j	−40 to 145	°C
Non−Operating Temperature Range	T_j	−55 to 175	°C
Lead Temperature, Soldering (10 Seconds)	T_L	260	°C
Drain Current, Peak (Internally Limited)	I_{pk}	20	A
Thermal Resistance, Junction−to−Air 0.5 in^2 copper 1.0 in^2 copper	$R_{\theta JA}$	 75 43	°C/W
Power Dissipation @ T_A = 25°C 0.5 in^2 copper 1.0 in^2 copper	P_{max}	 1.4 2.4	W
ESD Immunity for Device Handling (All Pins)	HBM JESD22−A114−B	2.0	kV
ESD Immunity Board Level (Note 1)	IEC 61000−4−2 (Level 3)	6.0	kV
Lightning, Surge (8 x 20 μsec) (Note 1)	IEC 61000−4−5 (Level 3)	2.0	kV
		48	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Applied between Input + and Input − pins only, and using an external 68 V bi−directional TVS device (P6SMB68AT3) connected across these pins.

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER FET					
Charging Time (Turn−On to Rated Max Current)	t_{chg}	–	5.0	–	ms
ON Resistance	R_{DSon}	–	43	50	mΩ
Zero Gate Voltage Drain Current (V_{DS} = 100 V_{dc}, V_{GS} = 0 V_{dc})	I_{DSS}	–	10	–	μA
Sense Voltage Tolerance (V_{input} = 48 V, RextI_{LIMIT} = 20 Ω)	V_{Sense}	–	3.0	–	%
Output Capacitance (V_{DS} = 48 V_{dc}, V_{GS} = 0 V_{dc}, f = 10 kHz)	–	–	326	–	pF
THERMAL LIMIT					
Shutdown Junction Temperature (Note 4)	T_{SD}	125	135	145	°C
Hysteresis (Note 4)	T_{hyst}	35	40	45	°C
OVER/UNDERVOLTAGE					
Turn−On Voltage (Rext$_{UVLO}$ = ∞)	V_{on}	41.5	46	50.5	V
Hysteresis (Rext$_{UVLO}$ = ∞)	V_{hyst}	6.3	8.0	9.7	V
Turn−On Voltage (Rext$_{UVLO}$ = 270 kΩ)	V_{on}	29	33	37	V
Hysteresis (Rext$_{UVLO}$ = 270 kΩ)	V_{hyst}	3.5	5.0	6.5	V
Zener Voltage (UVLO Pin Voltage at Turn−On)	V_Z	14.3	16	17.5	V
OVLO Threshold (Input + Increasing, Rext$_{OVLO}$ = ∞)	V_{OV}	100	–	–	V
OVLO Threshold (Input + Increasing, Rext$_{OVLO}$ = 300 kΩ)	V_{OV}	65	74	83	V
OVLO Hysteresis (Input + Decreasing, Rext$_{OVLO}$ = 300 kΩ)	V_{OVhyst}	3.0	4.7	6.4	V
CURRENT LIMIT					
Short Circuit Current Limit (RextI_{LIMIT} = 20 Ω) (Note 5)	I_{LIM1}	3.5	4.2	5.0	A
Overload Current Limit (RextI_{LIMIT} = 20 Ω) (Notes 4 and 5)	I_{LIM2}	5.4	6.0	6.6	A
TOTAL DEVICE					
Bias Current (Operational) (V_{input} = 48 V, R_{UVLO} = ∞)	I_{Bias}	–	1.4	–	mA
Bias Current (Non−Operational) (V_{input} = 30 V, R_{UVLO} = ∞)	I_{Bias}	–	800	–	μA
Minimum Operating Voltage (R_{UVLO} = 30 kΩ)	Vin_{min}	–	18	–	V

2. Pulse Test: Pulse width 300 μs, duty cycle 2%.
3. Switching characteristics are independent of operating junction temperatures.
4. Verified by design.
5. Please refer to explanation about the device's current limit operation in short circuit and overload conditions.

TYPICAL PERFORMANCE CURVES

(T_A = 25°C unless otherwise noted)

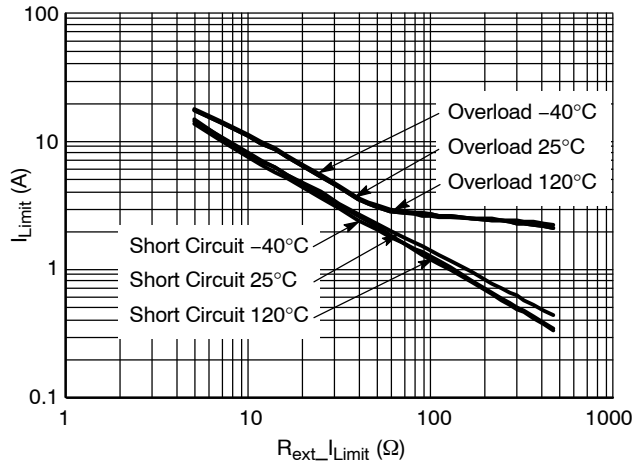


Figure 2. Current Limit Adjustment

(For Main/Mirror MOSFET Current Ratio explanation, see page 11)

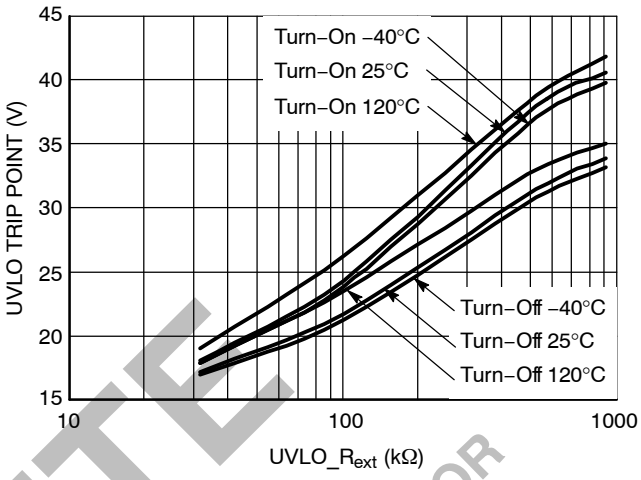


Figure 3. UVLO Adjustment

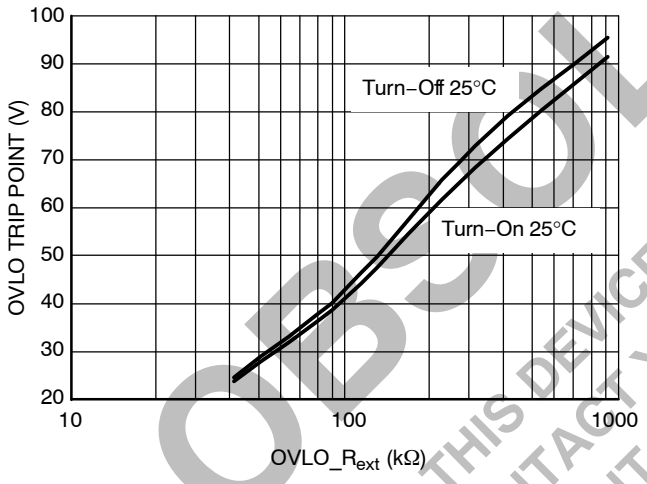


Figure 4. OVLO Adjustment, T_J = 25°C

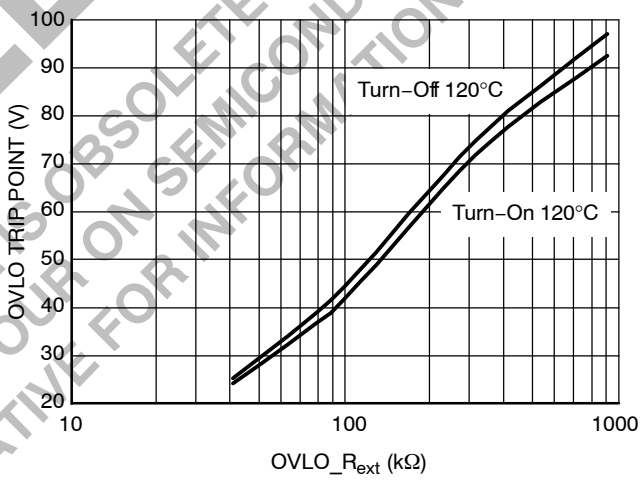


Figure 5. OVLO Adjustment, T_J = 120°C

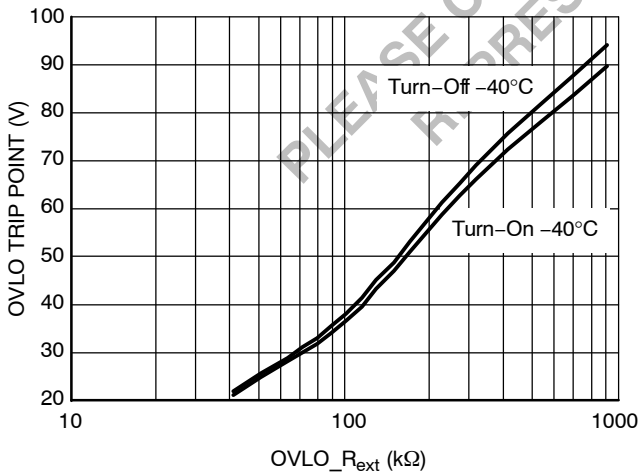


Figure 6. OVLO Adjustment, T_J = −40°C

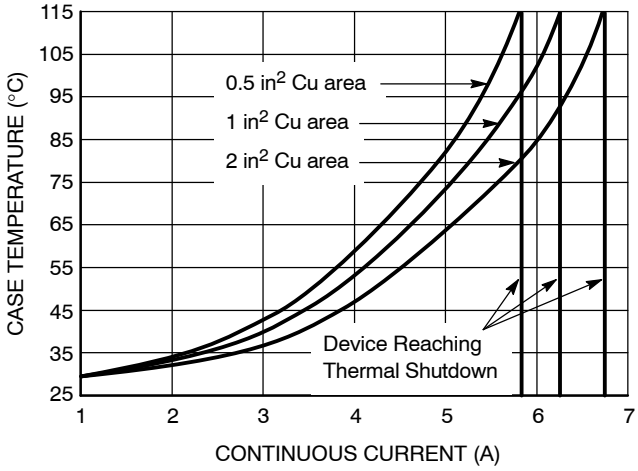


Figure 7. Continuous Current vs. Case Temperature

(Test performed on a double sided copper board, 1 oz)

TYPICAL APPLICATION CIRCUIT & OPERATION WAVEFORMS

(T_A = 25°C unless otherwise noted)

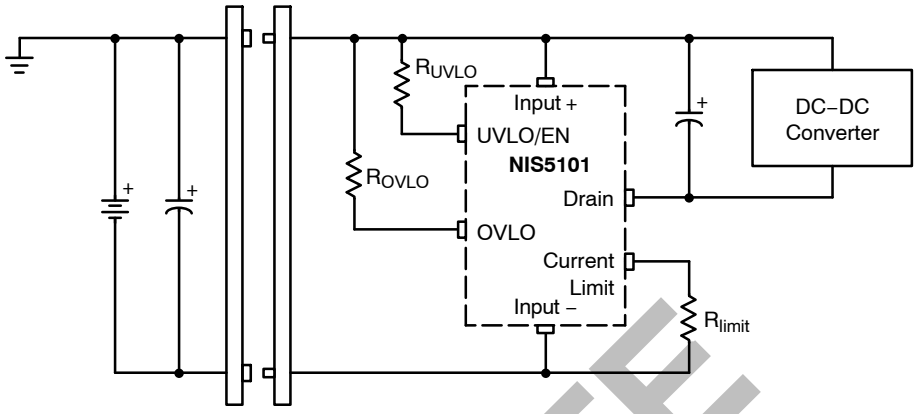


Figure 8. Typical Application

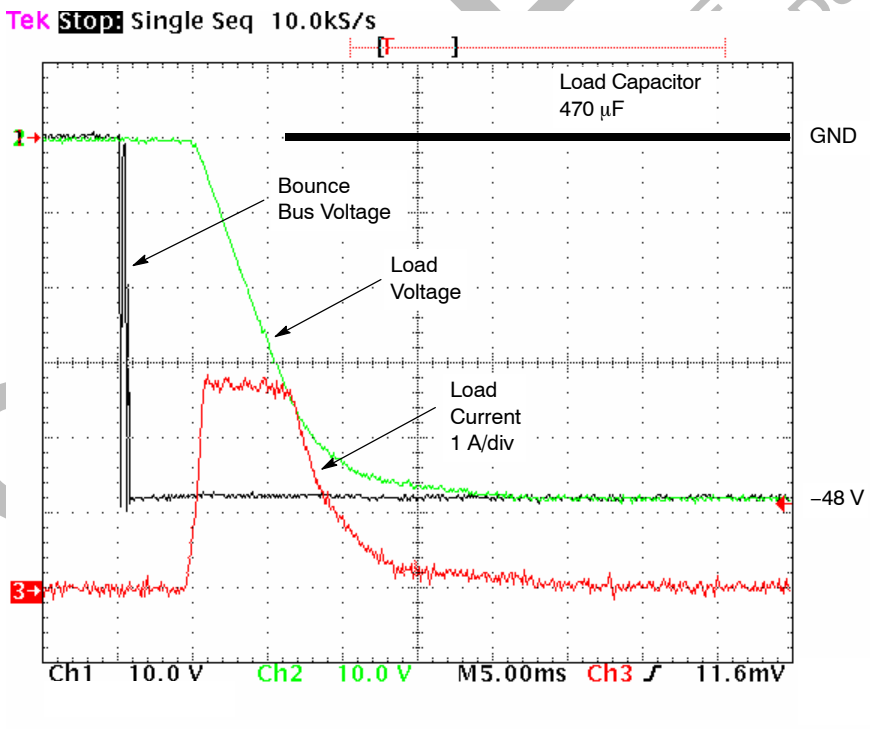


Figure 9. Turn On Waveforms for 470 μF Load Capacitor

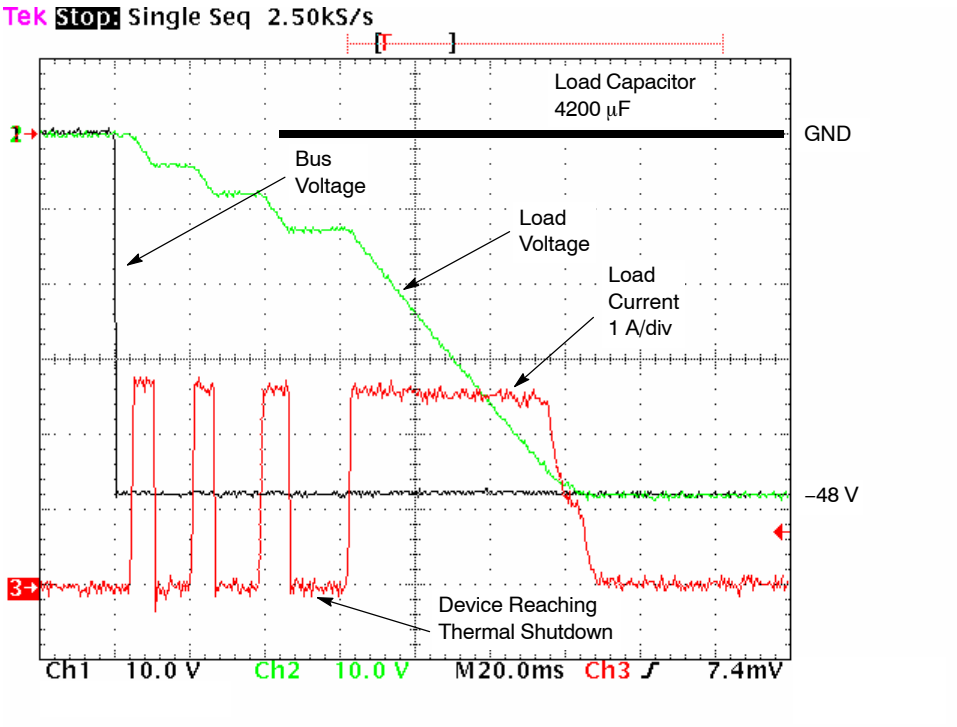


Figure 10. Typical Operation Waveforms of the Auto−Retry Device

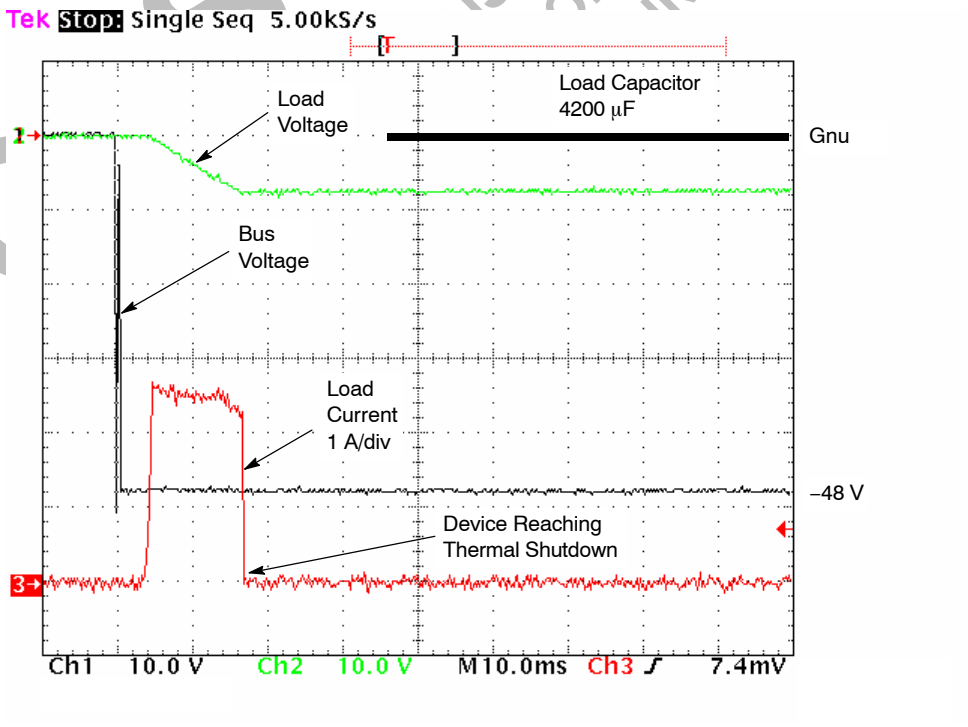


Figure 11. Typical Operation Waveforms of the Latch Off Device

ADDITIONAL APPLICATION CIRCUITS FOR DIFFERENT FUNCTIONS

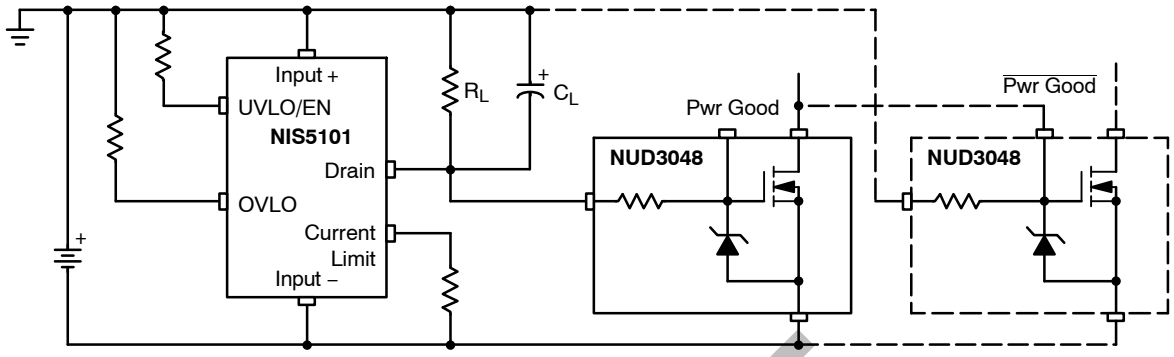


Figure 12. Power Good Signal Circuit

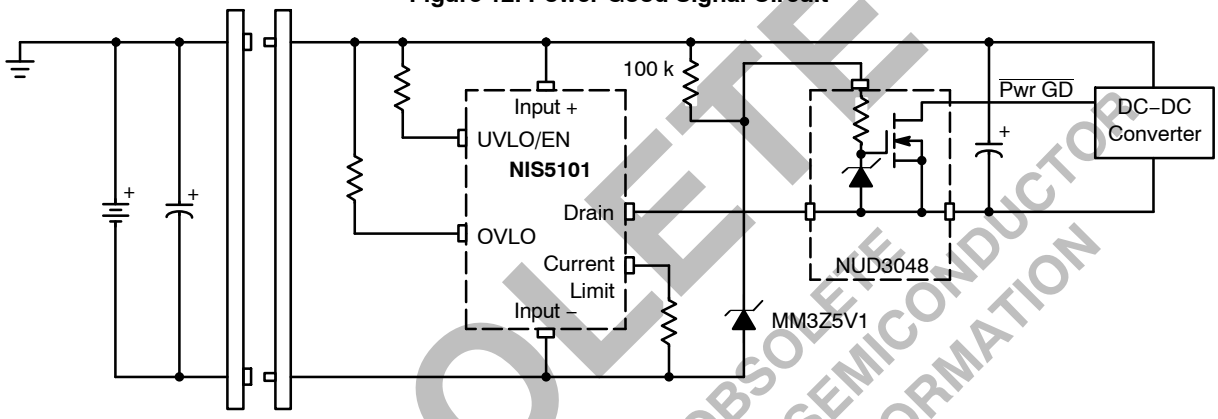
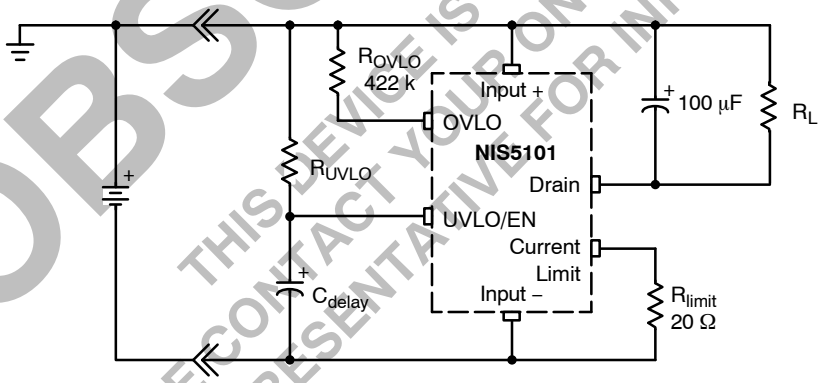


Figure 13. Power Good Signal Referenced to Drain



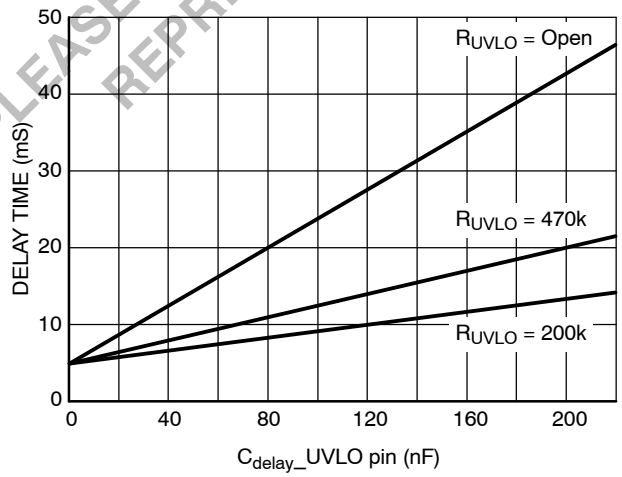


Figure 14. Increased Delay Time Circuit

TYPICAL DEVICE PERFORMANCE FOR DIFFERENT SYSTEM INDUCTANCE VALUES

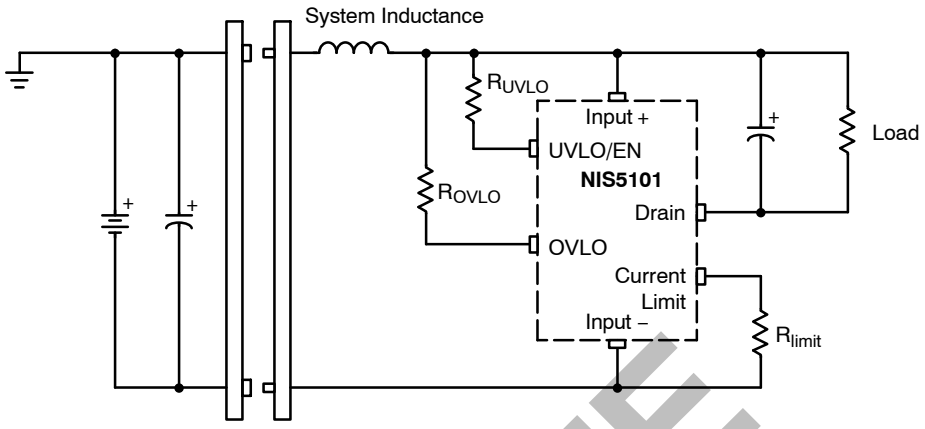


Figure 15. System Inductance Test Circuit

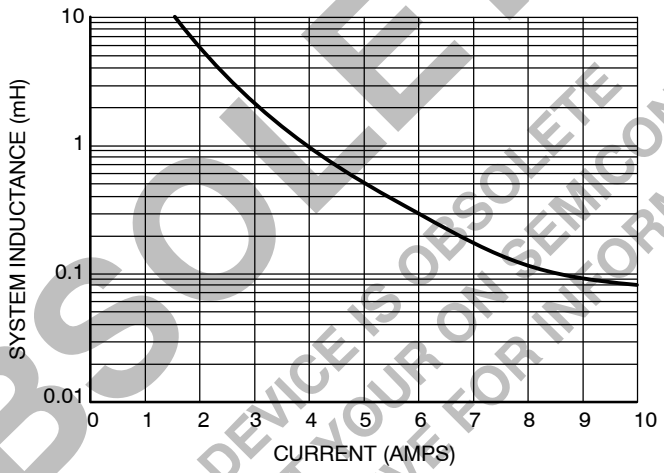


Figure 16. Total System Inductance vs. Current

OPERATION DESCRIPTION

Turn−on

The NIS5101 monitors the input voltage by sensing the voltage across the Input + to Input − pins. When the UVLO voltage has been reached, the internal circuitry slowly charges the gate of the internal SENSEFET®. There will be a slight delay of several milliseconds before the SENSEFET begins conduction. This may be increased by adding a capacitor to the UVLO pin. For a discussion of this, see application note AND8115/D.

The SENSEFET will increase the load current with a controlled di/dt until the current limit level has been reached. At this point the SENSEFET will enter a constant current mode of operation until the load capacitor has been fully charged. If the thermal limit threshold is reached before the capacitor reaches its final charge level, the device will shut down until the die temperature reaches 95°C and then restart, if it is the auto−retry device. The thermal latching version must not be allowed to reach the thermal shutdown level at turn−on as this will cause it to latch in an off state.

During the capacitor charging period, the dv/dt of the capacitor is:

$$dv/dt = \frac{I_{LIMIT}}{C_{LOAD}}$$

Faults

Once the load capacitance is charged, the SENSEFET will become fully enhanced as long as the current does not reach the current limit threshold, or is shut−down due to an overvoltage, undervoltage or thermal fault. Both the UVLO and OVLO circuits incorporate hysteresis to assure clean turn−on and turn−offs with no chatter. The thermal latching circuit will require the input power to be recycled to resume operation after a fault. The current limit is always active, so any transient or overload will always be limited.

Circuit Description

Undervoltage Lockout: The UVLO circuit holds the chip off when the input voltage is less than the turn−on limit. It includes internal hysteresis to assure clean on/off switching. An internal divider sets the turn−on voltage level at 46 V. This voltage can be reduced by adding an external resistor from the UVLO pin to the Input + pin. The equivalent circuit is shown in Figure 17.

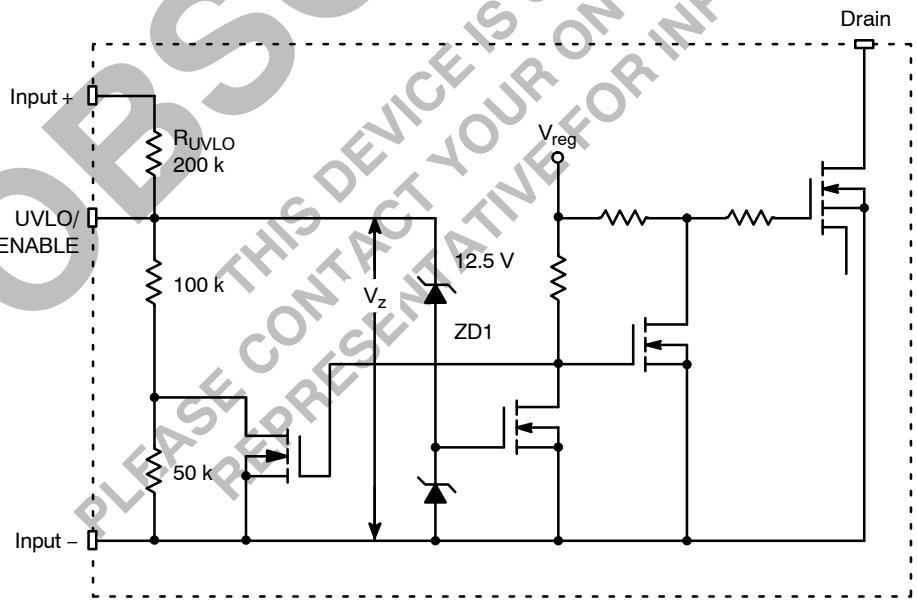


Figure 17. Undervoltage Lockout Circuit

The theoretical equation for the UVLO turn−on voltage is:

$$R_{UVLO}\ (k\Omega) = \frac{215\ V_{in} - 2970}{46.8 - V_{in}}$$

Where V_{in} is the desired turn−on voltage, and R_{UVLO} is the programming resistance from the UVLO pin to the Input + pin.

The UVLO trip point voltage calculated through the theoretical formula may show small variations with respect to Figure 3, therefore it is recommended to use the formulas gotten from the UVLO characterization, which are shown below:

$R_{UVLO}\ (k\Omega) = e^{[(y+4.4706)\ /\ 6.4484]}$; for $T_J = 25°C$

$R_{UVLO}\ (k\Omega) = e^{[(y+4.6185)\ /\ 6.8525]}$; for $T_J = 120°C$

$R_{UVLO}\ (k\Omega) = e^{[(y+5.7642)\ /\ 6.7234]}$; for $T_J = -40°C$

where “y” is the desired UVLO value.

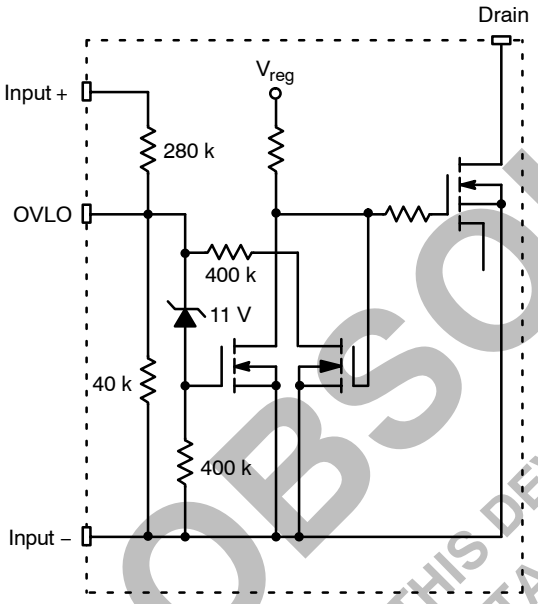


Figure 18. Overvoltage Lockout Circuit

To reduce nuisance tripping due to transients and noise spikes, a capacitor may be added from the UVLO pin to the Input – pin. This will create a low pass filter with a cutoff frequency of f. The required capacitance on this pin is:

$$C = \frac{1}{2\pi \cdot f\left[150\ k + \left(\frac{R_{UVLO} \cdot 200\ k}{R_{UVLO} + 200\ k}\right)\right]}$$

Overvoltage Lockout: The overvoltage shutdown circuit is an optional protection feature that can be disabled by simply grounding the OVLO pin.

This circuit contains an internal Zener diode/resistor combination in series with the gate of a FET. When the input + to input − voltage reaches a level sufficient to apply the required gate voltage to the FET, operation of the device will be inhibited. There is a hysteresis circuit built in that will eliminate on/off bursts due to noise on the input. The equivalent circuit is shown in Figure 18.

The equation for the OVLO trip point is:

$$R_{OVLO}\ (k\Omega) = \frac{290\ V_{in} - 3200}{113.7 - V_{in}}$$

Where R_{OVLO} is the overvoltage programming resistor from the OVLO pin to Input +, and V_{in} is the desired trip point for the overvoltage shutdown to occur.

The OVLO trip point voltage calculated through the theoretical formula may show small variations with respect to Figures 4, 5 and 6, therefore it is recommended to use the formulas gotten from the OVLO characterization, which are shown below:

$R_{OVLO}\ (k\Omega) = e^{[(y+69.6)\ /\ 24.82]}$; for $T_J = 25°C$

$R_{OVLO}\ (k\Omega) = e^{[(y+60.56)\ /\ 23.27]}$; for $T_J = 120°C$

$R_{OVLO}\ (k\Omega) = e^{[(y+66.47)\ /\ 23.52]}$; for $T_J = -40°C$

where “y” is the desired OVLO value.

Similar to the undervoltage lockout circuit, the noise sensitivity of this circuit can be reduced by adding a capacitor from the OVLO pin to Input −. The capacitor required for the desired pole frequency is:

$$C_{OVLO} = \frac{(1 + 31.3 \cdot 10^{-6} \cdot R_{OVLO})}{2\pi f \cdot R_{OVLO}}$$

Temperature Limit: The temperature limit circuit senses the temperature of the Power FET and removes the gate drive if the maximum level is exceeded. There is a nominal hysteresis of 40°C for this circuit. After a thermal shutdown, the device will automatically restart when the temperature drops to a safe level as determined by the hysteresis.

Current Limit: The device uses a SENSEFET to measure the Drain Current. The behavior of the SENSEFET in a short circuit condition varies from that in an overload because there is sufficient voltage across the drain to source terminals for the sense current to follow the ratio of the sense cells to main FET cells. This is not the case when the device is fully enhanced, since there are only a few millivolts from drain to source. In this condition, the sense voltage follows a different set of equations.

An overload condition is one in which the FET is fully enhanced and operating at it's minimum R_{DSon}. A short circuit condition occurs when either the load has shorted or upon turn on, as the load capacitor to the hot swap device initially looks like a short circuit.

A single resistor will determine both the short circuit and overload current. For example, a 110 Ω resistor would result in a 1 A current limit when charging the capacitance at turn on, but once the FET is fully enhanced, it would allow the load to operate at a current up to 2.5 A. Once the 2.5 A limit is reached, any further reduction in load impedance will result in a short circuit condition and the current will be reduced to 1 amp.

The current limit will never shut down the limiter. Only the thermal limit will stop the flow of current to the load. Once the current is stopped due to the thermal limit, it will remain off until input power is recycled for the latching version, or it will continuously retry to start again if it is the auto−retry version.

The I_{Limit} graph shown in Figure 2 was generated from the data of the I_{Limit} characterization, the formulas for each of the curves and temperatures are shown below:

R_{ILimit} (Ω) = $(56.55 / y)^{1.20}$; for T_J = 25C

R_{ILimit} (Ω) = $(52.91 / y)^{1.22}$; for T_J = 120°C

R_{ILimit} (Ω) = $(44.80 / y)^{1.33}$; for T_J = −40°C

where "y" is the desired ILimit value.

Main/Mirror MOSFET Current Ratio. The ratio varies with current and sense resistance. The key parameter that it is important to know is that the current sense reference voltage of the device is 50 mV. Knowing this information, it is possible to use Figure 2 on the datasheet for the current limit to calculate the ratio for any condition.

For "normal" operating condition, the overload curve would apply. If a 100 Ω for the I_{Limit} resistor is used, the sense current would be 50 mV/ 100 Ω at the current limit level, which results in 500 μA. The drain current is 2.7 A under this condition, so the ratio is 5400:1.

Same analysis can be made for "short circuit" conditions, the only difference is that the short circuit curve of Figure 2 is used to do the ratio calculations instead.

There is a 5 Ω resistor in series with the sense cells. This has a tolerance of about 10% and should be taken into account when making the above calculations.

Turn−onSurge: During the turn−on event, there is a large amount of energy dissipated due to the linear operation of the power device. The energy rating is the amount of energy that the device can absorb before the thermal limit circuit will shut the unit down. This is very important specially for the latch off device as it determines the maximum load capacitance that the device can charge before the thermal limit shuts the device down. The calculation of this is not very simple as it depends on several factors such as the input voltage (V_{in}), load capacitance (C_L), current limit settings (I_{Limit}) and device's thermal transient response, therefore, it is recommended to do lab evaluations for these purposes. Figure 19 shows the device's thermal transient response for minimum pad.

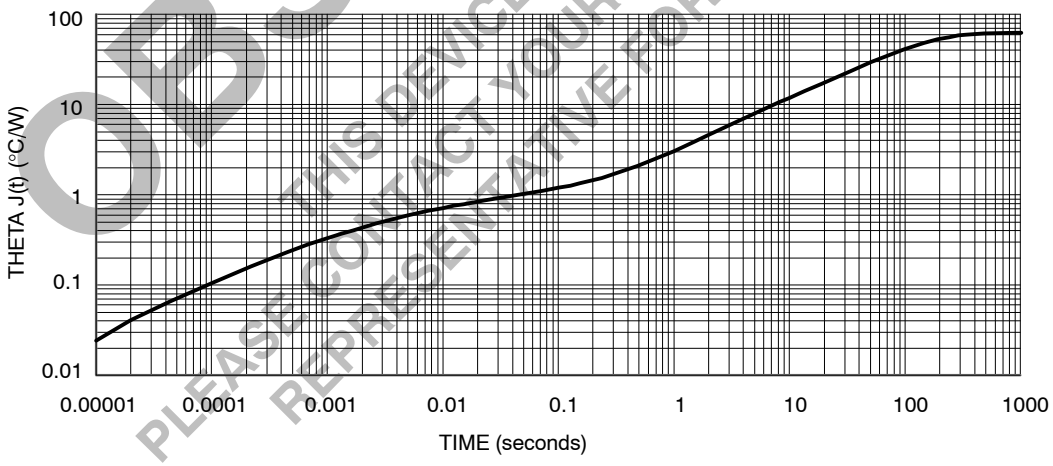
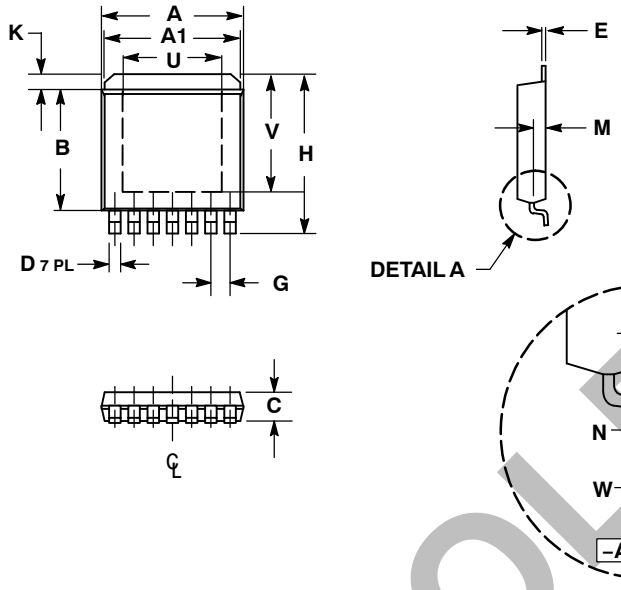


Figure 19. Thermal Transient Response

PACKAGE DIMENSIONS

S−PAK−7
EX SUFFIX
CASE 553AA−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010 BSC		0.25 BSC	
G	0.050 BSC		1.27 BSC	
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010 BSC		0.25 BSC	
P	0.031	0.041	0.79	1.04
R	0 °	6 °	0 °	6 °
U	0.256 BCS		6.50 BSC	
V	0.316 BSC		8.03 BSC	
W	0.010 BSC		0.25 BSC	

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PUBLICATION ORDERING INFORMATION

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