# ORCA ORT82G5 Evaluation Board

***Evaluate 3.7Gbps SERDES + FPGA Quickly and Easily***

## *Making the Right Choice...*

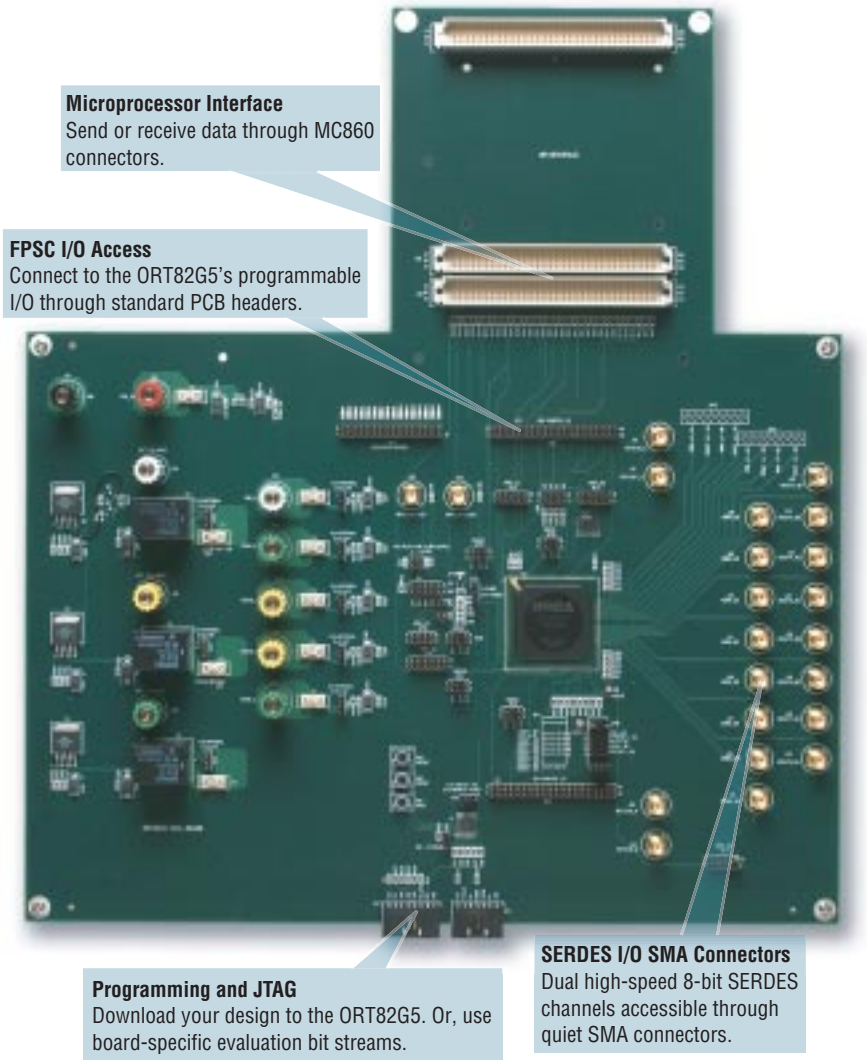
Choosing the right device to drive 3.7Gbits/s data over your backplane can be a critical decision, but evaluating your options shouldn't be complicated. Lattice has created the ORCA® ORT82G5 Evaluation Board so you can efficiently test the characteristics of a 3.7Gbits/s data stream generated by Lattice's ORT82G5 FPSC.

## *Examine Features Such as:*

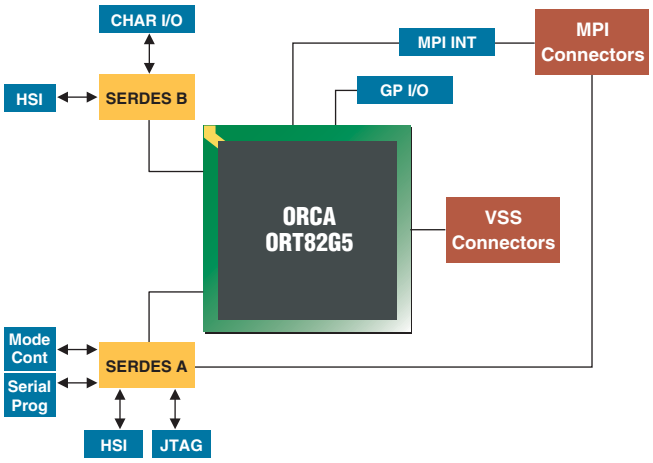
- Field Programmable System Chip (FPSC) flexibility and features
- ORT82G5 SERDES functionality and performance
- Programmable I/O capabilities
- Output strength and clarity
- Compliance to data transmission standards, from fiber channel to 10Gbit Ethernet (XAUI)

## *Working on an ORT82G5 Application?*

Use the ORT82G5 Evaluation Board to help develop your application in an established and flexible environment. Download your design to the ORT82G5 for instant feedback.

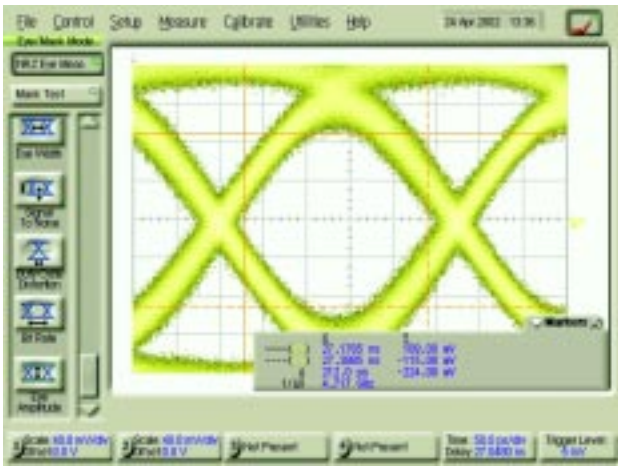



## *ORT82G5 Evaluation Board Block Diagram*




## *Full Feature Set*

- Push-button switches assert/de-assert the logic levels on the FPGA PRGMN, PRESET, and the SERDES reset.
- Interconnect test points for SERDES characterization.
- SMA connectors for differential inputs to the ORT82G5's four on-chip PLLs.
- Independent power supplies for the board and SERDES I/O.
- Downloadable programming bit streams are available from www.latticesemi.com for testing specific functions of the ORT82G5.



## About the ORCA ORT82G5...

Lattice's ORT82G5 is a Field Programmable System Chip is based on the ORCA Series 4 architecture. The ORT82G5 integrates eight 3.7Gbits/s backplane transceiver channels and a full-duplex synchronous interface with built-in Clock and Data Recovery with a flexible FPGA logic core.

- **Eight channels at 1.25 to 3.7 Gbits/s, exceeds XAUI specifications for 10Gbits/s Ethernet applications**
- **Optional 8b/10b encoding/decoding support on all channels**
- **Multi-channel alignment FIFOs available in 8b/10b mode**
- **More than 400K of usable FPGA gates, internal performance of >250MHz**
- **Four programmable PLLs**
- **Two extra embedded 4Kx36 dual-port RAM blocks**
- **Programmable I/O with programmable drive and slew rate control supports LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL/3, HSTL, ZBT, DDR, LVDS, BLVDS and LVPECL**
- **372 programmable user I/O**

See www.latticesemi.com for complete specifications of the ORT82G5

## ispLEVER™ Development Tools

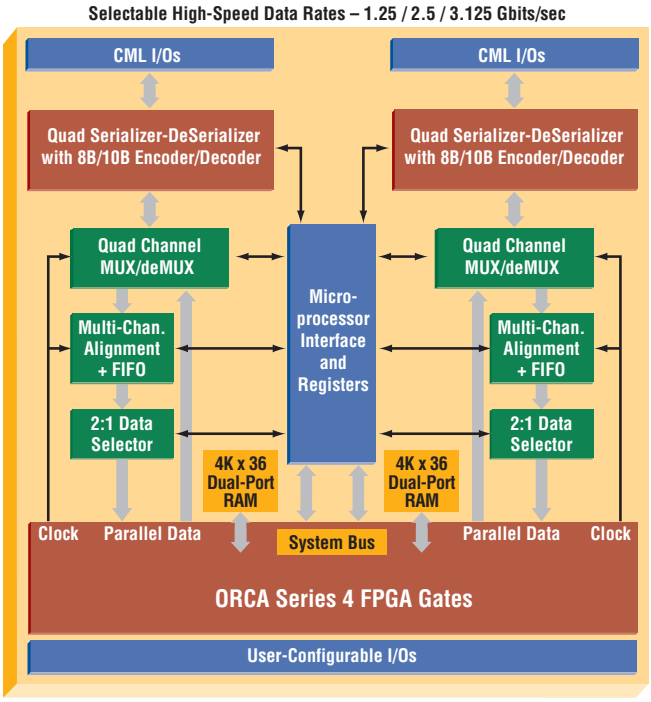
ispLEVER is an integrated software sysem for the development of all Lattice programmable logic devices, including the ORT82G5. The ispLEVER software incorporates ASIC design techniques and FPGA development methodologies that meet today's high-speed design demands.


## Clear Your Eyes With the ORT82G5!

With data wavelengths now shorter than your backplane, clean and reliable signals are crucial. The ORT82G5 provides I/O capabilities that exceed today's tight standards. The ORT82G5 also features programmable pre-emphasis for transmission of reliable low-jitter SERDES signals, giving you more flexibility in applications utilizing Clock and Data Recovery (CDR).

With the ORT82G5 Evaluation board, you can measure the I/O performance of the ORT82G5 in an environment you control. The signal to the left is the actual data-eye of a 3.7Gbps SERDES transmission across 26 inches of FR-4 backplane, generated by the ORT82G5 using 25% pre-emphasis.

## ORCA ORT82G5 Block Diagram




- **Included with the ORT82G5 Evaluation Board:**
  - ORT82G5-2BM680 device
  - ORCA download cable
  - Board schematic and bill of materials
- **Available on www.latticesemi.com:**
  - ORT82G5 Eval Board User Manual and Tutorial
  - IBIS and HSPICE models, and BSDL files
  - Schematic and Gerber files
  - Evaluation bit streams

**Applications Support**
1-800-LATTICE (528-8423)
(408) 826-6002
techsupport@latticesemi.com

Lattice Semiconductor Corporation
www.latticesemi.com

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