Actel
POWER MATTERS

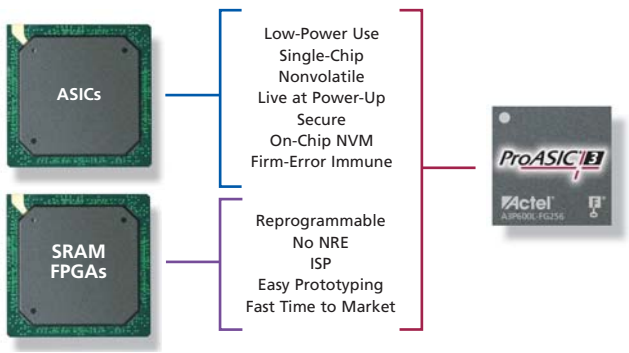
ProASIC®3

THE INDUSTRY'S **LOW-POWER FPGAs**

Key Features

- Lowest-Cost FPGA, Starting at $0.49
- Static Power as Low as 330 µW
- 40% Reduction in Dynamic Power (relative to 1.5 V) with 1.2 V Support
- Ultra-Low-Power Flash*Freeze Support
- Optimized for High Performance
- Free ARM Cortex-M1 (ARM FPGA processor) Support for All Devices
- Cost-Optimized, Reprogrammable, and Nonvolatile
- 1,024 Bits of User Flash Memory
- Single-Chip and Live at Power-Up
- In-System Programming (ISP) with Optional On-Chip AES Decryption
- Firm-Error Immune

The ProASIC3 families of flash FPGAs offer a breakthrough in power, price, performance, density, and features for today's most demanding high-volume applications. ProASIC3 devices support the ARM7™ and ARM® Cortex™-M1 soft processor IP cores, offering the benefits of programmability and time-to-market at costs as low as $0.49. The ProASIC3 families are based on nonvolatile flash technology and support 10 k to 3 M gates and up to 620 high-performance I/Os.



Flash FPGA Advantages that Extend Beyond Performance and Cost

Based on true flash technology, ProASIC3 family FPGAs offer industry-leading low power and high performance in a low-cost solution.

Low Power

The Actel flash-based ProASIC3 devices exhibit industry-leading low-power characteristics, making them an ideal choice for battery-operated and other power-sensitive applications. With an offering of a low density, 10 k system gate FPGA for $0.49, low-power benefits can now be coupled with low price. Unlike SRAM FPGAs, ProASIC3 devices exhibit no power-on current surge and conform to industry-leading power specifications. With the introduction of ProASIC3L devices, which have a wide operating range from 1.2 V to 1.5 V, Actel continues to address stringent power budgets with leadership in both static and dynamic power consumption.

Static Power is defined as power consumption of the device in a quiescent state, and is a result of transistor leakage. While ProASIC3/E devices offer power savings, the 1.2 V core operation of ProASIC3L devices supports additional savings of up to 90 percent.

Dynamic Power claims the dominant portion of the power budget today. To address the increasing device density requirements and the growing demand for high performance with low power, Actel presents the ProASIC3L family, which offers 40 percent savings with the 1.2 V core voltage versus the 1.5 V ProASIC3 core voltage. Additionally, its state-of-the-art Flash*Freeze pin instantaneously switches from active to static mode, eliminating the need for additional circuitry to turn off the clocks or I/Os, and thereby simplifying power management on boards.

Based on a low-power, 130 nm, true flash-based nonvolatile memory process, the third generation of Actel flash devices includes ProASIC3/E and low-power ProASIC3L. These devices combine performance and industry-leading power savings, and are a live-at-power-up, single-chip, secure solution. These reprogrammable devices offer high performance, enabling system designers to make smart choices based on density, performance, cost, and power budgets. In addition, the ProASIC3E family offers extended I/O feature support and up to six on-board phase-locked loops (PLLs). ProASIC3E and ProASIC3L devices support 504 kbits of true dual-port SRAM and up to 620 user I/Os. Free ARM Cortex-M1 support is provided for all devices.

Single Chip

Actel's programmable logic solutions do not require additional nonvolatile memory in order to load the device configuration data at every system power-up, which reduces cost and increases security and system reliability.

Live at Power-Up

Actel's programmable logic devices, based on nonvolatile memory technologies, store their configuration in the logic gates, making the devices available to perform critical system setup tasks such as system configuration and supervision during voltage ramp-up. Additionally, rapid operation from ultra-low-power Sleep mode is possible—typically less than 25 µW, even for 3 M system gates.

Secure

Actel's portfolio of nonvolatile FPGAs offers virtually unbreakable design security to meet your most demanding design requirements. Once programmed, the devices are inherently nonvolatile, enabling them to retain their configuration internally on the chip. This means that there is no external bitstream susceptible to interception.

Neutron Immune

Actel offers extremely reliable antifuse and flash FPGAs that are immune to configuration upsets due to neutron and alpha radiation.

ProASIC3 nano—Lowest Cost Solution with Enhanced I/O Functionality

Globalization and removal of trade barriers have led to increased competition in the manufacturing and marketing of electronic devices. Actel's ProASIC3 nano devices are specifically optimized for consumer, industrial, medical, and other high-volume, cost-sensitive applications. Reduced device cost, availability of Known Good Die, a single-chip implementation, and a broad selection of small-footprint packages all contribute to lower total system costs. Advanced packaging enables devices to utilize existing pick and place machines as well as standard low-cost board assembly procedures, using packages as small as 6 x 6 mm. In most cases, all of these small-footprint packages are routable with two-layer boards, reducing both material and labor costs.

Enhanced I/O functionality ensures multiple standards with mixed voltage levels typically found in power-sensitive or battery-powered designs can be addressed with a single device. ProASIC3 nano devices support Schmitt trigger inputs and are hot-swappable. The Schmitt trigger input delivers greater noise immunity in the circuit, enabling designers to safely identify an input signal that rises slowly, such as a keyboard or touchpad. The hot-swap capability offers designers the flexibility to maintain direct system connection while powering up.

When measured against the typical project metrics of performance, cost, flexibility, and time-to-market, the ProASIC3 nano devices provide an attractive alternative to ASICs and application-specific standard products (ASSPs) in fast moving or highly competitive markets. Configurable "on the fly" through insystem programming (ISP) of the flash-based fabric, enables value-added enhancements and product differentiation to be made or allows the end device to adapt to changing standards.

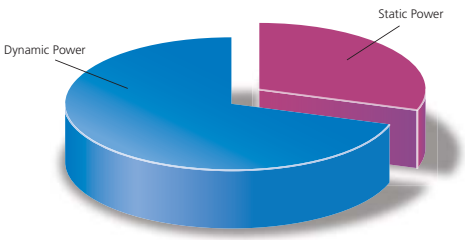
ProASIC3L—Offering Low Power, High Performance, and Low Cost

Featuring 40 percent lower dynamic power and 90 percent lower static power than its previous-generation ProASIC3 FPGAs, and orders of magnitude lower power than SRAM competitors, ProASIC3L combines dramatically reduced power consumption with up to 350 MHz operation. The ProASIC3L family supports an FPGA-optimized, 32-bit ARM Cortex-M1 processor, allowing system designers to select the Actel flash FPGA solution that best meets their speed and power design requirements. Combined with optimized software tools using Power-Driven Layout (PDL), this provides instant power reduction capabilities.

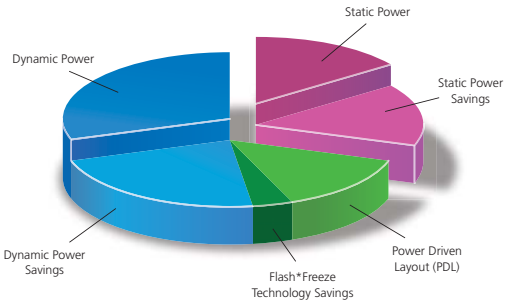
ProASIC3L devices incorporate proven Flash*Freeze technology, which allows fast switching (within 1 µs) from an active to a static state. No additional components are required to switch from or to these states, thereby eliminating the need for additional I/O or clock management circuits. This capability makes dynamic power reduction possible by quickly switching the device in and out of Flash*Freeze mode during periods of inactivity. A ProASIC3L device can operate from a single voltage (ranging from 1.2 V to 1.5 V core supply) and offers secure in-system programming (ISP) for valuable field programming upgrades.

The ProASIC3L family supports up to 3 M system gates with advanced I/O options, user nonvolatile memory, Level 0 live-at-power-up (LAPU) support, and the industry's most secured AES encryption capability.

FPGA Design at 1.5 V



FPGA Design at 1.2 V



ProASIC 3—Actel's Third-Generation Flash FPGA Architecture

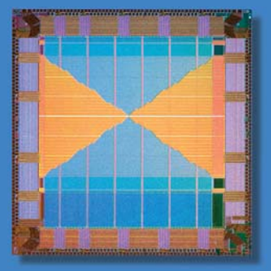
1 Flash*Freeze

(only supported by ProASIC3L devices)

Flash*Freeze enables ProASIC3L devices to switch between active and static states instantaneously within 1 µs. This feature simplifies power management so there is no need to turn off power supplies or clocks at the system level and the device retains register and SRAM content while in Flash*Freeze mode.

2 VersaTile

The ProASIC3 low-power VersaTile elements allow synthesis and mapping tools to use any tile as a three-input lookup table equivalent, a D-flip-flop, or latch (with or without enable). ProASIC3 devices with VersaTiles offer an abundance of registers so you can often choose a smaller device and still meet register requirements.

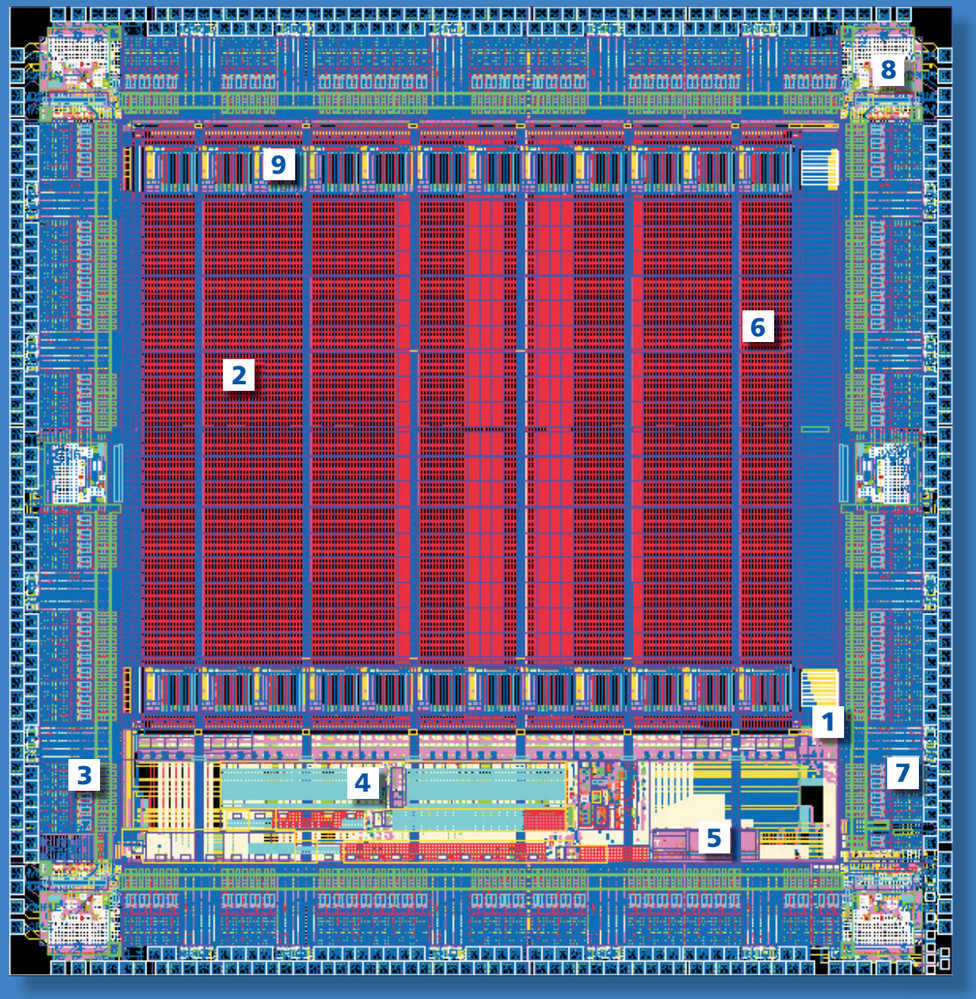


Extensive power bussing gives ProASIC3 micro-photography its distinctive "bow tie" appearance.

3 Advanced I/O Standards

ProASIC3 devices support up to 19 advanced I/O standards:

- Cold-sparing I/Os
- 700 Mbps LVDS-capable DDR I/Os
- Up to 8 different I/O banks per chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V (ProASIC3L only), 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V input
- Differential I/O Standards: LVPECL and LVDS, BLVDS, M-LVDS support
- Voltage-Referenced I/O Standards (ProASIC3E and ProASIC3L only): GTL+2.5 V / 3.3 V, GTL2.5 V / 3.3 V, HSTL Class 1 and 2, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
- Registered I/Os
- Hot-swap compliant I/Os
- Programmable slew rate and drive strength on outputs
- Programmable delay, weak pull-up/down
- Schmitt trigger option on inputs (ProASIC3 nano and ProASIC3E/L only)
- Pin compatibility across a given package



4 Charge Pumps

ProASIC3 devices can be programmed from a single 3.3 V supply voltage. If remote programming is not required, ProASIC3 devices can be run off a single 1.5 V supply, whereas ProASIC3L has a wide operating range from 1.2 V to 1.5 V on the core supply voltage.

5 FlashROM

ProASIC3 flash FPGAs include user flash memory. One kbit of flash memory, arranged in eight 128-bit pages, allows for diverse applications support, such as device serialization, secure application key storage, revision control, and selective feature enabling.

6 Routing Structure

ProASIC3 provides millions of flash cell switches and an abundance of hierarchical routing resources, enabling extensive design and routing flexibility.

VersaNet (segmented global) routing allows high-fanout nets to traverse small or large areas of the ProASIC3 devices with low skew and flexibility. The VersaNet network is used automatically by the software tools to route clocks and high-fanout nets.

7 JTAG (IEEE1532)

ProASIC3 devices use industry-standard JTAG programming (IEEE1532). In addition, ProASIC3 devices support board-level JTAG (IEEE1149) I/O boundary scan.

8 PLL and CCC

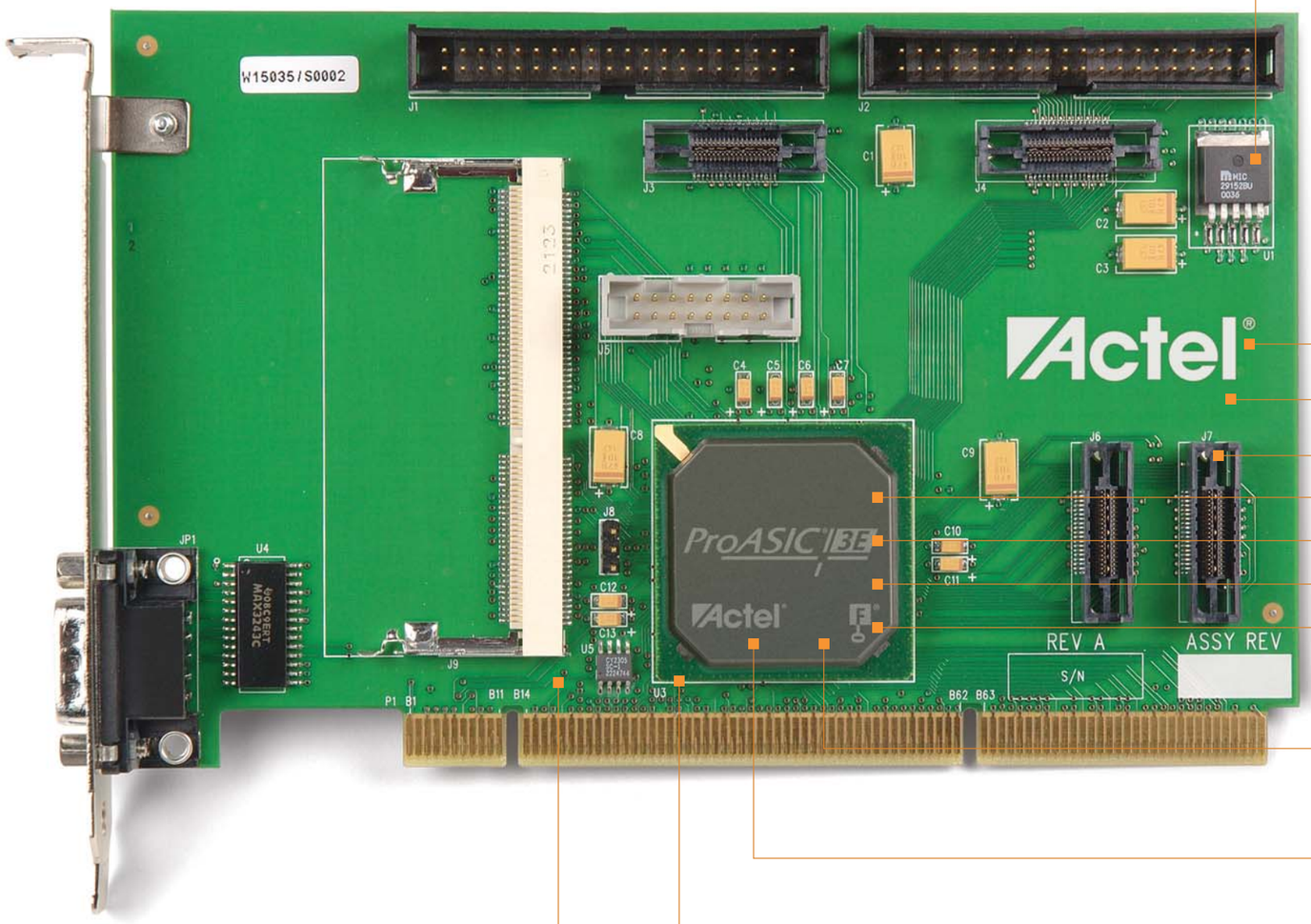
ProASIC3 devices have up to six clock conditioning circuits (CCCs) with up to six PLLs.

- Wide input frequency range (f_{IN_CCC}) = 1.5 to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 to 350 MHz
- Output phase shift = 0°, 90°, 180°, and 270°

9 SRAM and FIFOs

ProASIC3 devices have embedded dual-port SRAM and FIFO blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, or 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. Dedicated FIFO control logic enables flexible and efficient FIFO implementations.

The Lowest Total System Cost with ProASIC3 Flash FPGAs



Single-Voltage Solution

ProASIC3 and ProASIC3L devices can be powered from a single 1.2 V or 1.5 V supply for both core and I/Os. Unlike some SRAM FPGAs, there is no requirement for a 2.5 V or 3.3 V supply for power-up. The FPGA configuration information is stored on the chip in nonvolatile flash as part of the FPGA fabric. Running the whole system on a single supply saves the cost and area associated with voltage regulators.

No Live At Power-Up (LAPU) CPLD Required

ProASIC3 flash-based FPGAs are live at power-up (LAPU). CPLDs are unnecessary to start your system during power-up, saving total system cost.

Reduced Board Space

Fewer components in your system lead to reduced PCB area, increased reliability, simpler inventory management, and total system cost savings. Feature-rich FPGAs supporting small footprint packages allow you to implement complex designs in a tight area and reduce cost.

ISP Header

ISP uses the industry-standard JTAG (IEEE1532) protocol. In addition, configuration data can be decrypted using the on-chip AES-decryption core. This allows for secure FPGA updates to be sent over public networks (e.g., the Internet) and decrypted on-chip. The FROM data can also be sent to the ProASIC3 device encrypted if required. No expensive service call is required to update the FPGA code.

Single Chip

No boot PROM or flash MCU is required to load the FPGA at system power-up. This results in a reduced PCB area and simplified inventory management, which reduces total system cost.

No Power Sequencing

I/O power-up/-down management is built into ProASIC3 devices. Reliable and predictable I/O and device behavior during power-up and power-down eliminates the need for a system power sequence device and reduces total system cost.

Ultra-Low Power

ProASIC3 flash-based FPGAs have low static and dynamic power consumption and no power-up current spike. This allows you to use a smaller and cheaper power source, reducing total system cost, and increasing system reliability. With ProASIC3L, additional power savings can be achieved using the Flash*Freeze pin, allowing designers to enter and exit from active to static mode and back again within 1 µs, thus eliminating the need for additional clocks or I/Os for power management.

Clock Management

Simplify system complexity and reduce component count and cost by using Actel ProASIC3 devices for "instant-on" derivative clock generation and distribution. The live-at-power-up clock conditioning circuitry and PLLs of ProASIC3 devices allow for removal of the additional external clock distribution chips often used to boot SRAM FPGAs or microcontrollers during system start-up.

Single-Voltage ISP

In-system programming can be done with a single 3.3 V connection to the part. The 3.3 V V_{PUMP} voltage can be provided directly from the programmer via the ISP header and does not need to be generated on the board.

Reduced Liability and Enhanced Reliability

Secure and firm-error immune ProASIC3 flash devices allow you to protect your designs from theft, tampering, and cloning. In addition, ProASIC3 devices protect your systems from costly firm-error related support and litigation liability concerns.

Superior Noise-Reduced I/Os

ProASIC3 devices support separate power and ground supplies for input and output pins. This contributes to I/O noise immunity and may help remove EMI emission.

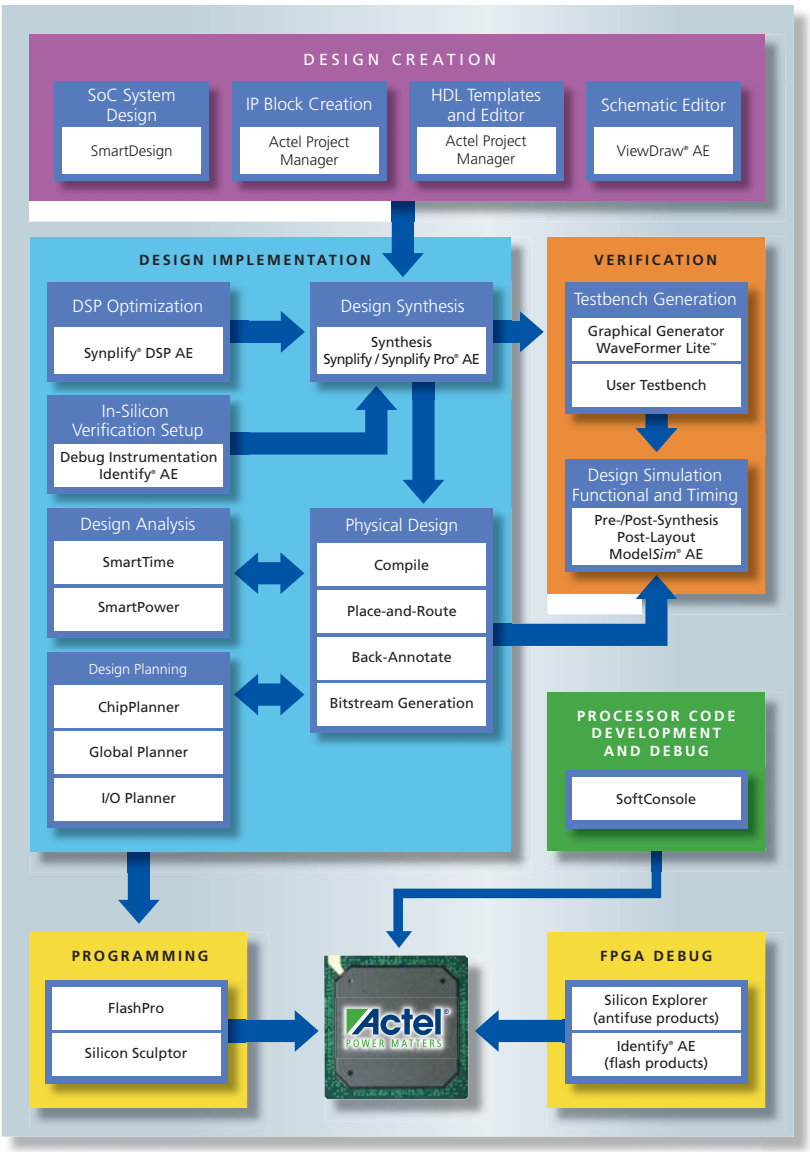
No Power-Up Monitor Chip

Unlike SRAM configuration bits, flash configuration switches do not experience brownout. No voltage monitor chip is required to ensure reliable operation and clean power-up/-down of the system, reducing total system cost.

Design Software

Actel Libero® Integrated Design Environment (IDE) is a comprehensive software toolset for designing with all ProASIC3 family devices, including the ProASIC3L low-power devices and low cost ProASIC3 nano devices. Libero IDE easily manages the complete design flow, ensuring maximum device performance and resource utilization. The lowest possible power consumption is assured using Libero Power-Driven Layout and detailed identification of power hotspots using SmartPower.

Libero IDE offers the latest and best-in-class FPGA development tools from leading EDA vendors such as Mentor Graphics®, SynaptiCAD™, and Synplicity®. These tools, combined with Actel-developed tools, allow quick optimization, verification, and physical implementation of your design. An intuitive user interface guides you through the process while a powerful Project Manager organizes your design files and manages exchanges between the various tools.



Libero IDE flow begins with multiple options for design entry, which include processor subsystem and IP configuration, core configuration, HDL templates, and schematic capture. The output of these design entry tools can easily be combined and utilized by the new Libero IDE SmartDesign tool, which provides a graphical block system design flow. Design optimization and verification are easily managed with Synplify Pro, Synplify DSP, WaveFormer Lite, and Model*Sim*. From netlist import, physical implementation is performed using the following features:

- Timing and power-driven place-and-route
- Floor planning (MultiView Navigator)
- Physical constraints (MultiView Navigator and SmartTime)
- Timing constraints and analysis (SmartTime)
- Power analysis (SmartPower)
- Program file generation, programming with the FlashPro series, and debug with Synplicity Identify AE.

Libero IDE offers feature, cost, license, and operating system flexibility. Libero IDE Platinum for Microsoft® Windows® is a comprehensive tool suite, supporting all tools and all Actel FPGAs. A 45-day evaluation version that contains all the Actel tools (except program file generation) is available at no charge. You can also choose a one-year free Libero IDE Gold license that includes programming but has limited tool and device support. Libero IDE is supported on Red Hat® Linux operating systems with a limited tool set. Actel Designer FPGA physical implementation software is part of Libero IDE, but if you have your own front-end design and verification tools, Designer is available in a standalone version and is compatible with all leading design and verification tools. Designer is available for Windows and Linux operating systems.

Programming

ProASIC3 devices offer ISP capabilities. To program a device mounted on a system board, a programmer can simply be connected to the ISP header. The configuration data is supplied through a standard JTAG interface from a microprocessor, Silicon Sculptor II, or FlashPro3. The FlashPro3 programmer, with its small size, ease of portability, and USB programming port connections, is ideal for prototyping. FlashPro3 allows high-speed programming; even the largest ProASIC3 parts may be programmed in less than two minutes.

FlashPro3 Programmer

By connecting several FlashPro3 programmers via USB 2.0 hubs, low-cost parallel programming is possible. The FlashPro3 programmers allow ISP of ProASIC3 parts already board-mounted via a single ISP header. Commonly used ISP headers are provided in FlashPro3. The FlashPro software provides a simple GUI to allow parallel programming of ProASIC3 devices and serialization of the FlashROM.

Multiple ProASIC3 devices, as part of a large JTAG programming chain on a single board, may be programmed via a single header using the ChainBuilder software. ChainBuilder allows standard JTAG (IEEE1152) programming of ProASIC3 parts, one by one, automatically bypassing the non-flash parts. ChainBuilder and the FlashPro software work together to simplify and reduce the costs of programming complex systems. The concurrent version of ChainBuilder extends this capability to allow multiple devices on the same board to be programmed at the same time.

Finally, microprocessor-based ISP programming for ProASIC3 devices is handled by Actel DirectC software, which provides a high-speed solution for low-speed microprocessors.

Starter Kits

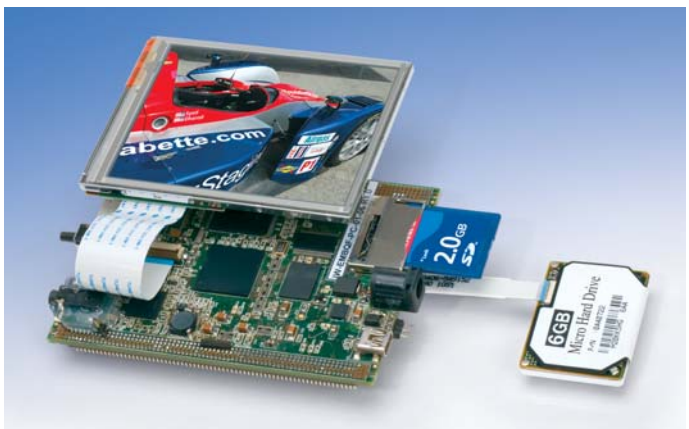
Various ProASIC3 family starter kits are available as a complete package, consisting of an evaluation board with a ProASIC3 family device, Actel Libero IDE Gold, the FlashPro3 programmer with a USB cable, FlashPro software, programming cables with an ISP header, a power supply, tutorials, and support documentation. You can explore the various benefits of nonvolatile ProASIC3 family FPGAs, including ISP, device serialization, and FlashLock on-chip system security. Additionally, this kit enables you to efficiently evaluate the performance and functionality of designs for cost-sensitive, ASIC-alternative applications.

System Solutions

In collaboration with its partners, Actel offers a wide range of solutions targeted for applications, including the following:

- Storage interfaces like SD, CompactFlash, ATA, CE-ATA and more
- Display controllers for performing various video functions for a wide range of LCD panels from different manufacturers and supporting different standards

- GPS receiver
- Motor control for stepper, brushed, and brushless motors to implement fast and precise control algorithms
- Communications including USB, Ethernet, CAN and more



Solutions include demonstration and development platforms, reference designs, and tools that allow the integration of proven IP cores or reference blocks into final designs. Through a network of Solutions Partners who have extensive knowledge and a proven track record in various applications, Actel provides a complete ecosystem to assist development. The result is faster time-to-market and reduced costs.

IP Compliments Nonvolatile, Secure, Low-Power Actel FPGAs

With over 170 IP cores and supporting products optimized for the Actel flash-based ProASIC3 family of devices, Actel supports the communications, consumer, military, medical, industrial, automotive, and aerospace markets.

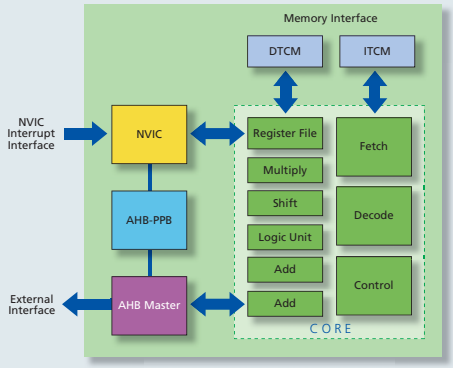
DirectCores are sourced, verified, supported, and maintained by Actel. They come complete as pre-implemented, synthesizable building blocks and have been thoroughly tested and verified in Actel FPGAs. They are designed and optimized for use in Actel flash-based families of devices. DirectCores are delivered seamlessly using CoreConsole, with automatic updates and no additional licensing required for most of the cores.

CompanionCores provide Actel customers with a wide variety of IP cores that are sourced, verified, supported, and maintained by Actel IP partners. They are pre-built IP cores and reference blocks to streamline your designs, enable faster time-to-market, and minimize design costs and risks.

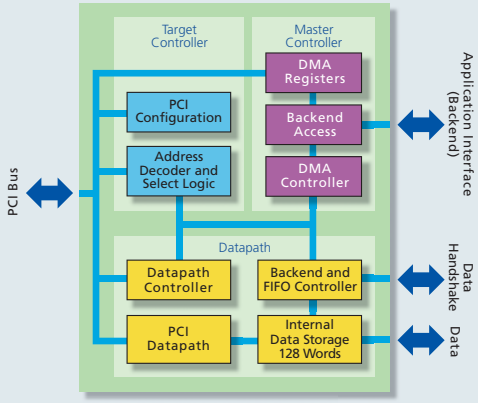
One Company Serving All Your Design Needs

Actel DirectCores and Third Party Cores provide an abundance of IP choices to complete your design. Actel IP cores allow the system designer to focus on differentiating capabilities, not recreating building blocks. Additionally, Actel IP cores are optimized for use with Actel silicon. Because Actel thoroughly verifies its IP cores, you can spend more of your time verifying the system instead of the IP component.

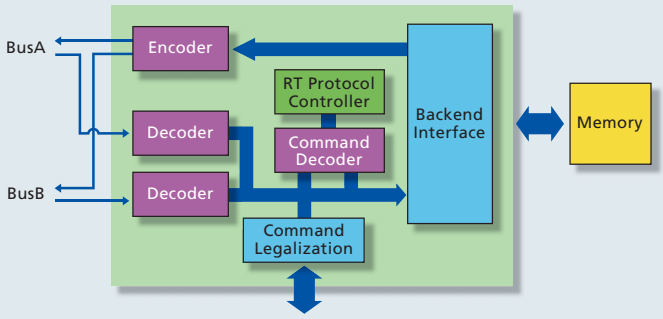
- Developed specifically for FPGA implementation
- 3-stage, 32-bit pipeline—ARMv6-M instruction set architecture
- No license fees or royalties
- User-programmed into the FPGA
- All ARM Cortex-M1 I/Os are accessible to the user
- Upwards compatible with Cortex-M3
- Executes all Thumb® code—can run ARM7 and ARM9 Thumb subroutines
- Supported by a full range of development tools



- PCI specification 3.0 compliant
- Application interface designed for synchronous or asynchronous transfers with FIFO support
- Zero-wait-state burst mode transfers
- Silicon-proven 66 MHz performance
- 32-bit and 64-bit operation
- Includes Master and Target
- Backend designed to work with CoreSDR/DDR
- Used in PCI card and embedded applications



- MIL-STD-1553B compliant
- Connects backend interface to memory or directly to system devices
- Interfaces to standard transceivers
- 12, 16, 20, or 24 MHz clock operation
- Compatible with legacy remote terminal systems
- Redundancy for severe environments
- Low-power operation



ProASIC3 Family Product Table

ProASIC3 Devices	A3PN010	A3PN015	A3P015	A3PN020	A3PN030	A3P030	A3PN060	A3P060	A3PN125	A3P125
System Gates	10 k	15 k	15 k	20 k	30 k	30 k	60 k	60 k	125 k	125 k
Typ. Equivalent Macrocells	86	128	128	175	256	256	512	512	1,024	1,024
VersaTiles (D-flip-flops)	260	384	384	520	768	768	1,536	1,536	3,072	3,072
RAM kbits (1,024 bits)	–	–	–	–	–	–	18	18	36	36
4,608-Bit Blocks	–	–	–	–	–	–	4	4	8	8
FlashROM (bits)	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP[3]	–	–	–	–	–	–	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	–	–	–	–	–	–	1	1	1	1
VersaNet Globals[1]	4	4	6	4	6	6	18	18	18	18
I/O Standards	Std., Hot-Swap	Std., Hot-Swap	Std., Hot-Swap	Std., Hot-Swap	Std., Hot-Swap	Std., Hot-Swap	Std., Hot-Swap	Std.+	Std., Hot-Swap	Std.+
I/O Banks (+ JTAG)	2	3	2	3	2	2	2	2	2	2
Speed Grades	Std., -1, -2	Std., -1, -2	-F, Std., -1, -2	Std., -1, -2	Std., -1, -2	-F, Std., -1, -2	Std., -1, -2	-F, Std., -1, -2	Std., -1, -2	-F, Std., -1, -2
Temperature Grades	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I
Package Pins	QN48	QN68	QN68	QN68	QN48 QN68 VQ100	QN48 QN68 QN132 VQ100	VQ100	QN132 VQ100 TQ144 FG144	VQ100	QN132 VQ100 TQ144 PQ208 FG144

ProASIC3 Devices	A3PN250	A3P250L	A3P250	A3P400	A3P600	A3PE600	A3P600L	A3P1000	A3P1000L	A3PE1500	A3PE3000	A3P3000L
ARM-Enabled ARM7 ProASIC3 Devices								M7A3P1000				
ARM-Enabled Cortex-M1 ProASIC3 Devices			M1A3P250	M1A3P400	M1A3P600		M1A3P600L	M1A3P1000	M1A3P1000L	M1A3PE1500	M1A3P3000	M1A3P3000L
System Gates	250 k	250 k	250 k	400 k	600 k	600 k	600 k	1 M	1 M	1.5 M	3 M	3 M
VersaTiles (D-flip-flops)	6,144	6,144	6,144	9,216	13,824	13,824	13,824	24,576	24,576	38,400	75,264	75,264
RAM kbits (1,024 bits)	36	36	36	54	108	108	108	144	144	270	504	504
4,608-Bit Blocks	8	8	8	12	24	24	24	32	32	60	112	112
FlashROM (bits)	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP[3]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	1	1	1	1	1	6	1	1	1	6	6	6
VersaNet Globals[1]	18	18	18	18	18	18	18	18	18	18	18	18
I/O Standards	Std., Hot-Swap	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS
I/O Banks (+ JTAG)	4	4	4	4	4	8	4	4	4	8	8	8
Speed Grades	Std., -1, -2	-F, Std., -1	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1	-F, Std., -1, -2	-F, Std., -1	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1
Temperature Grades	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I
Package Pins	VQ100	VQ100 PQ208 FG144 FG256	QN132 VQ100 FG144 FG256	FG144 FG256 FG484	FG144 FG256 FG484	PQ208 FG256 FG484	PQ208 FG144 FG256 FG484	FG144 FG256 FG484	PQ208 FG144 FG256 FG484	PQ208 FG484 FG676	PQ208 FG324 FG484 FG896	PQ208 FG324 FG484 FG896

Notes: [1] *Six chip (main) and twelve quadrant global networks are available for PA3060 and above.*
[2] *Device/package support TBD.*
[3] *AES not available for ARM-enabled ProASIC3 devices.*
[4] *The M1A3P250 device does not support this package.*

For more information regarding **ProASIC3 Flash FPGA families**, please visit the Actel website at **www.actel.com** or contact your local sales representative.

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