

**PAM8902A**

**30 V<sub>PP</sub> MONO CLASS-D AUDIO AMPLIFIER FOR  
PIEZO/CERAMIC SPEAKERS WITH ANTI-SATURATION**

## Description

The PAM8902A is a mono, Class-D audio amplifier with integrated boost convertor designed for piezo and ceramic speakers. The PAM8902A is capable for driving a ceramic/piezo speaker with 30V<sub>PP</sub>(0.6Vrms) from a 3.6V power supply. The PAM8902A's boost converter operates at a fixed frequency of 1.5MHz and provides a 17.5V supply with a minimum number of external components. The three gain mode of 18dB, 22dB and 26dB is easy for using. PAM unique anti-saturation technology which detects output signal clip due to the over level input signal suppress the output signal clip automatically. PAM8902A features an integrated audio low pass filter that rejects high frequency noise, thus improving audio fidelity. PAM8902A also provides thermal, over current, under and over voltage protection.

The PAM8902A is available in a 16-ball 1.95mm x 1.95mm CSP package and 16-pin QFN4x4 package.

## Features

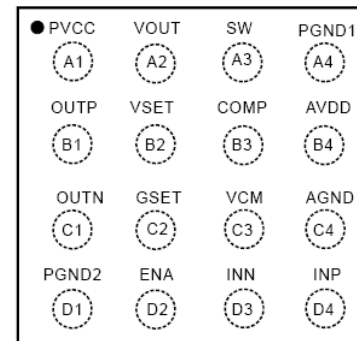
- Supply Voltage Range from 2.7V to 5.5V package.
- 30V<sub>PP</sub> Output Load Voltage from a 2.7V Supply
- Integrated Boost Converter Generates 17.5V Supply
- Programmable Soft-Start
- Unique Anti-Saturation Function
- Small Boost Converter Inductor
- Selectable Gain of 18dB, 22dB, and 26dB (Refer to "Application Notes")
- Selectable Boost output voltage of 8V, 12V, and 17.5V
- Low Shutdown Current: <1μA
- Build in Thermal, OCP, UVLO, OVP
- Available in Space Saving Packages:
  - 16-ball 1.95mm x 1.95mm CSP package
  - 16-pin QFN4x4 package

## Applications

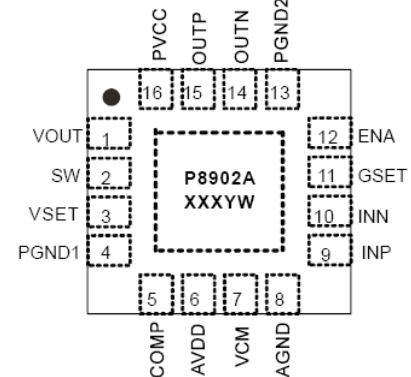
- Wireless or Cellular Handsets
- Portable DVD Player
- Personal Digital Assistants (PDAs )
- Electronic Dictionaries
- Digital Still Cameras

## Pin Assignments

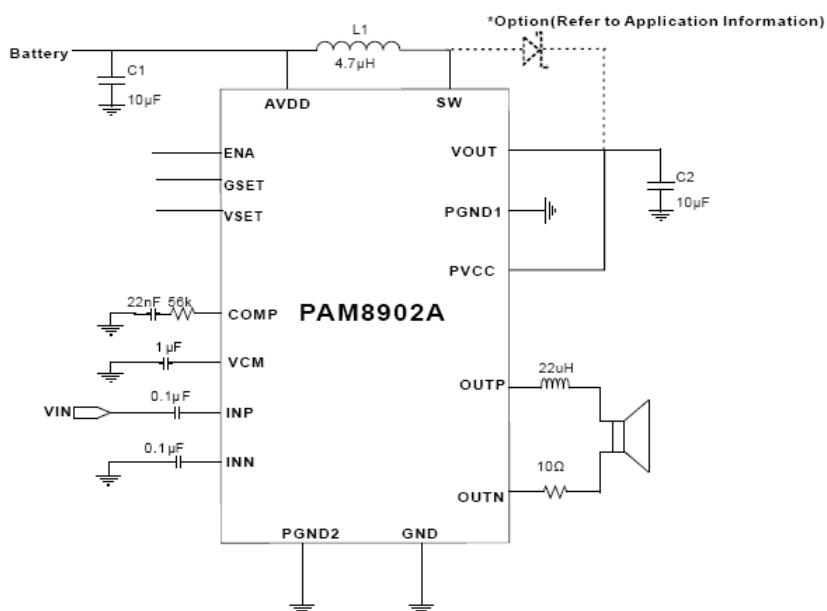
16 Ball CSP  
Top View



Top View  
QFN 4X4 16L



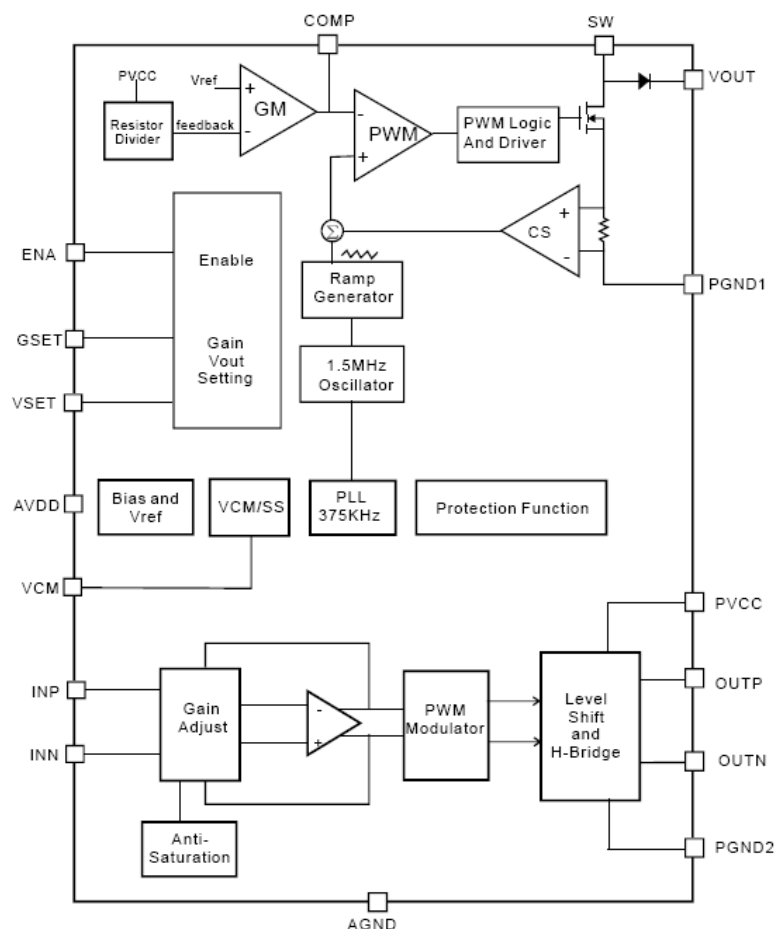
## Typical Applications Circuit



## Pin Descriptions

| Bump (CSP) | Pin Number (QFN) | Pin Name | Function                                              |
|------------|------------------|----------|-------------------------------------------------------|
| A1         | 13               | PVCC     | Audio Amplifier Power Supply                          |
| A2         | 1                | VOUT     | Boost Convertor Output                                |
| A3         | 2                | SW       | Boost Convertor Switching Node                        |
| A4         | 4                | PGND1    | Boost Convertor Power Ground                          |
| B1         | 15               | OUTP     | Positive Differential Audio Output                    |
| B2         | 3                | VSET     | Boost Convertor Output Voltage Setting(8V,12V,17.5V)  |
| B3         | 5                | COMP     | Boost Convertor Compensation                          |
| B4         | 6                | AVDD     | Power Supply                                          |
| C1         | 14               | OUTN     | Negative Differential Audio Output                    |
| C2         | 11               | GSET     | AmplifierGain Setting. (Refer to "Application Notes") |
| C3         | 7                | VCM      | Common Mode Bypass Cap                                |
| C4         | 8                | AGND     | Analog Ground                                         |
| D1         | 13               | PGND2    | Class D PowerGround                                   |
| D2         | 12               | ENA      | Whole Chip Enable                                     |
| D3         | 10               | INN      | Negative Differential Audio Input                     |
| D4         | 9                | INP      | Positive Differential Audio Input                     |

## Functional Block Diagram



## Absolute Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

| Parameter                    | Rating                       | Unit |
|------------------------------|------------------------------|------|
| Supply Voltage               | 6.0                          | V    |
| Input Voltage                | -0.3 to V <sub>DD</sub> +0.3 |      |
| Maximum Junction Temperature | +150                         | °C   |
| Storage Temperature          | -65 to +150                  |      |
| Soldering Temperature        | 250, 10 sec                  |      |

## Recommended Operating Conditions (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Parameter                  | Rating      | Unit |
|----------------------------|-------------|------|
| Supply Voltage Range       | 2.7 to 5.5  | V    |
| Ambient Temperature Range  | -40 to +85  | °C   |
| Junction Temperature Range | -40 to +125 | °C   |

## Thermal Information

| Parameter                                | Package   | Symbol        | Max      | Unit |
|------------------------------------------|-----------|---------------|----------|------|
| Thermal Resistance (Junction to Ambient) | CSP       | $\theta_{JA}$ | 90 – 220 | °C/W |
|                                          | QFN4x4-16 |               | 37       |      |
| Thermal Resistance (Junction to Case)    | CSP       | $\theta_{JC}$ | 75       |      |
|                                          | QFN4x4-16 |               | 2        |      |

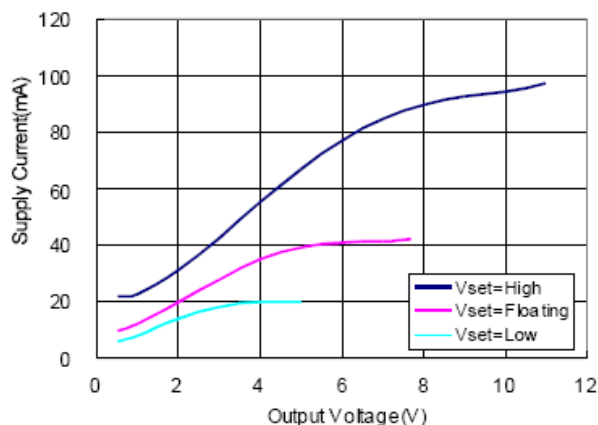
## Electrical Characteristics

(@T<sub>A</sub> = +25°C, V<sub>DD</sub> = 3.6V, C<sub>L</sub> = 1μF, V<sub>SET</sub> floating, R<sub>LOAD</sub> = 10Ω, L<sub>LOAD</sub> = 22μH with external schottky diodes, unless otherwise specified.)

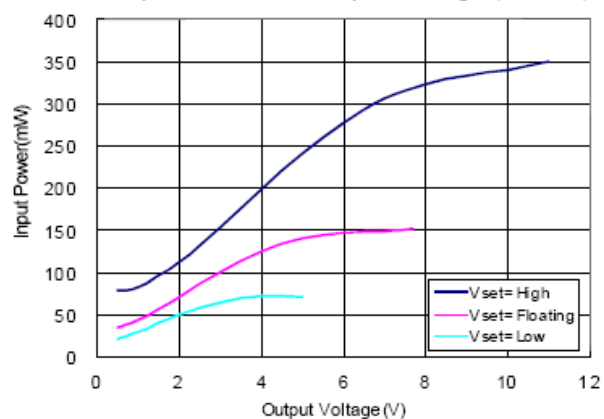
| Parameter                             | Symbol            | Test Conditions                                                 | Min                  | Typ  | Max                | Units |
|---------------------------------------|-------------------|-----------------------------------------------------------------|----------------------|------|--------------------|-------|
| Input Voltage                         | V <sub>DD</sub>   |                                                                 | 2.7                  |      | 5.5                | V     |
| Quiescent Current                     | I <sub>Q</sub>    | EN > 1.2V, V <sub>SET</sub> = High                              |                      | 30   | 48                 | mA    |
|                                       |                   | EN > 1.2V, V <sub>SET</sub> = Floating                          |                      | 10   | 18                 |       |
|                                       |                   | EN > 1.2V, V <sub>SET</sub> = GND                               |                      | 5    | 12                 |       |
| Shutdown Current                      | I <sub>SD</sub>   | EN = 0V                                                         |                      | 0.1  | 1                  | μA    |
| Wake-Up Time                          | T <sub>WU</sub>   | EN from Low to High                                             |                      | 40   |                    | mS    |
| Chip Enable                           | V <sub>EH</sub>   |                                                                 | 1.2                  |      |                    | V     |
| Chip Disable                          | V <sub>EL</sub>   |                                                                 |                      |      | 0.4                |       |
| GSET/ VSET High                       | V <sub>H</sub>    |                                                                 | V <sub>DD</sub> -0.5 |      | V <sub>DD</sub>    | V     |
| GSET/ VSET Floating                   | V <sub>F</sub>    |                                                                 | 1                    |      | V <sub>DD</sub> -1 |       |
| GSET/ VSET Low                        | V <sub>L</sub>    |                                                                 | 0                    |      | 0.5                |       |
| Under Voltage Lockout Threshold       | UVLO              | V <sub>DD</sub> from High to Low                                |                      | 2.2  |                    | V     |
| Under Voltage Lockout Hysteresis      | UVLO(H)           | V <sub>DD</sub> from Low to High                                |                      | 0.2  |                    |       |
| Thermal Shutdown Threshold            | OTP               |                                                                 |                      | 150  |                    | °C    |
| Thermal Shutdown Lockout Hysteresis   | OTP(H)            |                                                                 |                      | 30   |                    | °C    |
| <b>Boost Converter</b>                |                   |                                                                 |                      |      |                    |       |
| Output Voltage                        | V <sub>O1</sub>   | V <sub>SET</sub> = Low, No Load                                 | 7.2                  | 8.0  | 8.8                | V     |
|                                       | V <sub>O2</sub>   | V <sub>SET</sub> = Floating, No Load                            | 10.8                 | 12.0 | 13.2               | V     |
|                                       | V <sub>O3</sub>   | V <sub>SET</sub> = High, No Load                                | 16.0                 | 17.5 | 19.0               | V     |
| Current Limit                         | C <sub>L</sub>    | Average Input Current                                           |                      | 0.8  |                    | A     |
| Lowside MOSFET R <sub>DS(ON)</sub>    | R <sub>LS</sub>   | I <sub>O</sub> = 50mA                                           |                      | 0.5  |                    | Ω     |
| Boost Switching Frequency             | f <sub>OSCB</sub> |                                                                 | 1.1                  | 1.5  | 1.9                | MHz   |
| Over Voltage Protection Threshold     | V <sub>OVP</sub>  |                                                                 |                      | 18   |                    | V     |
| <b>Class D</b>                        |                   |                                                                 |                      |      |                    |       |
| Class D Amplifier Switching Frequency | f <sub>OSCD</sub> | Input AC-GND                                                    | 225                  | 375  | 475                | KHz   |
| Common Mode Reject Ratio              | CMRR              | V <sub>IN</sub> = ±100mV, V <sub>DD</sub> = 3.6V                |                      | 60   |                    | dB    |
| Output Offset Voltage                 | V <sub>OS</sub>   | Output Offset Voltage                                           |                      | 5    | 50                 | mV    |
| R <sub>DS(ON)</sub>                   | R <sub>P</sub>    | High Side                                                       |                      | 1.5  |                    | Ω     |
|                                       |                   | Low Side                                                        |                      | 0.6  |                    | Ω     |
| Closed-Loop Voltage Gain              | A <sub>V1</sub>   | G <sub>SET</sub> = High, V <sub>O</sub> = 1V <sub>RMS</sub>     | 25                   | 26   | 27                 | dB    |
|                                       | A <sub>V2</sub>   | G <sub>SET</sub> = Floating, V <sub>O</sub> = 1V <sub>RMS</sub> | 21                   | 22   | 23                 |       |
|                                       | A <sub>V3</sub>   | G <sub>SET</sub> = Low, V <sub>O</sub> = 1V <sub>RMS</sub>      | 17                   | 18   | 19                 |       |
| Power Supply Reject Ratio             | PSRR              | 200m V <sub>PP</sub> Supply Ripple @ 217Hz                      |                      | 70   |                    | dB    |
| Total Harmonic Distortion Plus Noise  | THD+N             | V <sub>O</sub> = 5V <sub>RMS</sub>                              |                      | 0.3  |                    | %     |
| Signal to Noise Ratio                 | SNR               | Input AC Ground, A-Weighting                                    |                      | 90   |                    | dB    |

**Typical Performance Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 3.6\text{V}$ ,  $C_L = 1\mu\text{F}$ ,  $L = 4.7\mu\text{H}$ ,  $V_{SET}$  floating,  $R_{LOAD} = 10\Omega$ ,  $L_{LOAD} = 22\mu\text{H}$ , with external schottky diode, unless otherwise specified.)

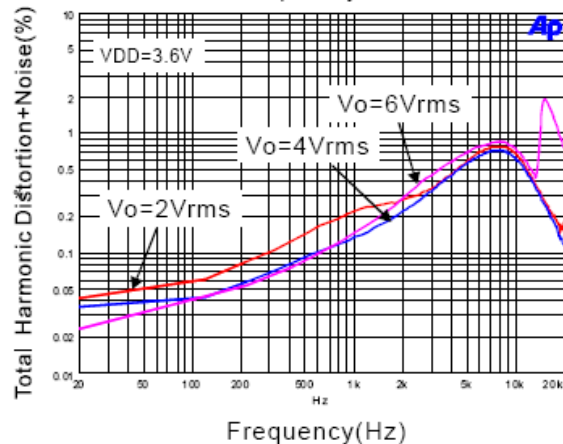
1. Supply Current VS Output Voltage ( $V_o=8\text{V}$ )



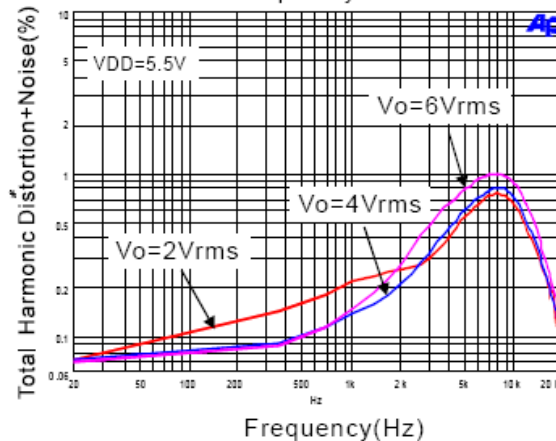
2. Input Power VS Output Voltage ( $V_o=8\text{V}$ )



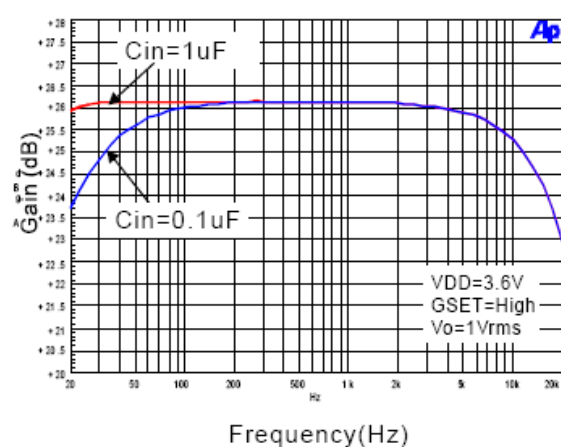
3. THD+N VS Frequency



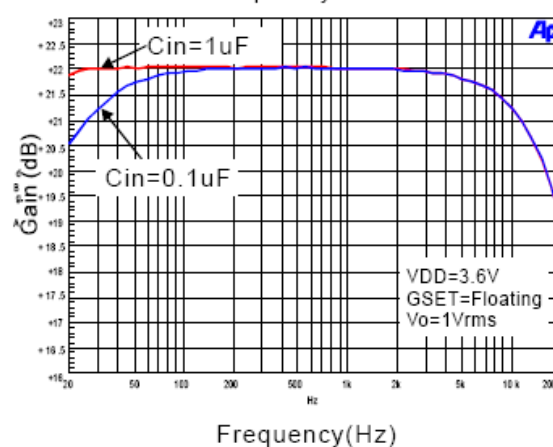
4. THD+N VS Frequency



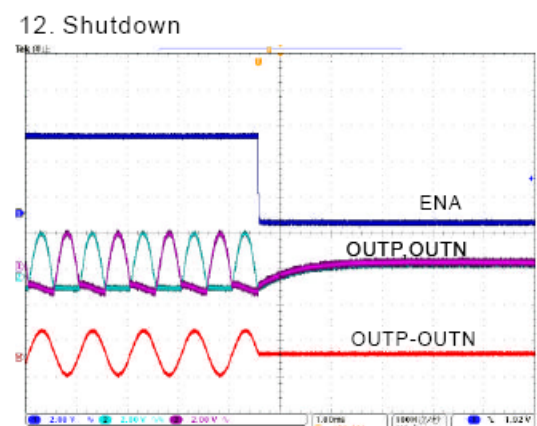
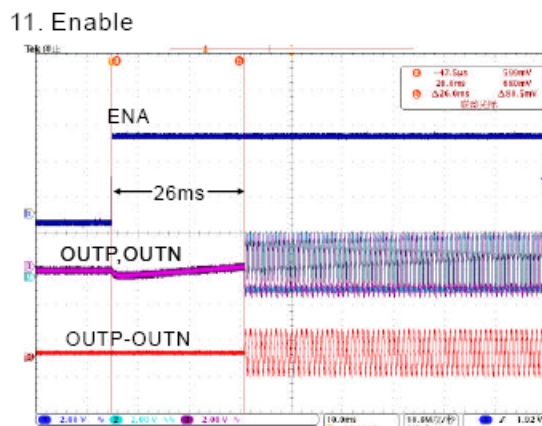
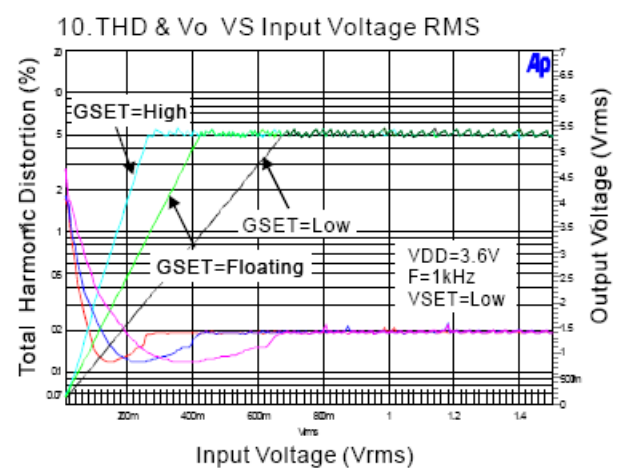
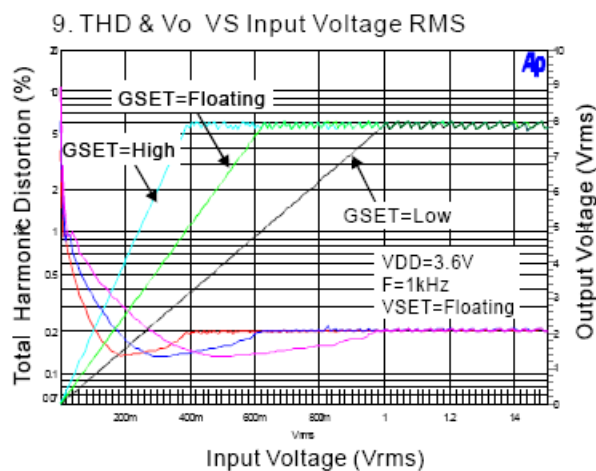
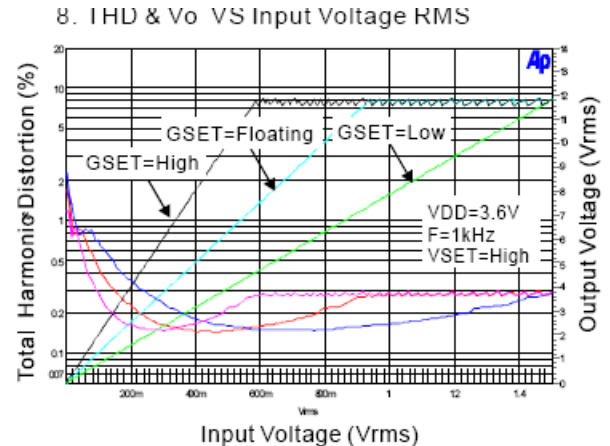
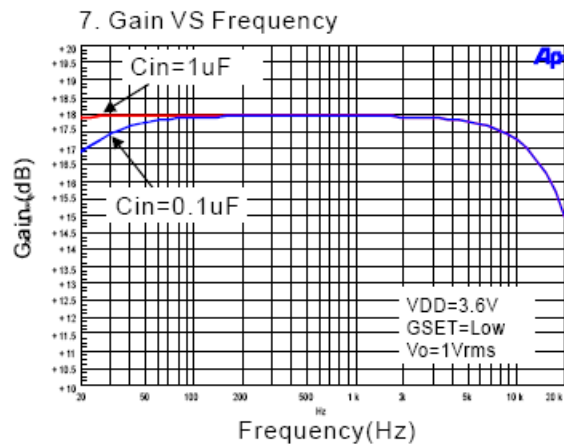
5. Gain VS Frequency



6. Gain VS Frequency



**Typical Performance Characteristics** (cont.) (@ $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 3.6\text{V}$ ,  $C_L = 1\mu\text{F}$ ,  $L = 4.7\mu\text{H}$ ,  $V_{SET}$  floating,  $R_{LOAD} = 10\Omega$ ,  $L_{LOAD} = 22\mu\text{H}$ , with external schottky diode, unless otherwise specified.)



## Application Information

### Select Boost Converter Output Voltage

The  $V_{SET}$  pin sets the boost converter output voltage to 8V, 12V or 17.5V.  $V_{SET}$  pin configuration table as below:

| $V_{SET}$ Pin Configuration | Min          | Max         | PVCC Voltage | Audio Amplifier Maximum Output Voltage |
|-----------------------------|--------------|-------------|--------------|----------------------------------------|
| High                        | $AVDD - 0.5$ | $AVDD$      | 17.5V        | 11 $V_{RMS}$ ( $V_{PP} = 31.1V$ )      |
| Floating                    | 1V           | $AVDD - 1V$ | 12V          | 8 $V_{RMS}$ ( $V_{PP} = 22.6V$ )       |
| Low                         | GND          | 0.5V        | 8V           | 5 $V_{RMS}$ ( $V_{PP} = 14.1V$ )       |

### Gain Setting and Input Resistance ( $R_I$ )

Gain setting function is only available in disable condition ( $ENA = low$ ) and need to follow the sequence as pull  $ENA$  to low (disable the IC) first, and change the  $GSET$  voltage between high, floating, low, then pull  $ENA$  to high (enable the IC).

The input resistors ( $R_I = R_{IN} + R_{EX}$ ) set the gain of the amplifier according to Equation 1 when anti-saturation is inactive.

$$G = 20 \text{ Log } [12.8 \cdot R_F / (R_{IN} + R_{EX})] \text{ (dB)}$$

| $G_{SET}$ | $R_{IN}$        | $R_{FB}$        |
|-----------|-----------------|-----------------|
| High      | 77.4k $\Omega$  | 122.6k $\Omega$ |
| Floating  | 100k $\Omega$   | 100k $\Omega$   |
| Low       | 122.6k $\Omega$ | 77.4k $\Omega$  |

Where  $R_{IN}$  is a 77.4k $\Omega$  internal resistor,  $R_{EX}$  is the external input resistor,  $R_F$  is a 122.6k $\Omega$  internal resistor. Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the PAM8902A to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to lower. Lower gain allows the PAM8902A to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise. In addition to these features, higher value of  $R_I$  minimizes pop noise.

### Anti-Saturation/Clipping Function

The anti-saturation circuitry detects the duty cycle of the PWM output. When the output starts to exhibit clipping, the gain is automatically decreased with an attack time of 100 $\mu$ s per step a release time of 186ms per step. The following table describes the operation:

| Variable          | Description                                                           | Value                                                                                     |
|-------------------|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| Gain              | The original gain of the device when the Anti-saturation is inactive. | 26dB ( $G_{SET} = High$ )<br>22dB ( $G_{SET} = Floating$ )<br>18dB ( $G_{SET} = Low$ )    |
| Attenuation Range | The gain control range when anti-saturation is active.                | -26dB ( $G_{SET} = High$ )<br>-22dB ( $G_{SET} = Floating$ )<br>-18dB ( $G_{SET} = Low$ ) |
| Step Size         | Gain adjust step size.                                                | 0.25dB/Step                                                                               |
| Attack Time       | The minimum time between two gain decrements.                         | 100 $\mu$ s                                                                               |
| Release Time      | The minimum time between two gain increments.                         | 186ms                                                                                     |

## Application Information (cont.)

### Input Capacitors ( $C_I$ )

In the typical application, an input capacitor,  $C_I$ , is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case,  $C_I$  and the minimum input impedance  $R_I$  form a high-pass filter with the corner frequency determined in the follow equation:

$$f_C = \frac{1}{2\pi R_I C_I}$$

It is important to consider the value of  $C_I$  as it directly affects the low frequency performance of the circuit. For example, when  $R_I$  is 150k and the specification calls for a flat bass response are down to 150Hz.

Equation is reconfigured as followed:

$$C_I = \frac{1}{2\pi R_{IFC}}$$

When input resistance variation is considered, the  $C_I$  is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network ( $C_I$ ,  $R_I$  +  $R_F$ ) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at  $V_{DD}/2$ , which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

### Decoupling Capacitor

The PAM8902 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent series-resistance (ESR) ceramic capacitor, typically 1 $\mu$ F is placed as close as possible to the device AVDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10 $\mu$ F or greater placed near the AVDD supply trace is recommended.

### External Schottky Diode

Use external schottky diode can get the best driving capability and efficiency.

Since internal power diode has limited driving capability, only in following conditions customer can remove the external schottky diode to reduce the cost.

1.  $V_{SET}$  = Low or Floating and  $C_L$  less than 1 $\mu$ F.
2. The signal frequency less than 4KHz.
3. Haptic application (50–500Hz).

### Shutdown Operation

In order to reduce power consumption while not in use, the PAM8902A contains shutdown circuitry amplifier off when a logic low is placed on the ENA pin. By switching the ENA pin connected to GND, the PAM8902A supply current draw will be minimized in idle mode.

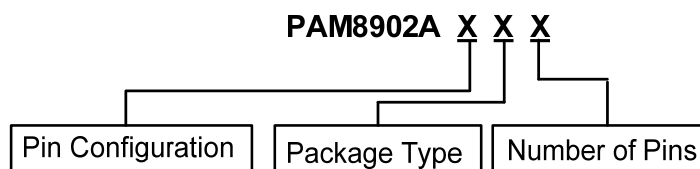
### Under-Voltage Lock-Out (UVLO)

The PAM8902A incorporates circuitry designed to detect supply voltage. When the supply voltage drops to 2.2V or below, the PAM8902A goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when reset the power supply or ENA pin.

### Over-Temperature Protection (OTP)

Thermal protection on the PAM8902A prevents the device from damage when the internal die temperature exceeds +150°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled, in this condition both OUP and OUTN will become high impedance. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 30°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

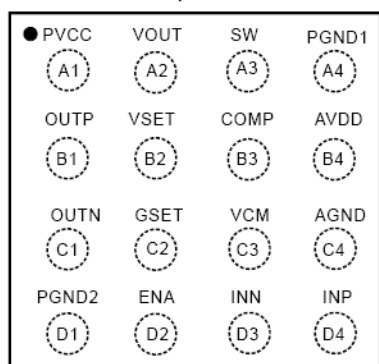
## Ordering Information



| Part Number | Part Marking    | Package Type | Standard Package    |
|-------------|-----------------|--------------|---------------------|
| PAM8902AZER | BN<br>YW        | CSP-16L      | 3000Units/Tape&Reel |
| PAM8902AKER | P8902A<br>XXXYW | QFN4x4-16L   | 3000Units/Tape&Reel |

## Marking Information

16 Ball CSP  
Top View

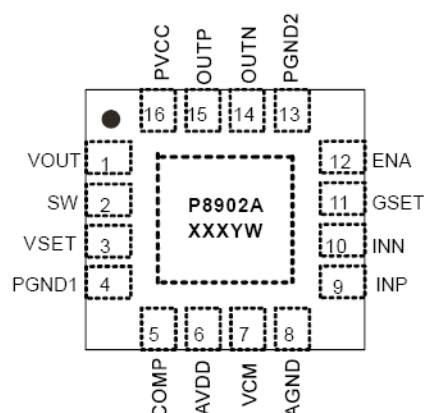


### Marking

BN  
YW

BN: Product Code of PAM8902A  
Y: Year  
W: Week

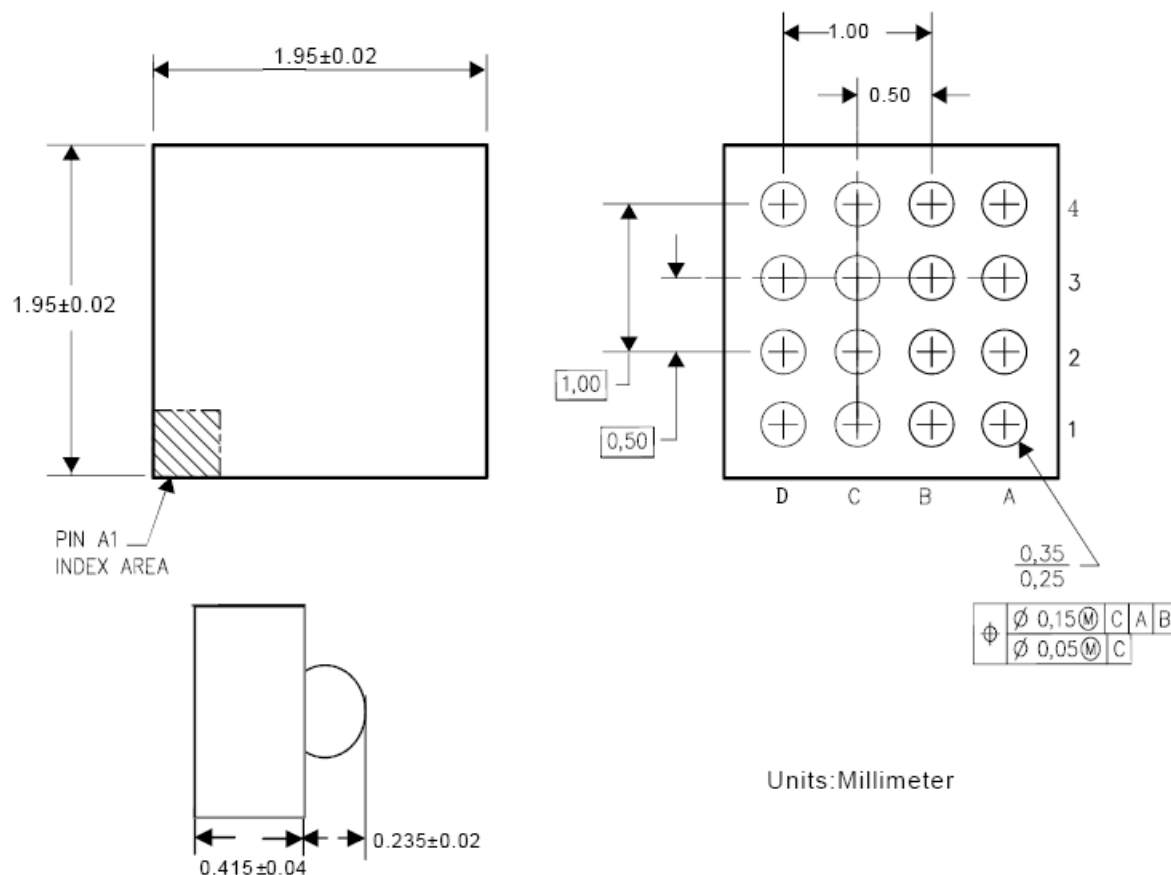
Top View  
QFN 4X4 16L



Y: Year  
W: Week  
X: Internal Code

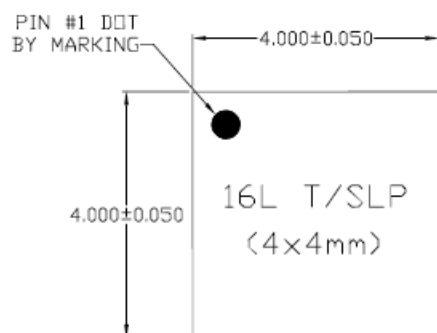
**Package Outline Dimensions** (All dimensions in mm.)

CSP-16

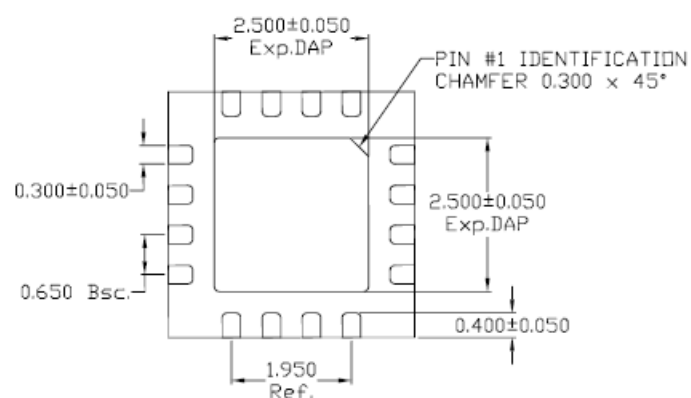


**Package Outline Dimensions** (cont.) (All dimensions in mm.)

QFN4x4-16



TOP VIEW

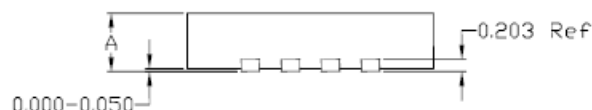


BOTTOM VIEW

NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE  
BUT WITH DIFFERENT THICKNESS:

| A |      |  | TSLP  | SLP   |
|---|------|--|-------|-------|
|   | MAX. |  | 0.800 | 0.900 |
|   | NOM. |  | 0.750 | 0.850 |
|   | MIN. |  | 0.700 | 0.800 |



SIDE VIEW

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1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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