PB63 • PB63A

Dual Power Booster Amplifier

FEATURES

- ♦ Wide Supply Range – ±20 V to ±75 V
- ♦ High Output Current – Up to 2 A Continuous
- ♦ Programmable Gain
- ♦ High Slew Rate – 1000 V/µs Typical
- ♦ Programmable Output Current Limit
- ♦ High Power Bandwidth – 1 MHz Typical
- ♦ Low Quiescent Current – 37 mA Typical (Total, Both Channels)

APPLICATIONS

- ♦ LED Test Equipment
- ♦ LCD Test Equipment
- ♦ Semiconductor Test Equipment
- ♦ High Voltage Instrumentation
- ♦ Electrostatic Transducers and Deflection
- ♦ Piezoelectric Positioning and Actuation
- ♦ Programmable Power Supplies

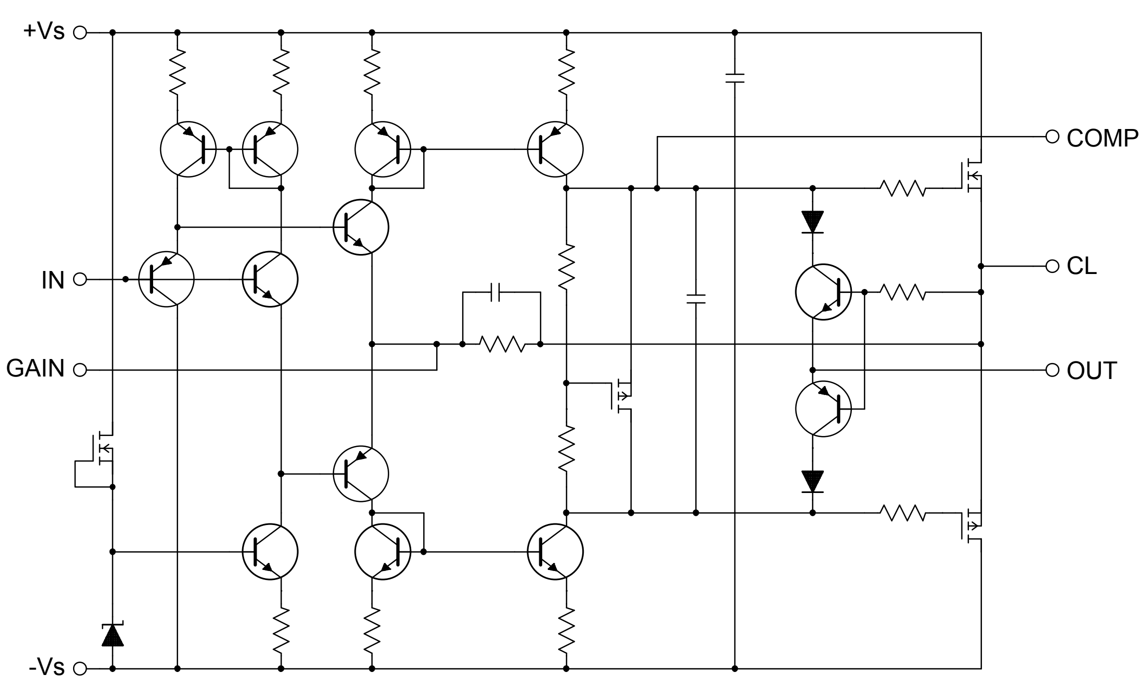
GENERAL DESCRIPTION

The PB63 is a dual high voltage, high current booster amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output current capability of the booster.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by Bipolar Junction Transistors. Although the booster can be configured quite simply, enormous flexibility is provided through the choice of driver amplifier, current limit and supply voltage.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The PB63 is packaged in Apex Microtechnology's 12-pin power SIP. The case is electrically isolated.

FIGURE 1. 1/2 Equivalent schematic



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	$+V_S$ TO $-V_S$		200	V
OUTPUT CURRENT, peak, per Channel within SOA			2	A
POWER DISSIPATION, internal DC (Note 5)	P_D		90	W
INPUT VOLTAGE referred to common	A_{IN}, B_{IN}	$(-V_S + 10V) / A_V$	$(+V_S - 10V) / A_V$	V
TEMPERATURE, pin solder - 10 secs max.	T_{PIN}		260	ºC
TEMPERATURE, junction (Note 2)	T_J		150	ºC
TEMPERATURE RANGE, storage	T_S	-55	125	ºC

SPECIFICATIONS (per amplifier)

Parameter	Test Conditions (Note 1)	PB63			PB63A			Units
		Min	Typ	Max	Min	Typ	Max	
INPUT								
OFFSET VOLTAGE		-20	±5	+20	-10	*	10	mV
OFFSET VOLTAGE vs. temp.	Full temperature range		+0.04			*		mV/ºC
INPUT BIAS CURRENT	Full temperature range	-50	+4	50	-25	*	25	µA
INPUT RESISTANCE, DC			97			*		MΩ
INPUT CAPACITANCE			3			*		pF
NOISE	f = 10KHz		25			*		$nV/Hz^{1/2}$
DC POWER SUPPLY REJECTION		87	100		*	*		dB
DC COMMON MODE REJECTION		75	78		*	*		dB
GAIN (Each Channel)								
OPEN LOOP GAIN	f = 10KHz		83			*		dB
BANDWIDTH, -3db	A_V = 5V/V, R_L = 50Ω		1.2			*		MHz
POWER BANDWIDTH, $100V_{p-p}$	A_V = 5V/V, R_L = 50Ω		1.0			*		MHz
OUTPUT (Each Channel)								
VOLTAGE SWING	I_O = 2A	|VS| - 11V	|VS| - 7.5V		*	*		V
VOLTAGE SWING	I_O = 0.5A		|VS| - 6.5V			*		V
CURRENT, Peak, Source	Per Channel		2		2			A
SLEW RATE	R_L = 50Ω, $10V_{P-P}$ input step, A_V = 10V/V	950	1000			*		V/µs
CAPACITIVE LOAD, 25% OVERSHOOT	$4V_{P-P}$ input step, A_V = 5V/V, Comp = 10pF		470			*		pF
SETTLING TIME to 0.1%	R_L = 50Ω, $4V_{P-P}$ input step, A_V=5V/V		300			*		ns
POWER SUPPLY (Note 3)								
VOLTAGE,± V_S		±20	±65	±75	*	*	*	V
CURRENT, quiescent	Both Channels		37	46		*	*	mA

Parameter	Test Conditions (Note 1)	PB63 Min	PB63 Typ	PB63 Max	PB63A Min	PB63A Typ	PB63A Max	Units
MATCHING SPECIFICATIONS, VS = ±75V, TC = 25°C Unless otherwise noted.								
INPUT OFFSET VOLTAGE MATCH			5			2	5	mV
GAIN MATCH			0.2				0.2	%
THERMAL								
RESISTANCE, AC junction to case (NOTE 4)	Full temp. range, f ≥ 60Hz		1.3	1.5		*	*	ºC/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		2.4	2.7		*	*	ºC/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
OPERATING TEMPERATURE RANGE, case		-25	25	85	*	*	*	°C

NOTES:

1. All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative supply voltages.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
5. Each device in the package is capable of dissipating 45W internally.

CAUTION The PB63 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

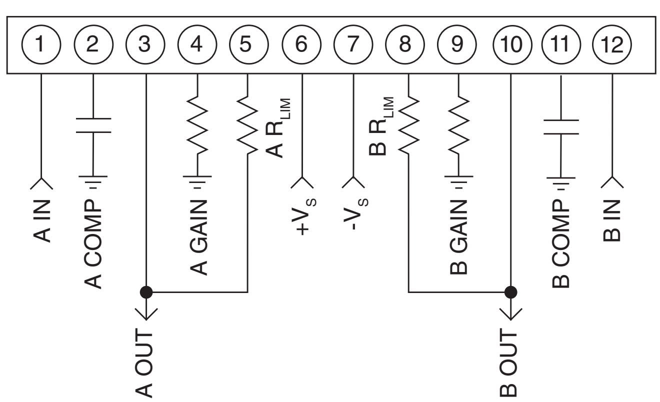
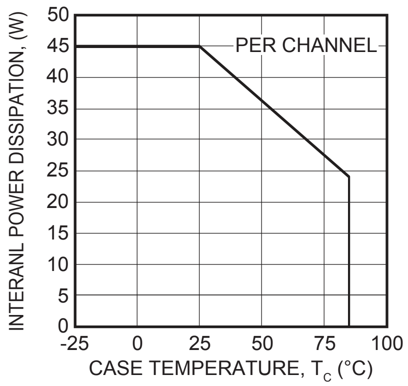


FIGURE 2. External Connections.

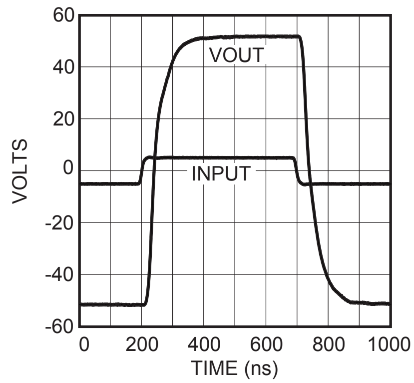
12-pin POWER SIP
PACKAGE STYLE DP

2. TYPICAL PERFORMANCE GRAPHS

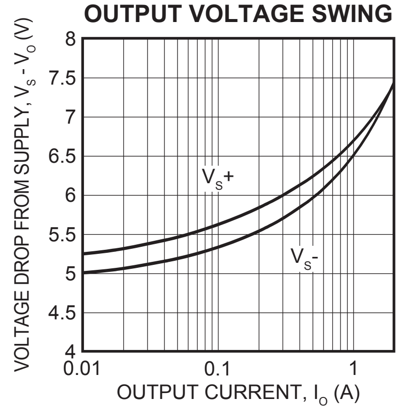
POWER DERATING



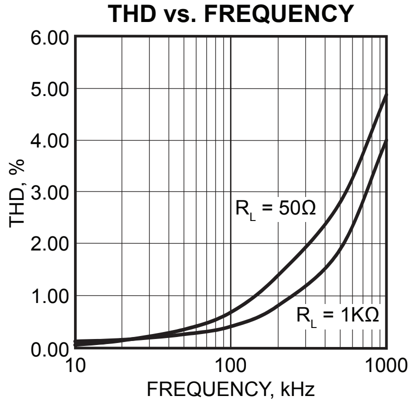
PULSE RESPONSE



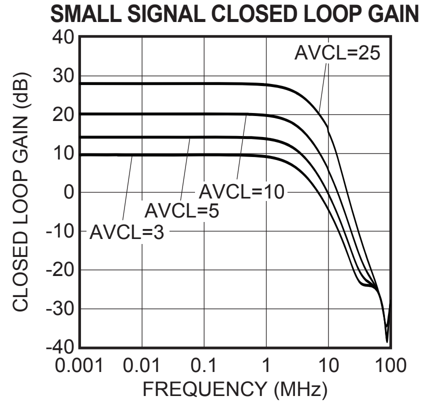
OUTPUT VOLTAGE SWING



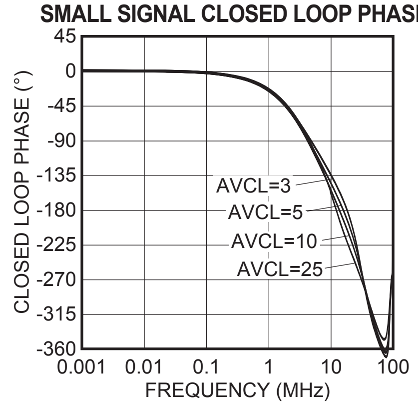
THD vs. FREQUENCY



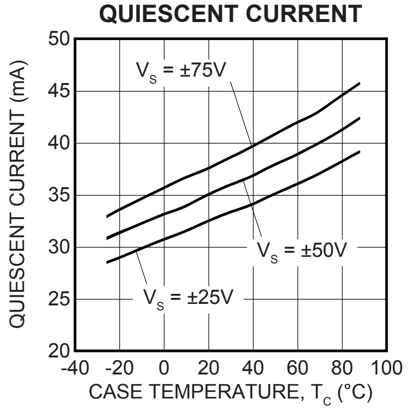
SMALL SIGNAL CLOSED LOOP GAIN



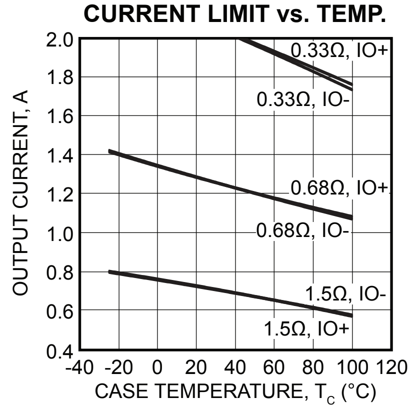
SMALL SIGNAL CLOSED LOOP PHASE



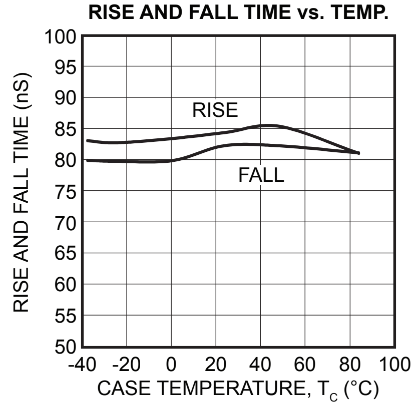
QUIESCENT CURRENT



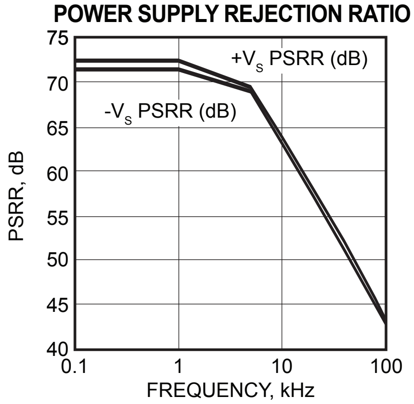
CURRENT LIMIT vs. TEMP.



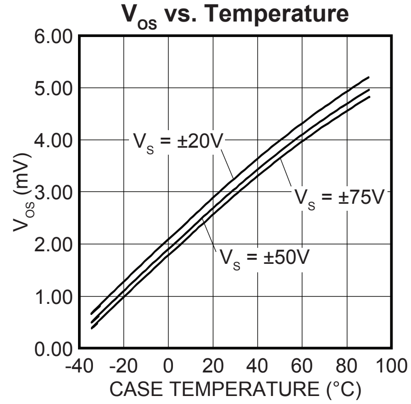
RISE AND FALL TIME vs. TEMP.



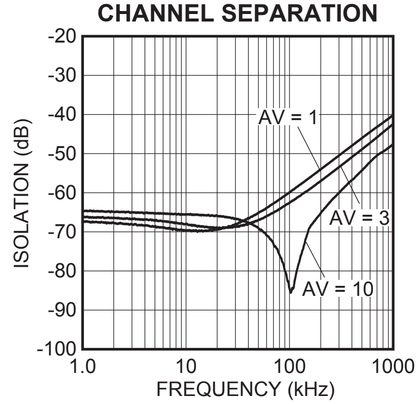
POWER SUPPLY REJECTION RATIO



V_{OS} vs. Temperature



CHANNEL SEPARATION



3. PIN DESCRIPTIONS

Pin #	Pin Name	Description
1	A IN	Signal Input, A channel
2	A COMP	Compensation, A channel
3	A OUT	Load Connection, A channel
4	A GAIN	Gain Setting Resistor connection, A channel
5	A CL	Current Limit Resistor connection, A channel
6	$+V_S$	Positive Power Supply Connection
7	$-V_S$	Negative Power Supply Connection
8	B CL	Current Limit Resistor connection, B channel
9	B GAIN	Gain Setting Resistor connection, B channel
10	B OUT	Load Connection, B channel
11	B COMP	Compensation, B channel
12	B IN	Signal Input, B channel

4. TYPICAL APPLICATION

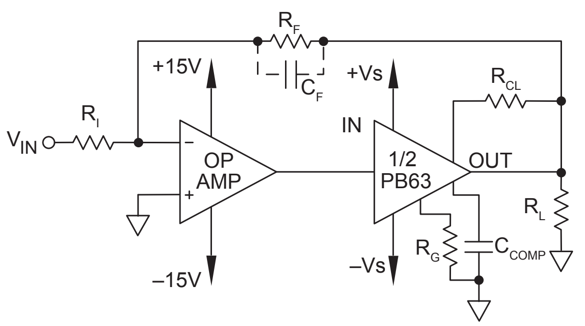


FIGURE 3. Inverting composite amplifier.

5. COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver.

STABILITY

Stability can be maximized by observing the following guidelines:

1. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster. Use the lowest possible booster gain
2. Minimize phase shift within the loop.

A good compromise is to set total (composite) gain at least a factor of 3 times booster gain. Phase shift within the loop is minimized through use of loop compensation capacitor C_F when required. Typical values are 5pF to 33pF. Stability is the most difficult to achieve in a configuration where driver effective gain is unity (i.e.; total gain = booster gain).

BOOSTER GAIN

The gain of each section may be set independently by selecting a value for the gain setting resistor R_G according to the relation: $GAIN = 1 + \frac{2000}{R_G}$ where R_G is in ohms. Recommended gain range is A_V = 3V/V to A_V = 25V/V.

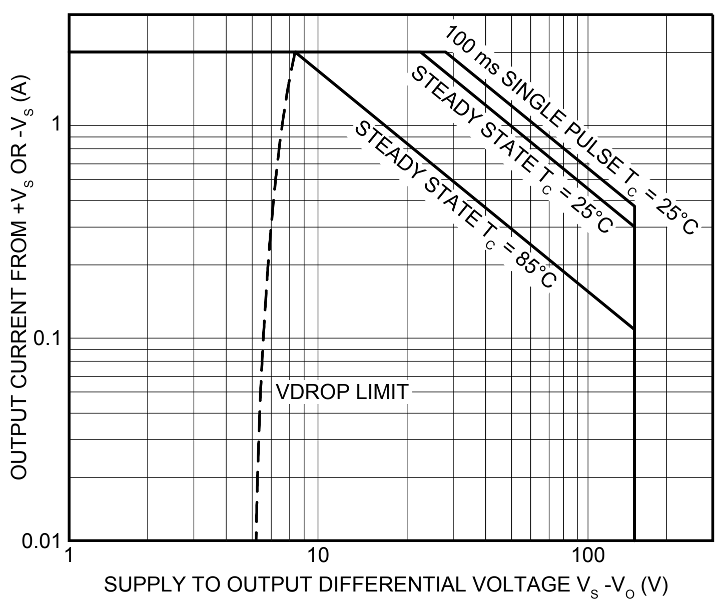
SLEW RATE
The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING
The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The offset voltage of the booster over temperature must be taken into account. Note also that effects of booster gain accuracy should be considered when calculating maximum available driver swing.

6. GENERAL
Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

SAFE OPERATING AREA
The MOSFET output stage of the PB63 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

SOA (PER CHANNEL)



POWER SUPPLY BYPASSING
Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the PB63. Use capacitors of at least 10µF for each supply. Bypass the large capacitors with high quality ceramic capacitors (X7R) of 0.1µF or greater.

CURRENT LIMIT
For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms. The current limit function can be disabled by shorting the CL pin to the OUT pin.

$$R_{LIM} = \frac{0.7}{I_{LIM}}$$

POWER SUPPLY PROTECTION
Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

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