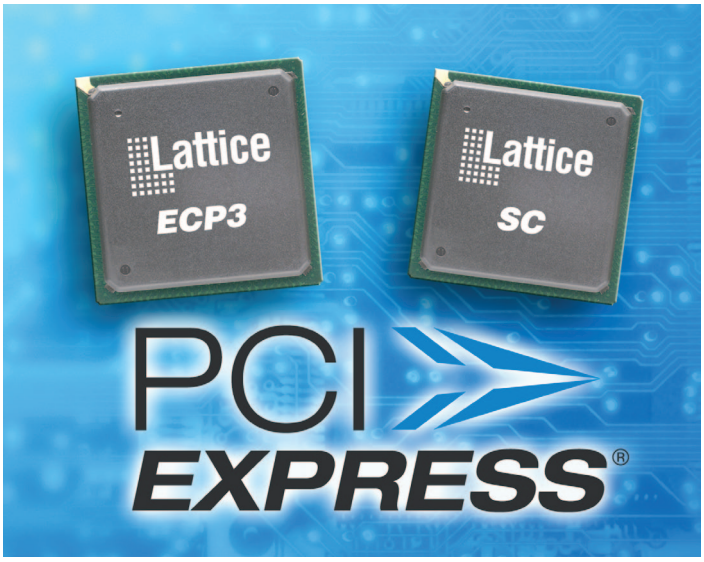
FULLY TESTED AND INTEROPERABLE

Lattice PCIe Solutions

Ready-to-Use PCIe Portfolio

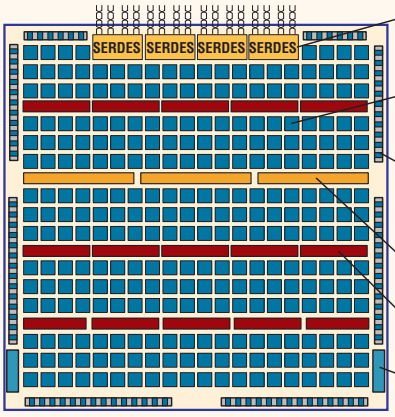
Lattice provides designers with low cost, low power, programmable solutions that are ready-to-use right out of the box. A suite of tested and interoperable solutions is available for PCI Express, including:

- FPGAs with Embedded PCIe-Compliant SERDES
- A Complete Portfolio of Soft and Hard IP Cores for PCI Express x1 and x4 with Scatter Gather DMA
- Application Specific Development Boards and Reference Designs
- A Complete PCI Express Development Kit, Including an Evaluation Board, Software Tools, IP Cores, Demo Designs, GUI, RTL Source, Project Directories, and Documentation
- Test and Interoperability Reports for PMA Electrical Characterization and PCI-SIG Compliance Workshop



Silicon: Industry Leading Programmable PCIe Platforms

LatticeECP3™ Low Cost FPGA



Embedded 3.2Gbps SERDES support PCI Express, Ethernet (XAUI, 1GbE, SGMII), CPRI, OBSAI & 3G/HD/SD-SDI.

Programmable Function Unit (PFU) perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

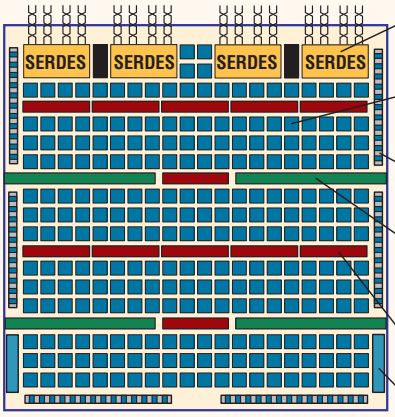
Pre-Engineered Source Synchronous Support implements DDR3 at 800Mbps, SPI4.2 at 700Mbps and generic interfaces up to 1Gbps.

sysDSP™ Blocks implement multipliers, adders, subtractors, accumulators.

sysMEM Embedded Block RAM (EBR) provides 18kbit dual port RAM.

sysCLOCK PLLs & DLLs for clock management.

LatticeSCM™ Extreme Performance FPGA



Quad SERDES + Embedded PCS – each channel runs from 600Mbps to 3.8Gbps with 105mW power dissipation.

Programmable Function Unit (PFU) perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

Programmable I/O Cells (PICs) include PURESPEED™ buffers that support over 20 I/O standards.

Structured ASIC Block (MACO™) provides 50,000 usable gates for increased performance, density and lower power.

sysMEM™ Embedded Block RAM (EBR) provides 18kbit dual port RAM.

sysCLOCK™ PLLs & DLLs for clock management.

LatticeECP3 Features

- Low Cost Digital SERDES
  - Compliant to PCI Express v1.1 electrical specifications
- Up to 16 Channels per Device
  - Useful for multi-protocol bridging
- Complete End-to-End Solution
  - PIPE compliant PCS
  - PCI Express x1 and x4 soft IP available
- Very Low Power (110mW Per Channel Typical @ 3.2Gbps)
- Low-Power, High-Value FPGA Fabric
  - High-end features at low cost

LatticeSC/M Features

- High Performance Analog SERDES
  - Compliant to PCI Express v1.1 electrical specifications
  - Ideal for long PCI Express based backplanes
- Up to 32 Channels per Device
  - Useful for multi-protocol bridging
- Complete End-to-End Solution
  - Rich PCS functionality
  - flexiMAC™ and MACO® LTSSM provide complete PHY and DL functionality in hard gates
  - PCI Express x1 and x4 core available
- Very Low Power (105mW Per Channel Typical @ 3.125Gbps)
- Extreme Performance FPGA Fabric
  - 500MHz block-level performance

Intellectual Property: Rich Portfolio of Hard & Soft IP

Lattice Supplied PCIe Solutions

Soft PCI Express x1 and x4

Platform: ECP3 ECP2M

- Compliant to PCI Express v1.1 Endpoint
- PCI-SIG Compliance Workshop Certified
- Soft Physical, Data Link and Transaction Layers, and 4KB Data Payload Size
- Low LUT Usage (5K LUTs) PCIe x1 Configuration
- Reference Design to Support TLP Termination, Interrupts, Ingress/Egress Datapath and Wishbone Bus Interface

Hard PCI Express x1 and x4

Platform: SCM

- Compliant to PCI Express v1.1 Endpoint Specifications
- PCI-SIG Compliance Workshop Certified
- Physical and Data Link Layer Implemented on MACO Structured ASIC technology
- Soft Transaction Layer and 4KB Data Payload Size
- Reference Design to Support TLP Termination, Interrupts, Ingress/Egress Datapath and Wishbone Bus Interface
- Available in Small Footprint 17x17 mm 256-ball fpBGA Package – 60% Smaller than Competitive Devices
- No IP Licensing Fee

PCS PIPE

Platform: ECP3 ECP2M

- Fully Compliant to PIPE Rev 1.00 Spec
- Standard PCI Express PHY Interface allows for Multiple IP Sources
- Selectable x1, Multiple x1 or x4 PCI Express
- Selectable SERDES Channel for PCI Express x1 Mode
- Clock/Data Recovery from the Serial Stream
- Direct Disparity Control for use in Transmitting Compliance Pattern
- 8b10b Encoder/Decoder & Error Indication
- Receiver Detection
- 2.5GT/s Full-Duplex Rate per Channel

Hard Memory Controller

Platform: SCM

- Supports QDR2/+ SRAM, DDR1/2 and RLDRAM1/2 DRAMs
- DDR1/2 Features:
  - •Data widths of 8-72 bits
  - •Programmable burst lengths of 4 or 8
  - •ODT signal generation
  - •True and complementary DQS during write
  - •Programmable CAS latency
  - •Clock frequency of up to 333MHz (667Mbps throughput)
- QDR2/+ Features:
  - •Configurable data address widths
  - •Programmable burst sizes
  - •Clock frequencies of up to 350Mbps
- RLDRAM1/2 Features:
  - •Supports CIO and SIO configurations
  - •Programmable burst lengths of 2, 4 or 8
  - •Supports two chip selects for cascading devices
  - •Industry's best 800Mbps performance

Soft DDR1, DDR2 and DDR3 Memory Controllers

Platform: ECP3 ECP2M SC/M

- Supports DDR1/2 and DDR3* (*ECP3 only)
- Data Widths of 8-72 Bits
- Up to 4 Chip Selects
- Programmable CAS Latencies of 3, 4, 5 or 6 Cycles
- Programmable Burst Lengths of 4 or 8
- Clock Frequency of Up To 400MHz (800Mbps Throughput)

Scatter Gather DMA Engine

Platform: ECP3 ECP2M SC/M

(LatticeSC/M, ECP3, ECP2M)

- Configurable for Simple, Split and Scatter-Gather DMA transactions
- Supports Up To 16 Physical Channels
- Supports Up To 8 Sub-channels per Physical Channel
- Four Priority Levels With WRR Arbiter
- Wishbone Bus Interface (8-128 bits) with Support for Burst and Classic Cycle Transfer
- Direct Interface to External Packet Buffer
- Autonomous or Hardware Directed Retries
- Supports Centralized and Distributed DMA Architectures

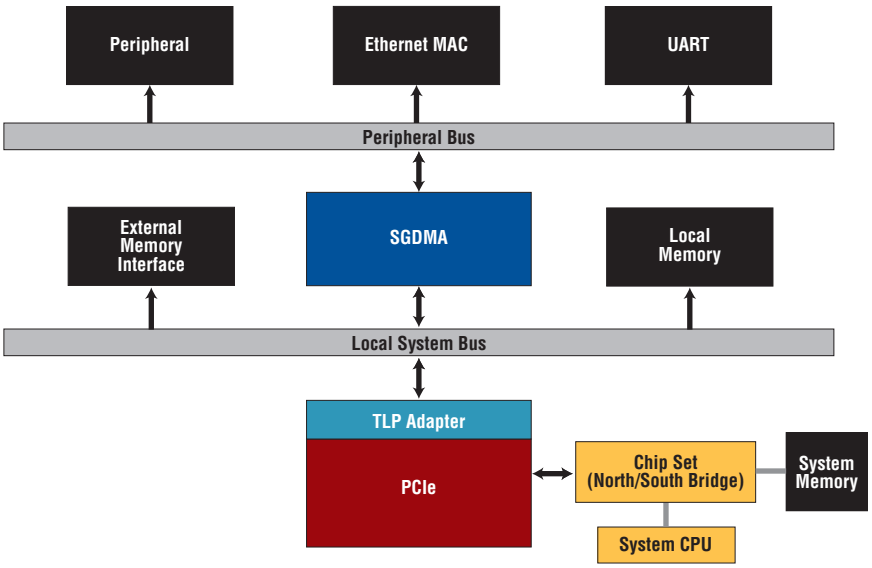
3rd Party Supplied PCIe Solutions

PLDA PCI Express x1 and x4

Platform: ECP2M

- Endpoint-only implementation
  - •Legacy or Native
  - •Compliant to rev. 1.1 of Specification
  - •x1 and x4 implementation
- x4 can initialize in x1
  - •Single Virtual Channel (VC)
  - •Configurable Payload_Size
- 128 Bytes to 2 Kbytes
  - •Up to 8 Outstanding Read Requests
  - •Integrated DMA engine
- 1 to 8 DMA channels
  - • Scatter-Gather support

EXAMPLE PCI EXPRESS ENDPOINT SYSTEM USING LATTICE INTELLECTUAL PROPERTY



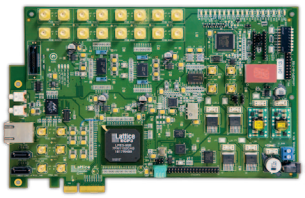
Development & Evaluation Systems

Lattice PCI Express Evaluation Platforms

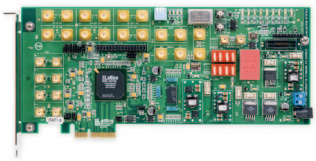
	Kit / Board Name	PCIe Interfaces	Other Interfaces	Memory Interfaces
LatticeECP3 Evaluation Platforms	LatticeECP3 PCI Express Development Kit	• PCI Express x1 and x4 Card Edge Finger	None	• DDR2 Component (18 bit)
	Serial Protocol Board	• PCI Express x4 Card Edge Finger	• SMAs for SERDES (4 channels) • SMAs for LVDS I/O • RJ-45	• DDR3 Component (8 bit) • DDR2 Component (18 bit)
LatticeECP2M Evaluation Platforms	LatticeECP2M PCI Express Development Kit	• PCI Express x1 and x4 Card Edge Finger	None	• DDR2 Component (16 bit)
	PCI Express x4	• PCI Express x4 Card Edge Finger	• SMAs for SERDES (4 channels) • SMAs for LVDS I/O	• DDR2 Component (16 bit)
	SERDES Evaluation	• PCI Express Card Edge Finger	• SMAs for SERDES (4 channels) • RJ-45 • SFP Optical Cage (SGMII) • SATA	• DDR2 Component (16 bit)
LatticeSC/M Evaluation Platforms	PCI Express x4 LFSC80-1152	• PCI Express x4 Card Edge Finger	• SMAs for SERDES (4 channels) • SMAs for LVDS I/O	• DDR2 Component (18 bit)
	PCI Express x1 LFSC25-900	• PCI Express x1 Card Edge Finger	• SFP Optical Cage (SGMII) • RJ-45	• RLDRAM and QDR2 (18 bit)

LatticeECP3 PCI Express Development Kit

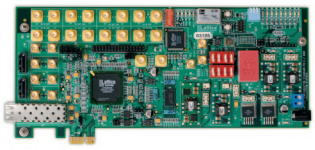
LatticeECP3 Serial Protocol Board



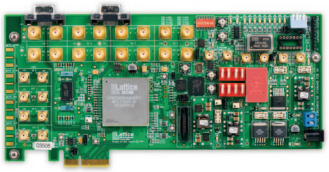
LatticeECP2M PCI Express x4 Evaluation Board



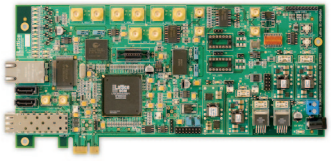
LatticeECP2M SERDES Evaluation Board



LatticeSC™ PCI Express x4 Evaluation Board



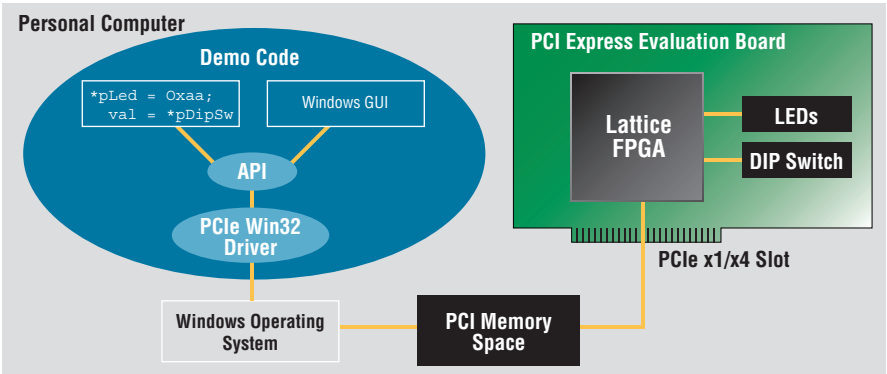
LatticeSC PCI Express x1 Evaluation Board



PCI Express Basic Demo & Throughput Demo

- Includes Hard or Soft PCI Express from Lattice
- Windows and Linux Drivers Included
- Self-Contained Demonstration Software and GUI
- Fully Synthesizable Application Layer Reference Design With:
  - Read and write access to internal EBR memory
  - Real time user interaction to peek and poke registers over the PCIe
- Allows Measurement of Throughput Across the PCI Express Link

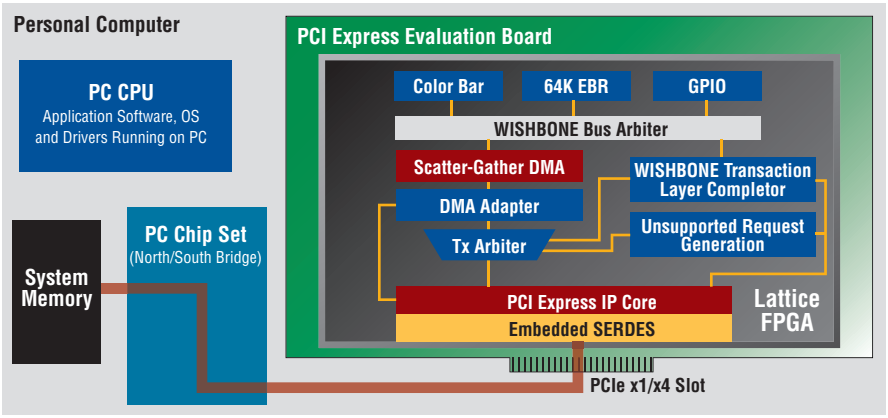
PCI EXPRESS BASIC DEMO



PCI Express DMA Demo

- Integrates PCI Express with SG-DMA Cores Into Single Reference Platform
- Full Ingress and Egress Datapath Support to Handle Requests to/from PC
- Fully Synthesizable TLP Termination and DMA Interface Reference Design

LATTICE PCI EXPRESS DMA DEMO



Testing and Usability

Hardware Testing

Lattice tests all critical components of the PCI Express stack rigorously, and puts a great deal of emphasis on interoperability with proven 3rd party silicon platforms. The following test documentation is available for customer review:

PMA ELECTRICAL CHARACTERIZATION

See technical note TN1084 and supplements (available under NDA) for PCI Express transmit jitter specifications test results.

PCI-SIG TESTING

Lattice is a regular participant of the Compliance Workshop Programs offered by the PCI Special Interest Group (PCI-SIG). Testing is done on Lattice-designed PCI Express Endpoint Add-in cards. All PCI Express Endpoint solutions have undergone rigorous testing and are currently compliant to Version 1.1 of the PCI Express specification. The following test are performed at the SIG:

- Electrical Testing – Examines device and card signal quality for eye pattern, jitter and bit error rate.
- Configuration Space Testing – Examines configuration space in the device by verification of required fields and values
- Link and Transaction Protocol Testing – Tests device behavior for link-level and transaction layer protocols.

INTEROPERABILITY

Lattice PCI Express solutions undergo peer-to-peer compatibility tests with various motherboards and root complexes. These tests are held internally as well as at the PCI-SIG Compliance Workshops. Lattice PCI Express solutions have successfully interoperated with a number of motherboards using a variety of processors and root complex chips.

A technical note summarizing the setup and results of PCI-SIG testing and interoperability exercises can be found on the Lattice website (www.latticesemi.com) in technical note TN1166.

Lattice IPexpress™ Tool

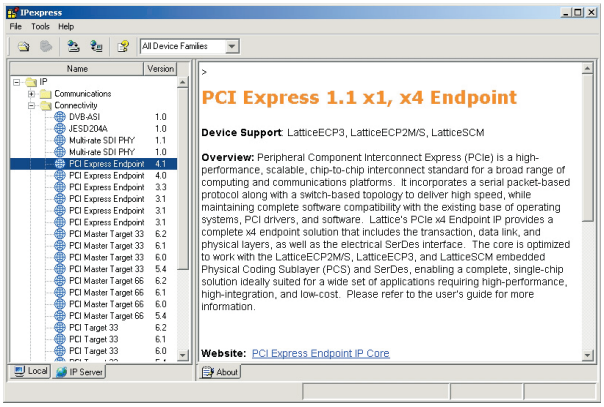
The IPexpress tool revolutionizes the way users design with Lattice IP cores and greatly simplifies IP design. The IPexpress design flow enables users to fully parameterize IP at design time. The designer can then instantiate the user-configured IP and complete the design process, including full timing simulation and bitstream generation.

VIEW IP CORES AVAILABLE FOR DOWNLOAD

From the Lattice IP Server Tab within IPexpress, you can view available ispLeverCORE™ user-configurable IP cores for download.

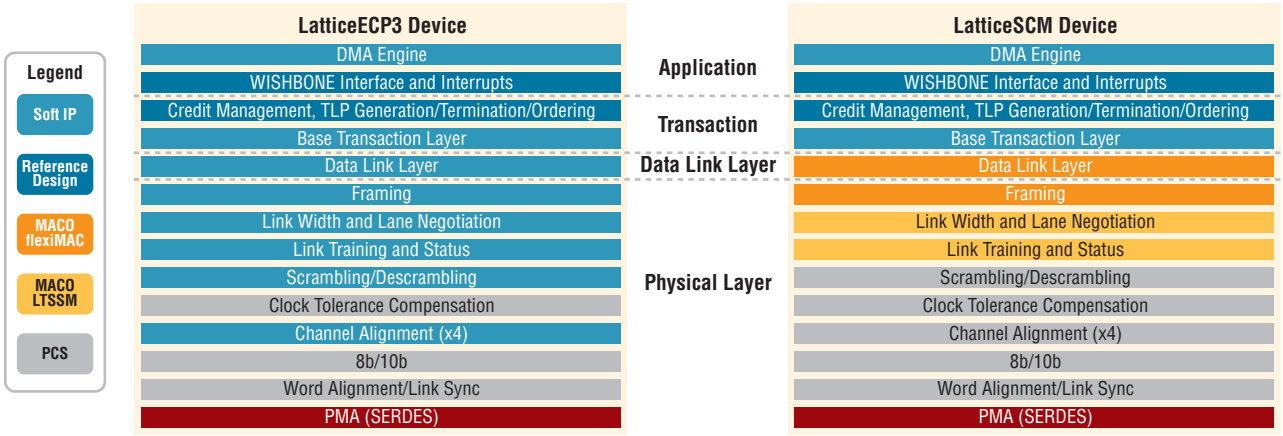
INSTALL OR DOWNLOAD IP CORES

You can download and install ispLeverCORE user-configurable IP cores on your computer, or you can simply download them and install them later.



Lattice's IPexpress tool can be used to easily configure both MACO hard IP and Lattice's growing selection of soft IP cores.

Lattice PCI Express Solution Guide



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