Dual bidirectional I²C-bus and SMBus voltage-level translator

Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I2C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I2C-bus and SMBus compatible
- Less than 1.5 ns maximum propagation delay to accommodate Standard mode and Fast mode I2C-bus devices and multiple masters
- Allows voltage level translation between:
  - 1.0V V_{REF1} and 1.8 V, 2.5 V, 3.3 V or 5 V V_{REF2}
  - 1.2 V VREF1 and 1.8 V, 2.5 V, 3.3 V or 5 V VREF2
  - 1.5 V VREF1 and 2.5 V, 3.3 V or 5 V VREF2
  - 1.8 V VREF1 and 3.3 V or 5 V VREF2
  - 2.5 V VREF1 and 5 V VREF2
  - 3.3 V VREF1 and 5 V VREF2
- Provides bidirectional voltage translation with no direction pin
- Low 3.5 ohm ON-state connection between input and output ports provides less signal distortion
- Open-drain I2C-bus I/O ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V tolerant I2C-bus I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Lock-up free operation for isolation when EN = LOW
- Flow through pin out for ease of printed-circuit board trace routing
- ESD protection exceeds 4KV HBM per JESD22-A114
- Package: TDFN2x3-8L, USOP-8L and SOIC-8L

Description

The PI6ULS5V9306 is a dual bidirectional I²C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.3 V (VREF1) and 1.8 V to 5.5 V(VREF2).

The PI6ULS5V9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The PI6ULS5V9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The PI6ULS5V9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

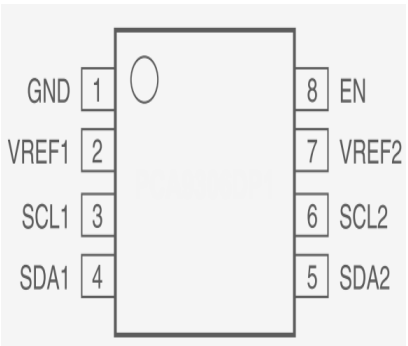
The PI6ULS5V9306 can also be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PI6ULS5V9306 has a standard open-collector configuration of the I²C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I²C-bus devices in addition to SMBus devices.

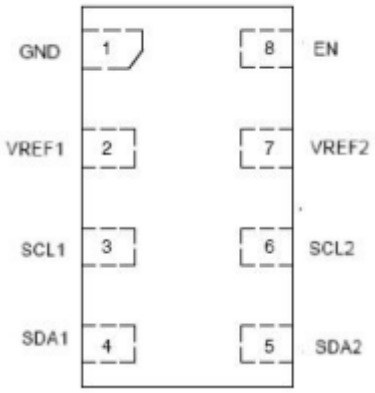
When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH , the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

Pin Configuration



SOIC-8L/USOP-8L(Top View)

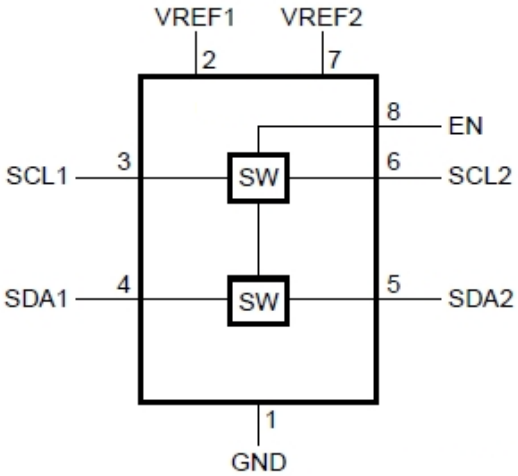


TDFN2x3-8L(Top View)

Pin Description

Pin No	Name	Description
1	GND	ground (0 V)
2	VREF1	low-voltage side reference supply voltage for SCL1 and SDA1
3	SCL1	serial clock, low-voltage side; connect to VREF1 through a pull-up resistor
4	SDA1	serial data, low-voltage side; connect to VREF1 through a pull-up resistor
5	SDA2	serial data, high-voltage side; connect to VREF2 through a pull-up resistor
6	SCL2	serial clock, high-voltage side; connect to VREF2 through a pull-up resistor
7	VREF2	high-voltage side reference supply voltage for SCL2 and SDA2
8	EN	switch enable input; connect to VREF2 and pull-up through a high resistor

Block Diagram



EN	Function
H	SCL1 = SCL2; SDA1 = SDA2
L	disabled

Figure.1Block Diagram

Maximum Ratings

Storage Temperature	-65°C to +150°C
Reference Voltage(2)	-0.5V to +6.0V
Reference bias voltage	-0.5V to+6.0V
DC Input Voltage	-0.5V to +6.0V
Control Input Votage(EN)	-0.5V to+6.0V
channel current (DC)	128mA
Input clamping Current	-50mA
ESD: HBM Mode	4000V

Note:
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

Recommended operation conditions

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_A = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{I/O}$	Voltage on an input/output pin	SCL1, SDA1, SCL2, SDA2	0	-	5	V
V_{REF1}	Reference voltage (1)	VREF1	0	-	5	V
V_{REF2}	Reference bias voltage (2)	VREF2	0	-	5	V
$V_{I(EN)}$	Input voltage on pin EN	-	0	-	5	V
$I_{(pass)}$	Pass switch current	-	-	-	64	mA
T_A	Ambient temperature	-	-40	-	85	°C

DC Electrical Characteristics

T_A = -40 °C to +85 °C; unless otherwise specified

Parameter	Description	Test Conditions(1)		Min	Typ.(2)	Max	Unit
Input and output SDAB and SCLB							
V_{IK}	input clamping voltage	I_I = -18mA; $V_{I(EN)}$ = 0 V		-	-	-1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; $V_{I(EN)}$ = 0 V		-	-	5	µA
$C_{i(EN)}$	input capacitance on pin EN	V_I = 3 V or 0 V		-	11	-	pF
$C_{io(off)}$	off-state input/output capacitance (SCLn, SDAn)	V_O = 3 V or 0 V; $V_{I(EN)}$ = 0 V		-	4	-	pF
$C_{io(on)}$	on-state input/output capacitance (SCLn, SDAn)	V_O = 3 V or 0 V; $V_{I(EN)}$ = 3 V		-	10.5	-	pF
Ron	ON-state resistance(2) (SCLn, SDAn)	V_I = 0V; I_O = 64mA	$V_{I(EN)}$ = 4.5 V	-	3.5	5.5	Ω
			$V_{I(EN)}$ = 3 V	-	4.7	7.0	Ω
			$V_{I(EN)}$ = 2.3 V	-	6.3	9.5	Ω
			$V_{I(EN)}$ = 1.5 V	-	60	140	Ω
		V_I = 2.4V; I_O = 15mA	$V_{I(EN)}$ = 4.5 V	1	6	15	Ω
			$V_{I(EN)}$ = 3 V	20	60	140	Ω
		V_I = 1.7V; I_O = 15mA	$V_{I(EN)}$ = 2.3 V	20	60	140	Ω

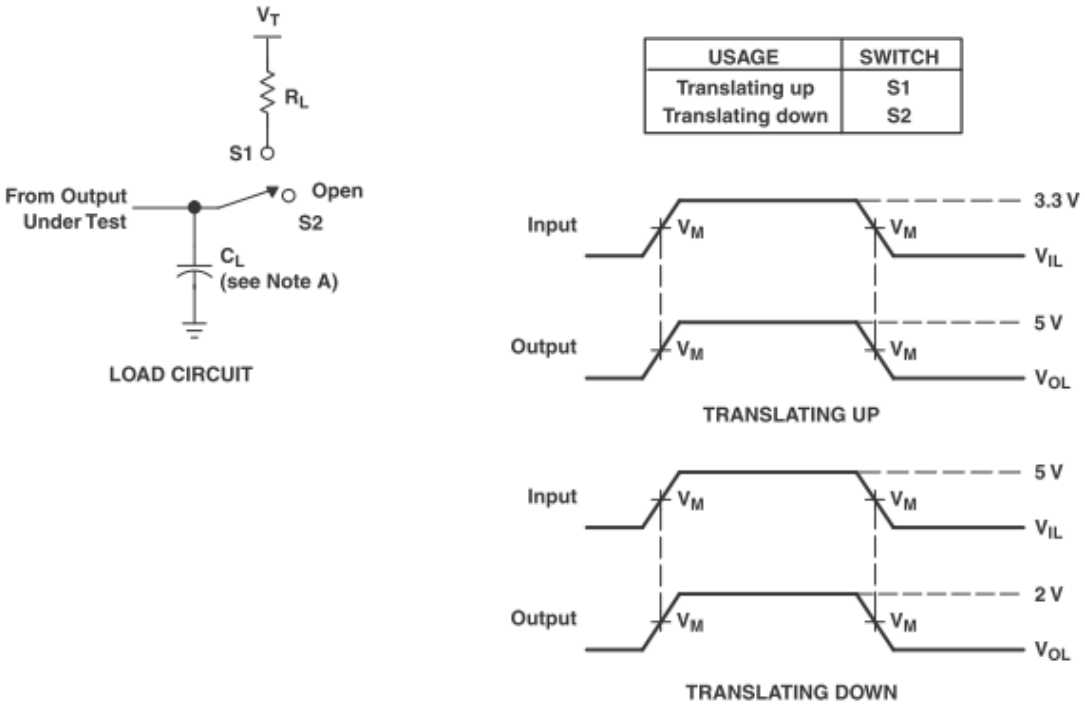
Notes:
1) All typical values are at T_A = 25 °C.
2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

Dynamic characteristics

T_A = -40 °C to +85 °C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)}$ = 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.2	0	1	0	0.5	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 0.75 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.3	0	1	0	0.6	ns
$V_{I(EN)}$ = 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_T = 3.3 V; V_M = 1.15 V; R_L = 300 □									
t_{PLH}	LOW-to-HIGH propagation delay	ffrom (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.4	0	1.1	0	0.7	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_T = 2.5 V; V_M = 0.75 V; R_L = 300 □									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.3	0	1.3	0	0.8	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure.2 Load Circuit for Outputs

Functional Description

The PI6ULS5V9306 is a dual bidirectional I^2C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2 V to 3.3 V (VREF1) and 1.8 V to 5.5 V(VREF2).

The PI6ULS5V9306 allows bidirectional voltage translations between 1.2 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The PI6ULS5V9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The PI6ULS5V9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The PI6ULS5V9306 can also be used to run two buses, one at 400kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I^2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PI6ULS5V9306 has a standard open-collector configuration of the I^2C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I^2C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

Application Information

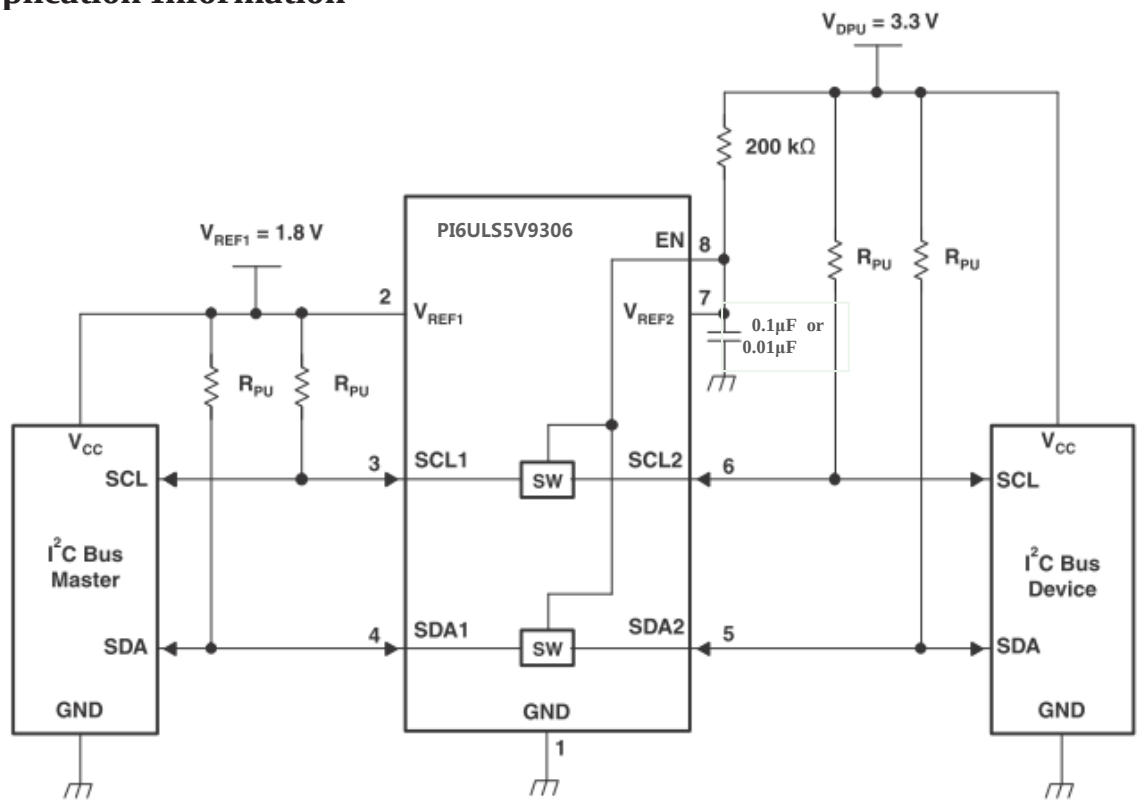


Figure.3 Typical Application Circuit (Switch Always Enabled)

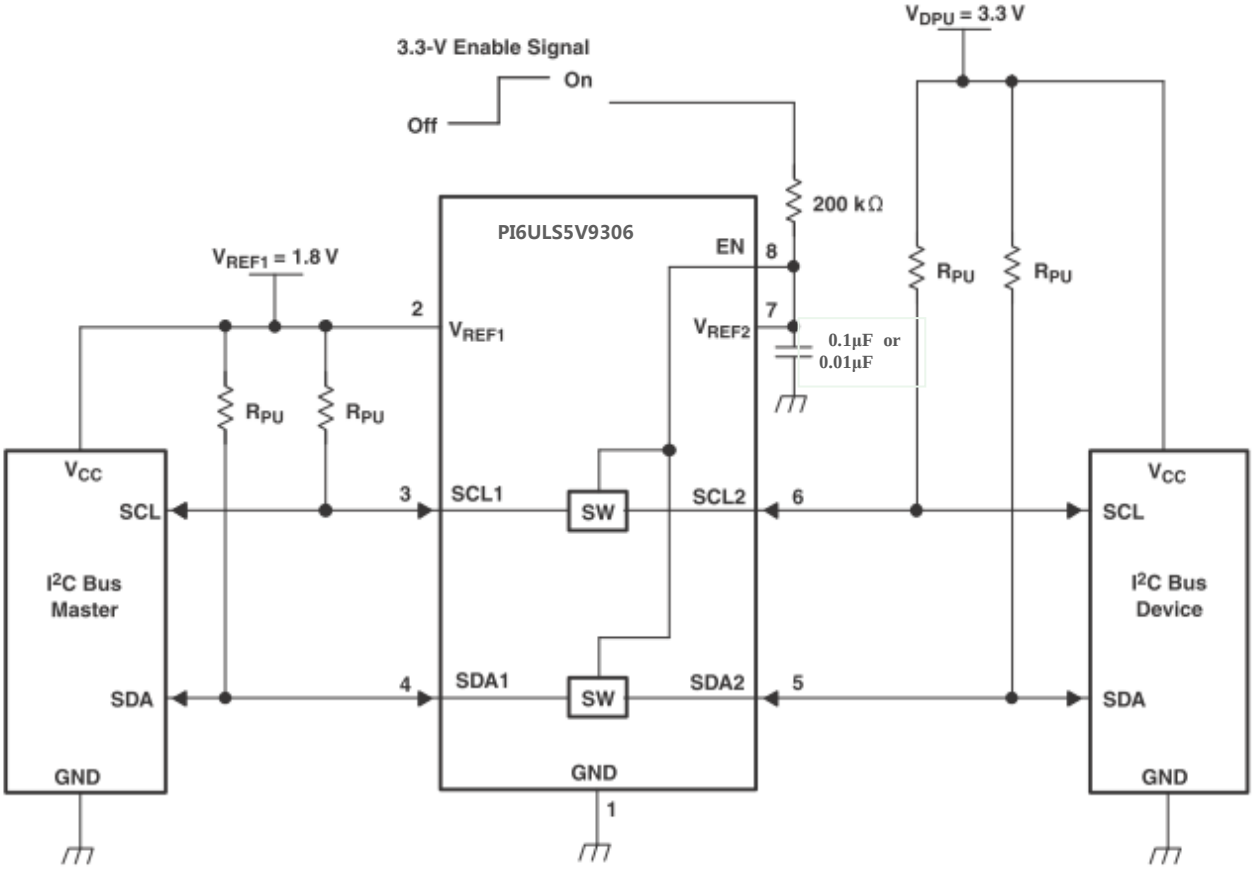


Figure.4 Typical Application Circuit (Switch Enabled Control)

Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pull-up resistor (typically 200 kΩ). This allows V_{REF2} to regulate the EN input. A filter capacitor on V_{REF2} is recommended. The I^2C bus master output can be totem pole or open drain (pull-up resistors may be required) and the I^2C bus device output can be totem pole or open drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open drain, no direction control is needed.

Application Operating Condition

Refer to Figure 3

Symbol	Parameter	Min	Typ	Max	Unit
V_{REF2}	Reference voltage	VR_{EF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	0	1.5	4.4	V
I_{PASS}	Pass switch current	-	14	-	mA
I_{REF}	Reference-transistor current	-	5	-	µA
T_A	Operating free-air temperature	-40	-	85	℃

Sizing Pull-up Resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35\ V}{0.015\ A}$$

The following table summarizes resistor values, reference voltages, and currents at 15mA, 10mA, and 3mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PI6ULS5V9306 device at 0.175 V, although the 15 mA applies only to current flowing through the PI6ULS5V9306 device.

PULLUP RESISTOR VALUES

Calculated for V_{OL} = 0.35 V; Assumes output driver V_{OL} = 0.175 V at stated current

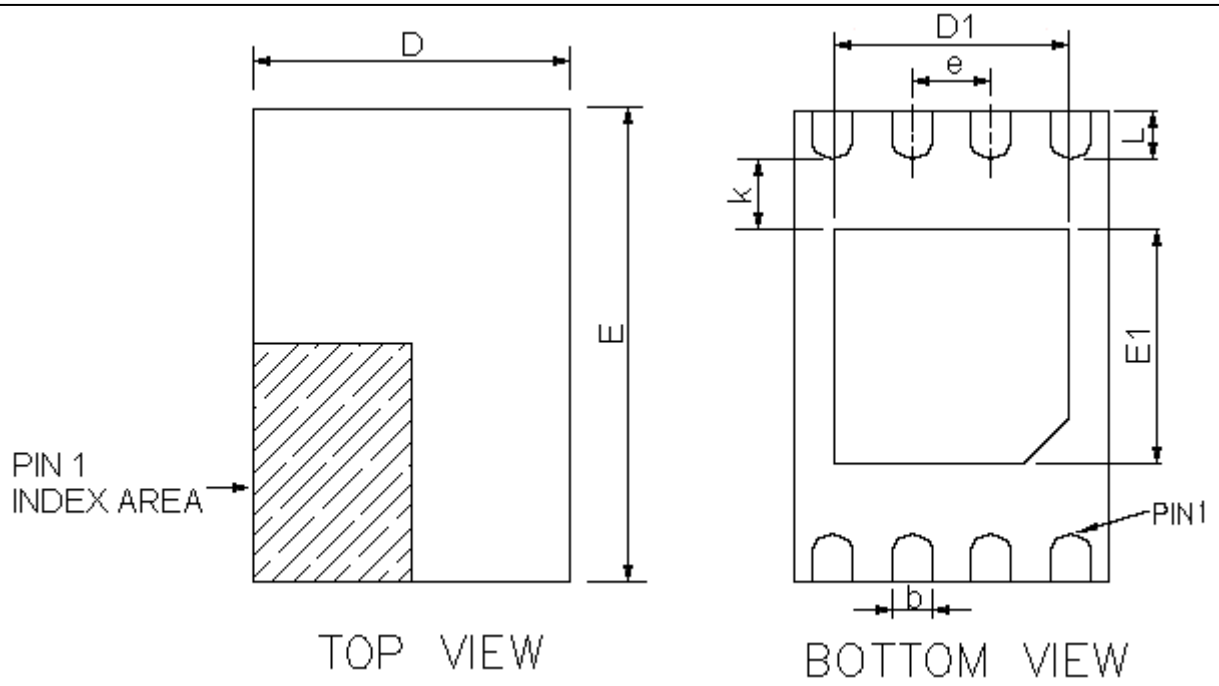
PULLUP RESISTOR VALUE						
V_{DPU}	**15 mA**		**10 mA**		**3 mA**	
	NOMINAL	**+10%** (1)	**NOMINAL**	**+10%** (1)	**NOMINAL**	**+10%** (1)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

NOTES:

1)+10% to compensate for V_{DD} range and resistor tolerance

Mechanical Information

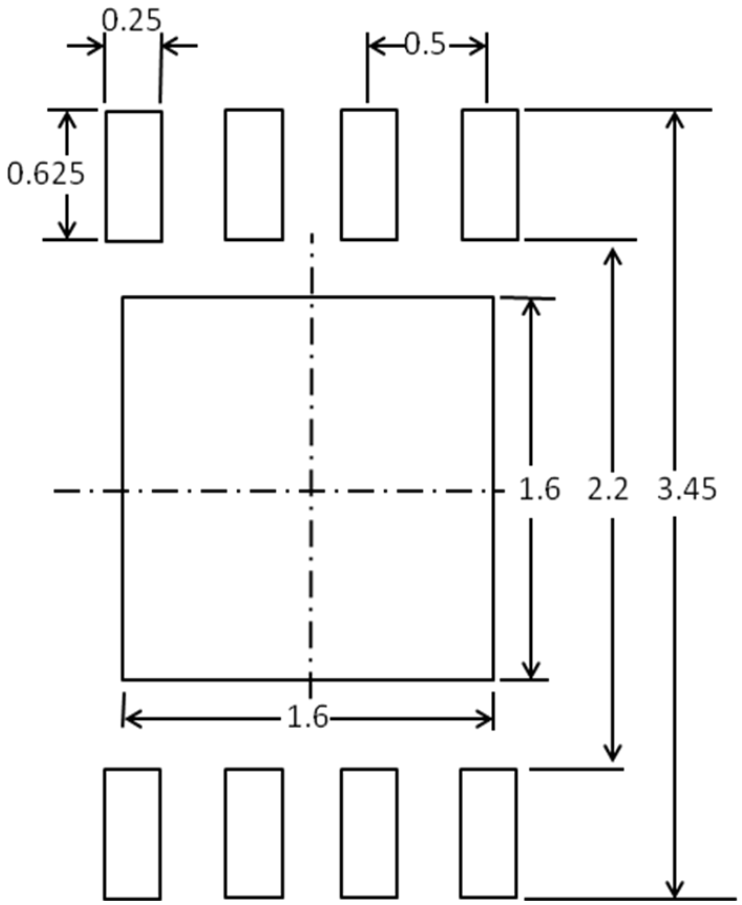
TDFN2x3-8L



PKG. DIMENSIONS(MM)		
SYMBOL	MIN.	MAX
A	0.70	0.80
A1	0.00	0.50
A3	0.20REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20MIN	
b	0.20	0.30
e	0.50TYP	
L	0.22	0.38

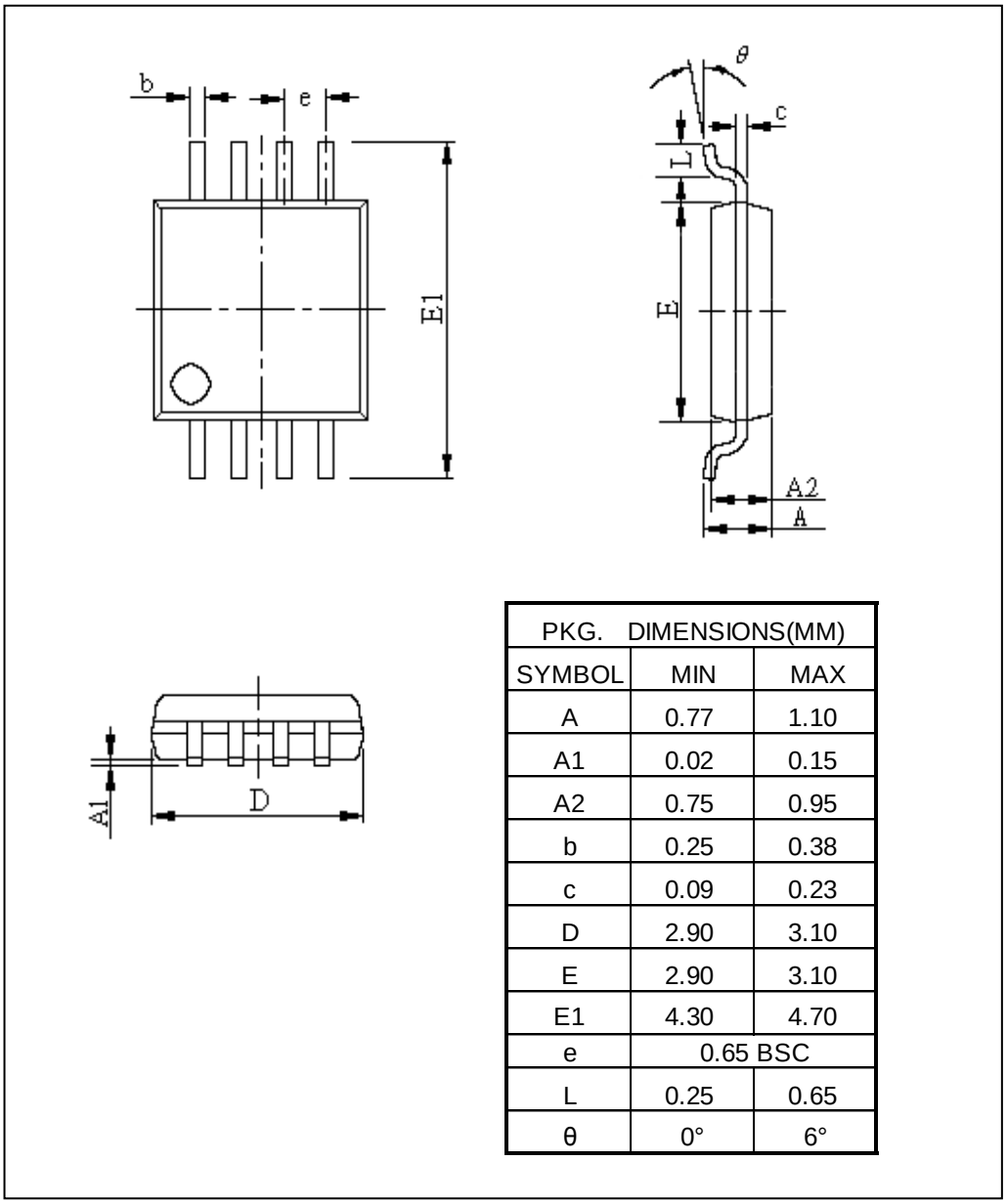
Note:
Ref: JEDEC MO-229

Recommended Land pattern for TDFN2x3-8L



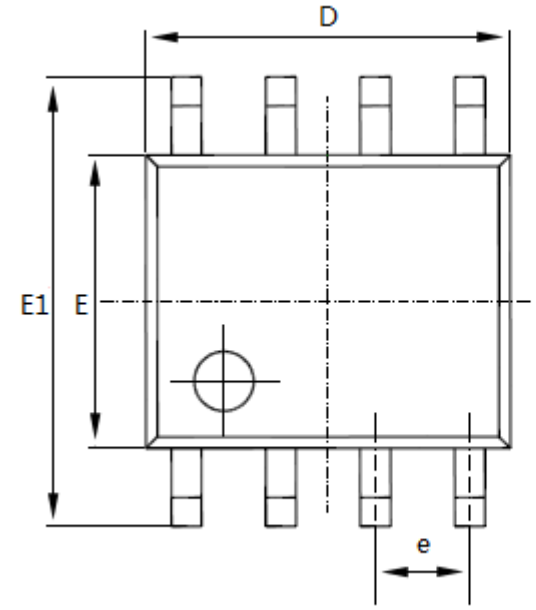
Note:
All linear dimensions are in millimeters

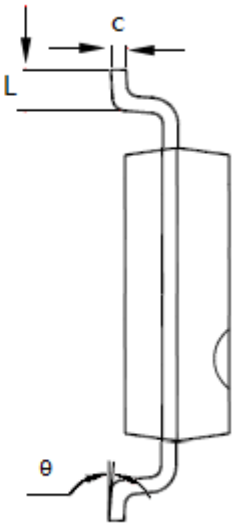
USOP-8L

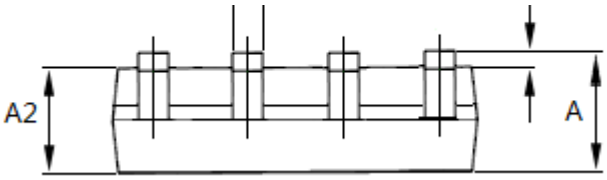


PKG.	DIMENSIONS(MM)	
SYMBOL	MIN	MAX
A	0.77	1.10
A1	0.02	0.15
A2	0.75	0.95
b	0.25	0.38
c	0.09	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.30	4.70
e	0.65 BSC	
L	0.25	0.65
θ	0°	6°

SOIC-8L







Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-012E/AA

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
e	1.27 BSC	
L	0.400	1.270
θ	0°	8°

Ordering Information

Part No.	Package Code	Package
PI6ULS5V9306ZEE	ZE	Lead free and Green TDFN2x3-8L
PI6ULS5V9306UAE	UA	Lead free and Green USOP-8L
PI6ULS5V9306WE	W	Lead free and Green SOIC-8L

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel