QorIQ Qonverge Platform

QorIQ Qonverge BSC9131 RDB for Femtocell Base Station Development

A new dimension in wireless processing

Target Applications

- Wireless infrastructure: 32-user eNodeB femtocell base stations
- Radio communications systems
- Test equipment: Network simulators for 3G and 4G technologies

Overview

The QorIQ Qonverge BSC9131 reference design board (RDB) application development system enables development of L1, L2 and L3 protocol stacks and applications ported above L3. The BSC9131 RDB also verifies BSC9131 QorIQ processor device operation and provides a high level of end-to-end system performance characterization.

The highly integrated BSC9131 targets the evolving small cell base station market and combines the e500 Power Architecture® CPU and SC3850 StarCore DSP with MAPLE-B2F baseband acceleration processing elements. Together, they address the need for a high-performance, cost-effective, integrated solution that handles all required processing layers without the need for additional external processing devices.

At the heart of this development system is Freescale's BSC9131 SoC, featuring:

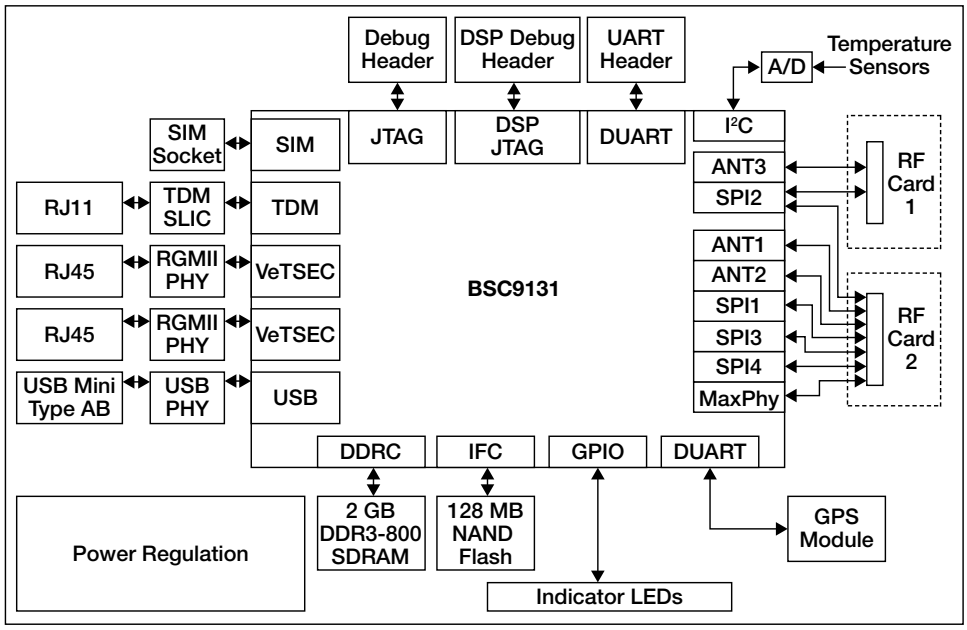
- High-performance 32-bit e500 core built on Power Architecture technology
  - 36-bit physical addressing
  - Double precision floating point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache
  - Enhanced hardware and software debug support
  - 800 MHz to 1 GHz clock frequency
  - 256 KB L2 cache with ECC, also configurable as SRAM and stashing memory
- One SC3850 core subsystem, which connects to the following:
  - 32 KB 8-way L1 instruction/data cache
  - 512 KB 8-way L2 unified instruction/data cache
  - Memory management unit
  - Enhanced programmable interrupt controller
  - Debug and profiling unit
  - Two 32-bit timers
- Multi Accelerator Platform Engine (MAPLE) for femtocell base stations
  - Baseband processing (MAPLE-B2F)
  - Supports variable sizes in Fourier transforms, convolution, filtering, turbo, Viterbi and chiprate
  - Consists of accelerators for UMTS chip rate processing, LTE UP/DL channel processing, matrix inversion operations and CRC algorithms
- DDR3/DDR3L SDRAM memory controller supports 16-bit with ECC and 32-bit without
- Rich set of peripherals perfectly suited for residential femtocell applications

freescale™
QorIQ Qonverge

Features

- High-performance QorIQ Qonverge BSC9131 integrated SoC for wireless infrastructure applications
- End-to-end development system for LTE-FDD/TDD, WCDMA (HSPA+) and CDMA2K, including the RF module for LTE and WCDMA (HSPA+) technologies (provided separately)
- Simultaneous dual mode operation, such as LTE-FDD + WCDMA (HSPA+)
- FCC certified
- Rich ecosystem with partners in OS, modem protocol stack and RF transceivers
- VortiQa software for enterprise equipment optimized for multicore processors

BSC9131 RDB + RF Block Diagram



Specifications

Processor	One e500 processor built on Power Architecture® technology and 256 KB shared L2 cache. StarCore SC3850 DSP subsystem including 512 KB private L2 cache
12V DC Power	12V DC @ 5.5A, 100–240V AC input
Ethernet (WAN)	RJ-45 jack
Memory	4 x 1 GB DDR3, 128 MB NAND flash
SIM Card	1.3/3.8V
Ethernet (Local Net)	RJ-45 jack
VoIP Handset	RJ-11 jack
USB	Mini-AB socket
GPS Antenna	SMA or MCX female
RF Card 1 Antenna(s)	Dual SMA female
RF Card 2 Antenna(s)	Dual SMA female
Operating Temperature	0°C to 40°C, Humidity 5% to 95% RH
Storage Temperature	-20°C to +70°C (-4°F to +158°F)

For more information about the QorIQ Qonverge BSC913x family, visit freescale.com/QorIQQonverge

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