

Platform Manager

Transforms Board Management Design

Platform Manager™ devices feature programmable analog, with a CPLD and FPGA blocks all in one package to integrate power and digital board management functions. The Platform Manager provides a flexible solution that can be used across a wide variety of systems as a standard instead of unique combinations of ICs for each design.

By integrating power and digital support functions, Platform Manager devices provide a lower-cost solution than traditional approaches. They also improve system reliability and provide a high degree of design flexibility, minimizing the risk of circuit board re-spins.

Power management functions include monitoring, MOSFET OR'ing, hot-swap control, power feed, supply sequencing, voltage scaling, VID control, trimming and margining functions. Digital board management functions include reset distribution, power-on configuration, I²C/SPI interface, fault logging, and glue logic.



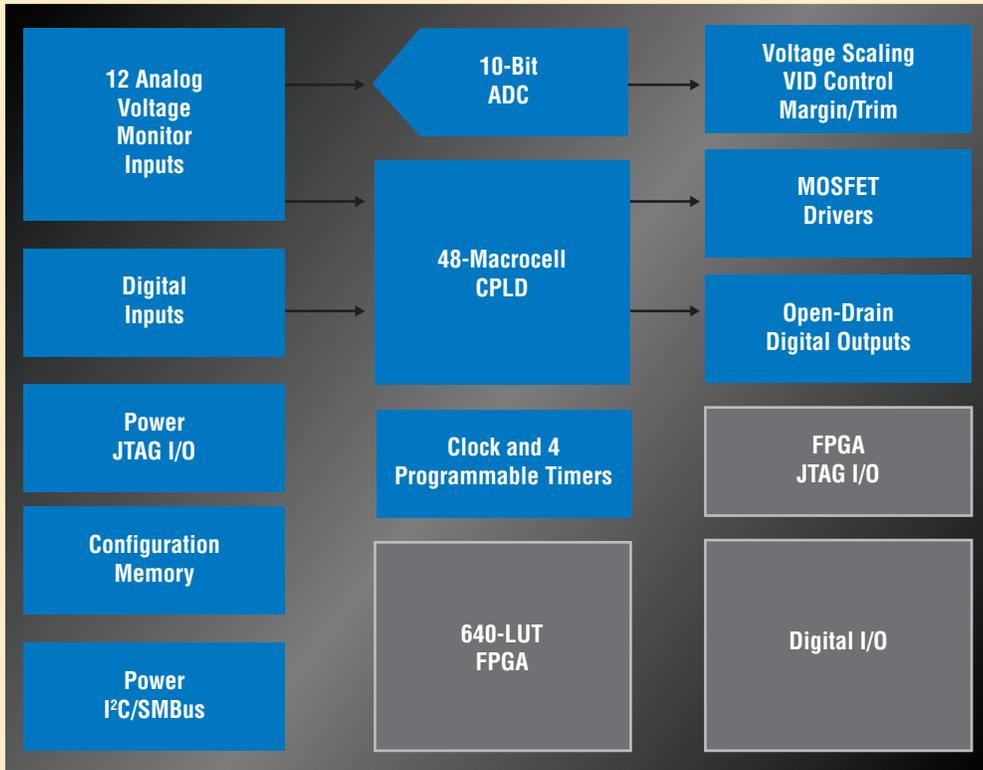
INCREASES RELIABILITY	<ul style="list-style-type: none"> 12 differential input voltage monitors Fast and accurate response (<65 μs; 0.7% max error) Closely integrated power and digital management functions Eliminates discrete components
LOWERS COST	<ul style="list-style-type: none"> Reduce BOM cost up to 50% versus multiple ICs Reduced number of BOM items Reduced board area saves additional cost
REDUCES RISK	<ul style="list-style-type: none"> Simulation reduces design errors before board layout Re-programmability minimizes risk of board re-spins Significantly reduces time-to-market
COMPLEX PLATFORM MANAGEMENT	<ul style="list-style-type: none"> Expandable up to 36 power supplies Up/down close loop sequencing Non-volatile logging of any power fault

Key Features and Benefits

- Precision Voltage Monitoring Increases Reliability**
 - 12 analog monitor inputs
 - Differential input sensing
 - Over/under voltage detection
 - Window comparison options
 - 10-bit voltage measurement ADC
- High-Voltage FET Drivers Enable Integration**
 - 4 N-channel MOSFET drivers
 - Digitally controlled power supply ramp control
 - Programmable current and voltage gate drive
 - Open drain output support
- Margining and Trimming Improves Supply Headroom**
 - Up to eight power supplies
 - Dynamic voltage control
 - Digital closed-loop mode of operation
 - Voltage scaling and VID control
- Programmable Timers Increase Control Flexibility**
 - Four independent timers
 - 32 μs to 2 seconds
 - Internal clock
- PLD Resources Integrate Power & Digital Functions**
 - 48-macrocell CPLD
 - 640-LUT FPGA
 - Up to 6.1 Kbits distributed RAM
 - Up to 107 digital I/Os
 - LVC MOS 3.3/2.5/1.8/1.5/1.2
 - LV TTL
 - Open-drain outputs
- System Level Support**
 - Single 3.3V supply operation
 - Industrial temperature range
- In-System Re-programmability Reduces Risk**
 - On-chip configuration memory
 - JTAG programming interface
- Fail-safe Sequencing**

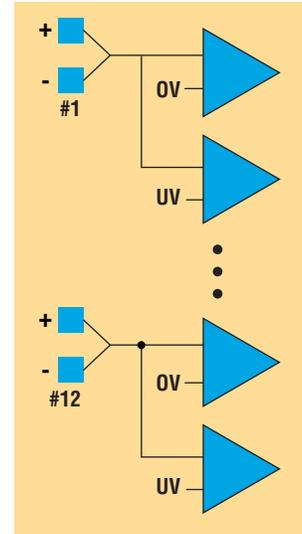
Architecture

Platform Manager Block Diagram



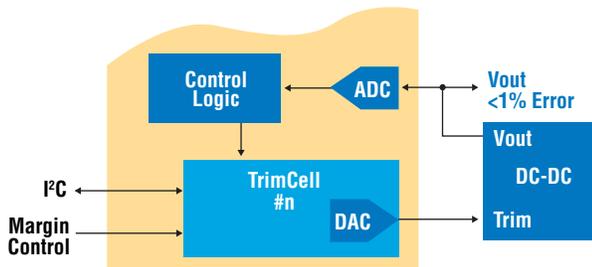
Programmable Supervisors

- 12 Analog Inputs
- Differential Sensing
- 24 Precision Comparators
- Programmable Threshold
- 368 Steps
- Accuracy 0.7% Max (0.2% Typ)



8 Power Supply Voltage Control

- Accurately Set DC-DC Voltages
- Trim & Margining Control
- Voltage Scaling and VID Control



4 N-Channel MOSFET Drive

- Charge Pump Output
- Programmable source and sink currents
- Programmable voltage up to 12V

Power Control

- 48 macrocell CPLD
- Fully synchronous design
- Ruggedized architecture
- Derived from ispMACH[®] 4000
- Predictable fast timing

Voltage and Current Measurement

- 10-bit resolution
- Measure analog voltage inputs
- I²C interface

Digital Control

- 640 LUT FPGA
- 91 I/Os
- 4 clocks
- 150 MHz operation
- Derived from MachXO™

POWER MANAGEMENT

- Hot-Swap Controller
- Power Supply OR'ing
- Voltage & Current Monitoring
- Sequence Control
- Reset Generation
- Voltage Scaling / VID Control
- Trimming & Margining



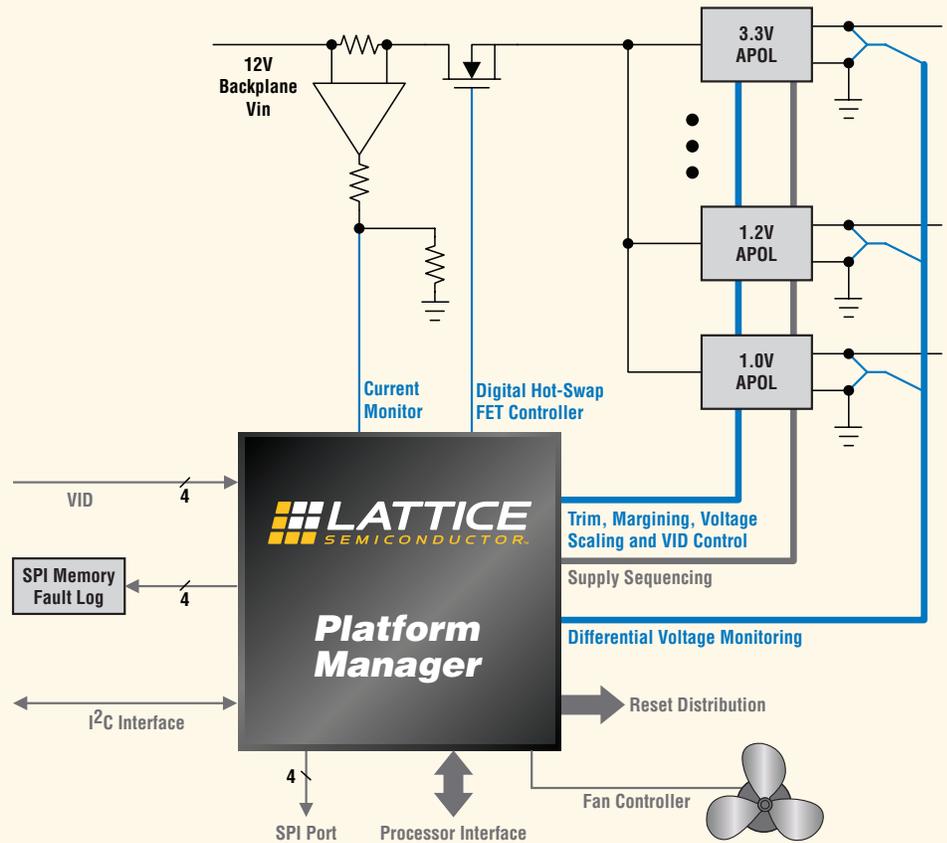
DIGITAL MANAGEMENT

- Power-on Configuration
- Reset Distribution
- Fault Logging
- System Interface

Applications

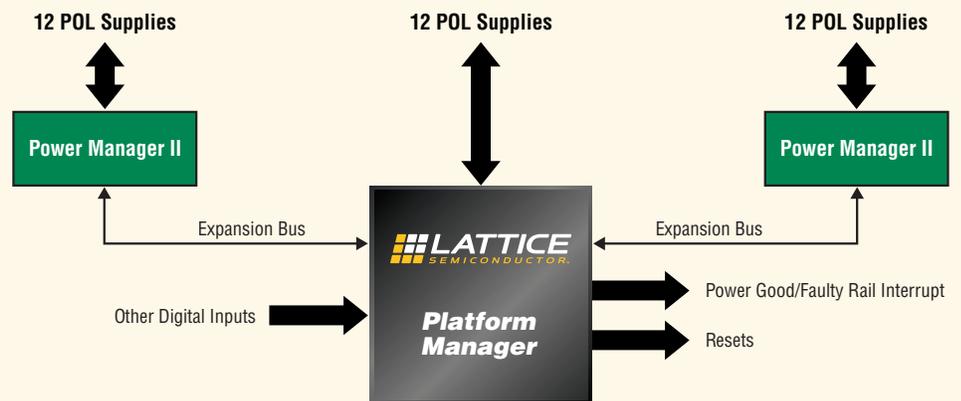
Platform Manager Functions

- Detect Faults Across 12 Supplies
- Margin and Trim up to 8 Supplies
- Capture and Log Faults to Non-Volatile Memory
- 4 Hot-Swap Controllers
- Flexible Reset Distribution
- Configuration of Payload ICs at Power-on
- Voltage Scaling / VID Control
- Fan Control

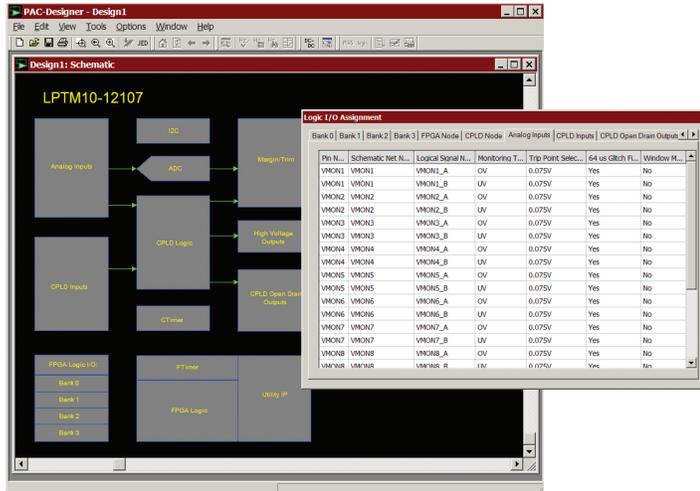


Centralized Monitoring and Sequencing of up to 36 POL Power Supplies

- Distributed Power and Rail Sense
- Monitors Either Digital or Analog Point of Load Power Supplies
- Forward and Reverse Sequencing All Power Supplies
- Capture Any Fault in Non-Volatile Memory
- Field Upgradable with Fail-safe Sequence Backup
- Flexible Power Good/Fault Rail Interrupt
- Reset Distribution
- Monitor Digital Signals
- Implements Platform Management Algorithm in Verilog HDL or VHDL



PAC-Designer® Design Software



For ease of design, PAC-Designer software is provided as the primary design entry tool for Platform Manager devices. For more detailed control over complex digital design, Lattice Diamond® design software may also be used. PAC-Designer software can be downloaded from the Lattice website at www.latticesemi.com/pacdesigner.

Lattice provides designs and IP cores that speed implementation of functions commonly implemented in Platform Manager devices, such as fault logging into non-volatile memory, closed loop margining and interface to I²C or SPI bus masters.

Detailed information about the reference designs and IP cores may be downloaded from the Lattice website at www.latticesemi.com/ip.

Platform Manager Development Kit

The Platform Manager Development Kit contains an evaluation board complete with evaluation code and documentation. The evaluation board allows users to see known good hardware in five minutes and to recompile the provided source code to get to a known good starting point in only 30 minutes.

The evaluation board includes support circuits such as LEDs, an LCD display, DIP switches, and analog slider switches to aid in testing Platform Manager's input/output capabilities. Also included is reserved space specifically for user circuit prototyping.

The kit is available from authorized Lattice distributors or the Lattice online store at www.latticesemi.com/ptmdevkit.



Platform Manager Selection Guide

Features	LPTM10-1247	LPTM10-12107
Analog Inputs - Single Ended	5	0
Analog Inputs - Differential	7	12
Total Analog Inputs	12	12
Dedicated Open Drain Digital Outputs	12	12
Dedicated Digital Inputs	4	4
FPGA Digital I/O	31	91
Total Digital I/O	47	107
Margin, Trim, Voltage Scaling & VID Output	6	8
N-Channel MOSFET Drivers	4	4
CPLD Macrocells	48	48
FPGA - LUTs	640	640
Package	128-Pin TQFP	208-Ball ftBGA

Applications Support

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 503-268-8001
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